

# On the Integration of SBT Capacitors on SOI Wafers

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Honolulu

This work was performed at the Jet Propulsion Laboratory, California Institute of Technology,  
under a contract with the National Aeronautics and Space Administration

# Agenda

- Introduction
- Motivation
- Challenges
- Implementation
- Results
- Conclusion

# Introduction

- This presentation represents the hard work of the following organizations:
  - Symetrix Semiconductor, Colorado Springs
  - IC Intelligence, Palo Alto
  - Oki Semiconductor, Hachoji, Japan
- This research was carried out at the Jet Propulsion Laboratory, California Institute of Technology, under a contract with the National Aeronautics and Space Administration

# Motivation

- A need exists for a radiation-tolerant, non-volatile memory device
  - Used for storage of start-up “boot” code,
    - initialization of microprocessors and boards used in spacecraft
  - Used for storage of information from Once-In-A-Lifetime experiences
    - Space exploration
  - GOAL: Develop a truly universal space-rated memory device
    - Replace EEPROM, Flash, DRAM

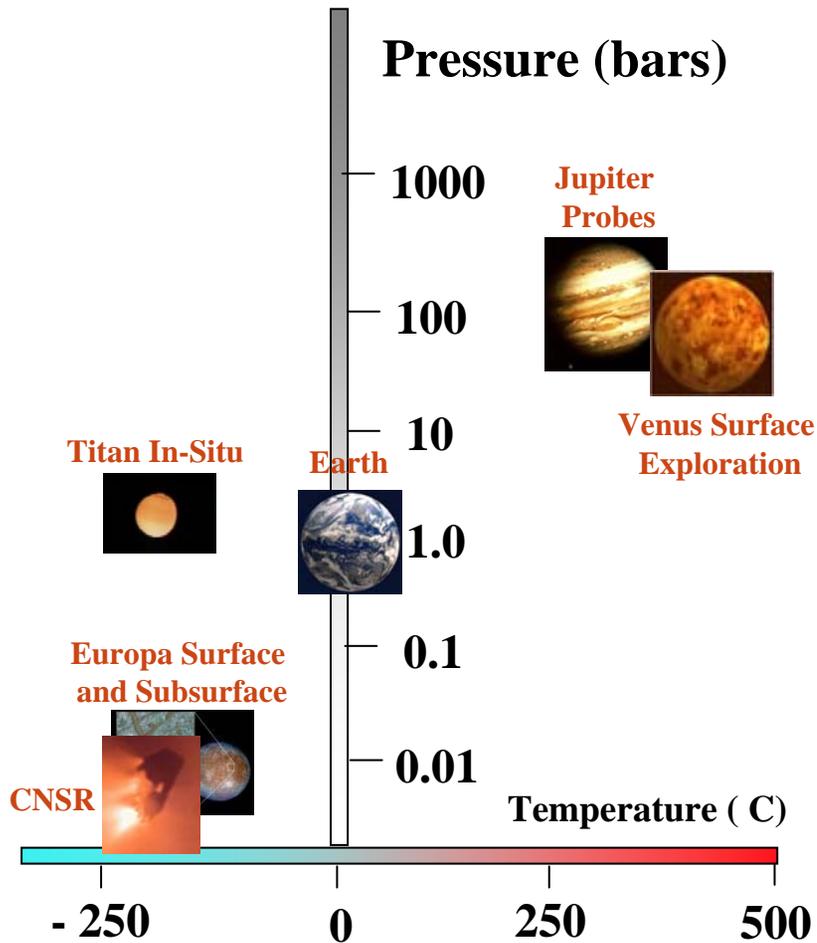
# Challenge:

## Elemental Requirements

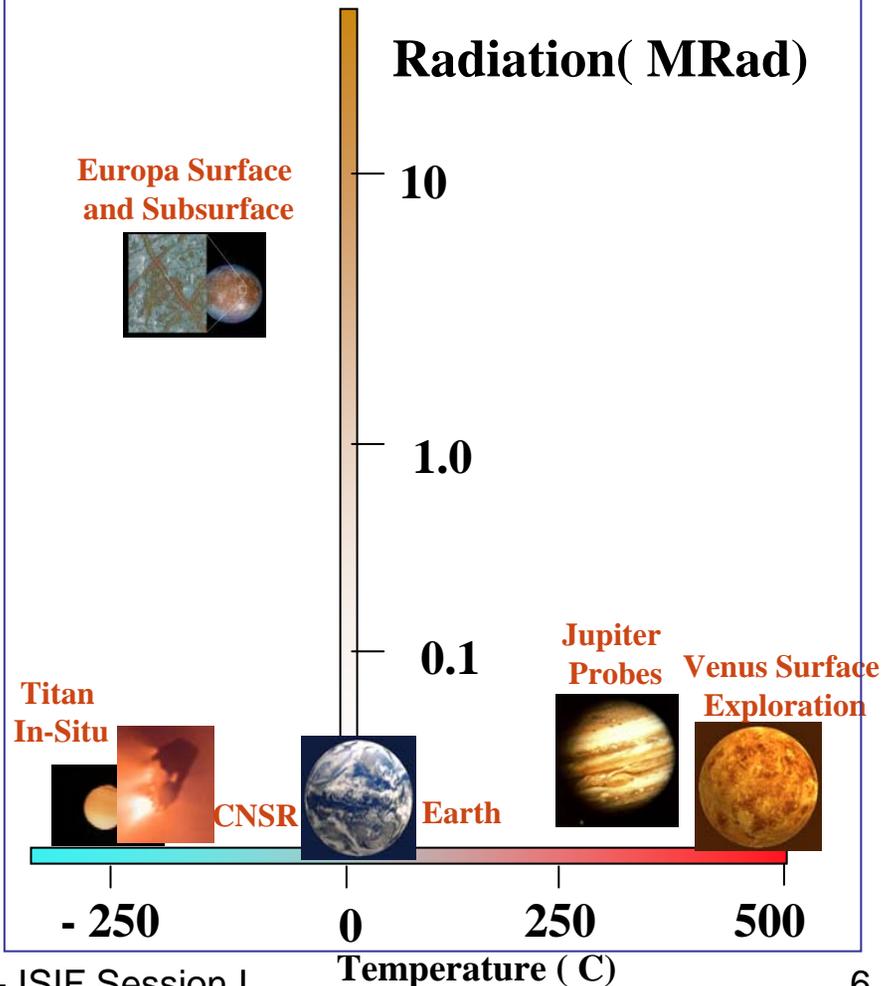
- Low power: <50 milliwatts
- Low voltage operation: 3.3 Volts
- High Speed: <10nS access
- Long data retention: 10 years minimum
- High data availability: Approaching 6-sigma
- High upset threshold due to ionizing radiation
  - Reduction in data upset permits use of more memory and less oversight
- Latch-up immune
  - So-called Heavy Ions can overcome local currents and turn-on parasitic SCR that is in almost every CMOS design
- High radiation tolerance
  - 300 krads (Si) minimum, >1 Mrad goal
    - Better Radiation tolerance, less mass, more science

# Challenge: Environment

## Pressure vs. Temperature



## Radiation vs. Temperature



# Selected Implementation

- Strontium Bismuth Tantalate (SBT) capacitors
  - Spin-on deposition
    - Later, MOCVD
    - Selected due to designer & foundry experience with this material
- Silicon on Insulator underlayer
  - Oki Electric, Fully Depleted 0.2 micron
    - Selected to due known radiation and speed characteristics of SOI

# Development Plan

- Produce & characterize samples SOI Transistor designs with
  - varying L/W ratios, channel lengths
  - Body Ties, No Body Ties
  - Annular design etc.
- 1. Which have not been exposed to Ferro processing temperatures
- 2. Which have been exposed to Ferro processing temperatures
- 3. Ascertain the difference

# Development Plan - 2

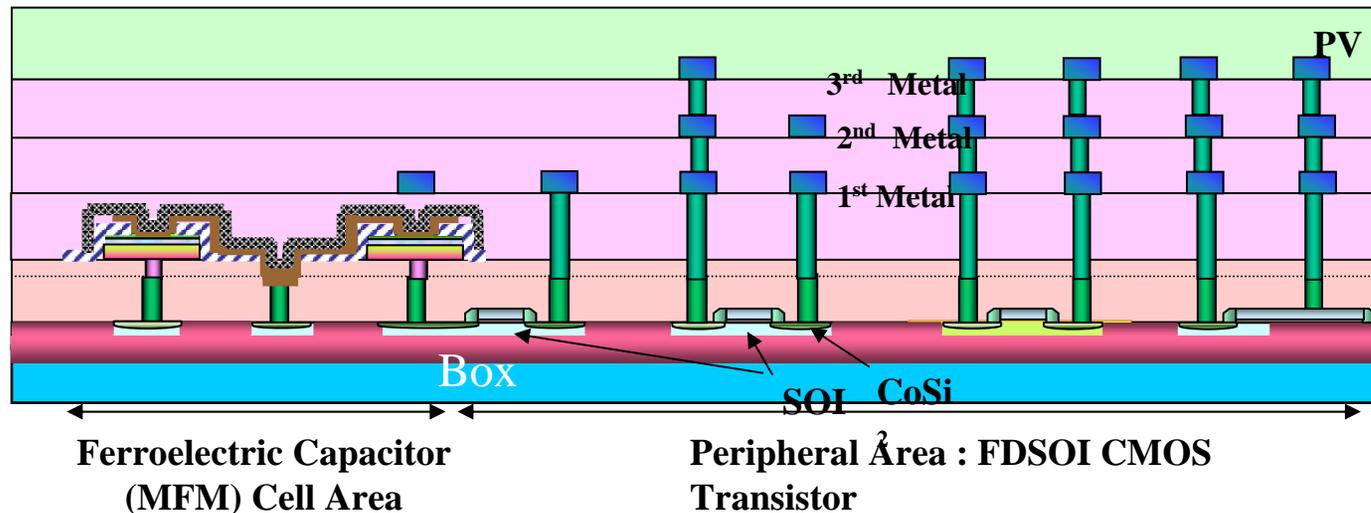
- Produce & characterize samples of selected Ferro capacitors with varying L/W ratios
  1. Which have not been exposed to Ferro processing temperatures
  2. Which have been exposed to Ferro processing temperatures
  3. Ascertain the difference

# Development Plan - 3

- Produce & characterize samples of combined SOI transistors with Ferro capacitors
  1. Which have not been exposed to Ferro processing temperatures
  2. Which have been exposed to Ferro processing temperatures
  3. Ascertain the difference

# Process Challenges

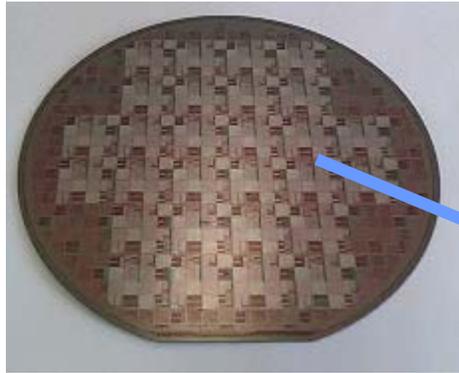
- The instantiation of Ferro-electric capacitors on SOI has never been done before
  - Perceived to be mutually exclusive processes
- Temperatures used in SBT processing can alter performance of SOI transistors
- Hydrogen processing used in SOI formation is poisonous to Ferro-materials



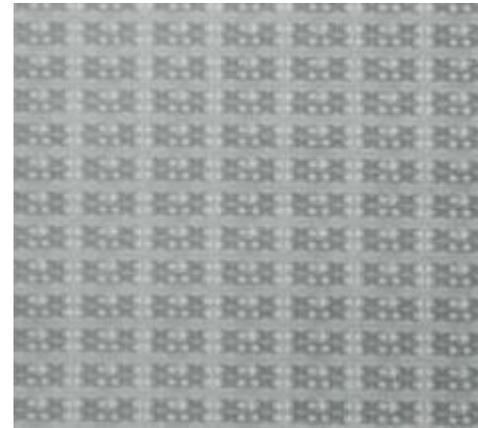
# Innovations

- Oki Electric developed these innovations
  - Inter-layer tungsten plug with very high aspect ratio
    - Development of successful etch-stop to sub- $nM$  level (after etch of 2 micron cavity)
  - Direct plug-to-plug electrical contact without the need for interstitial pad
  - Doping profile change to control threshold voltage shift

# Results – 22 test wafers

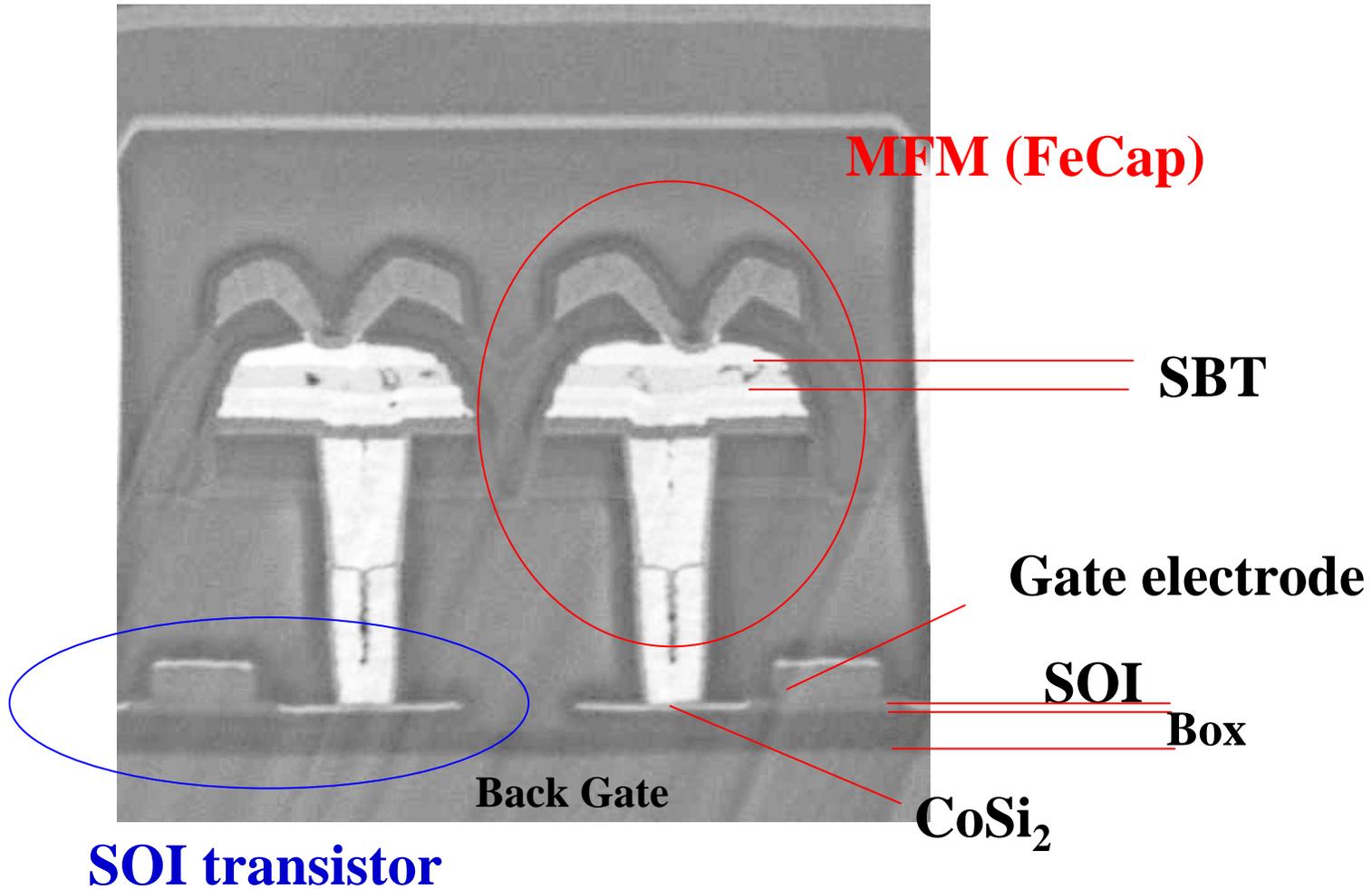


Okii Fe/FD-  
SOI Test  
Wafer



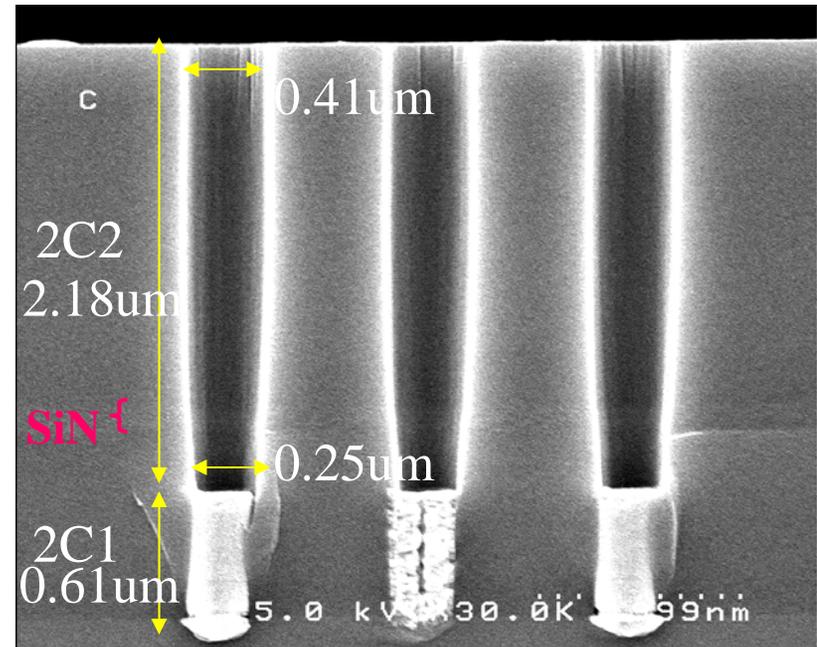
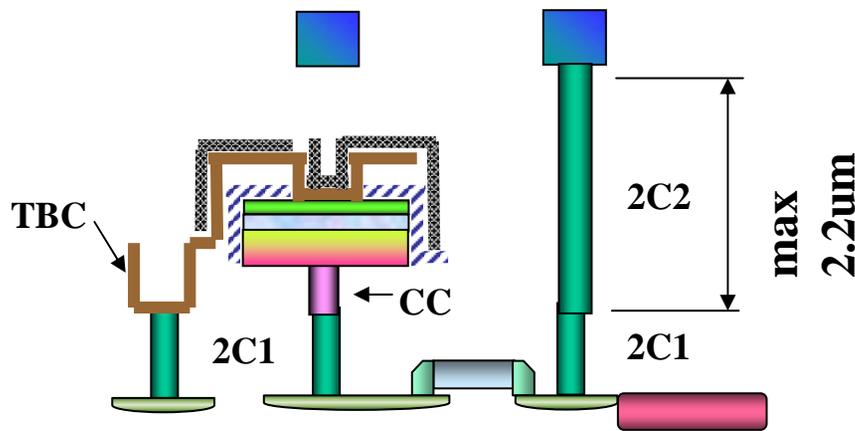
Ferro-electric capacitor array

# First ever ferro capacitors integrated on SOI



# High Aspect Ratio Plug

- High aspect ratio contact (2C2 to 2C1 plug direct contact) required for SOI/MFM integration.
- So as to insert MFM cell between FEOL and 1st Metal, the high aspect ratio which includes MFM-stack and TiN local wiring height became more than 2  $\mu\text{m}$ . Therefore, ultra high aspect ratio contact of 2C2 etching and filling process was required



# Process Splits

- About 2 dozen wafers were produced with about 12 different process splits
  - Time, temperature, doping, forming gas anneal yes/no, alumina deposition HighTemp/Low Temp, Slurry, MOCVD etc etc
  - Conventional & Edgeless, Enclosed Source/Drain
- This afforded the maximum insight into the affects of capacitor processing on the transistor, and transistor processing on the capacitors

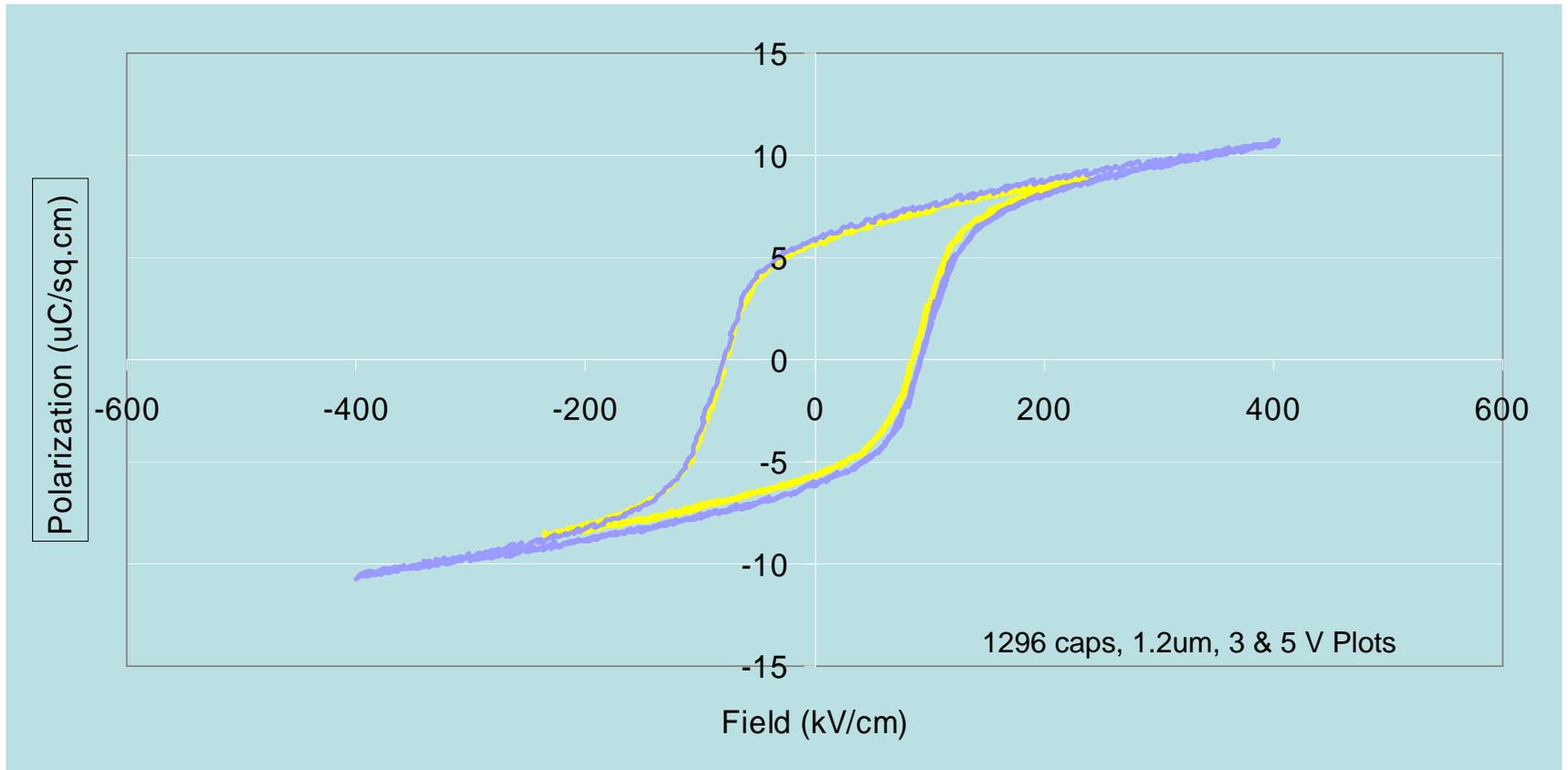
# Testing

- Testing was performed by Oki and IC Intelligence on packaged and bare die
- Some packaged die were shipped to Raytheon, Massachusetts for radiation testing

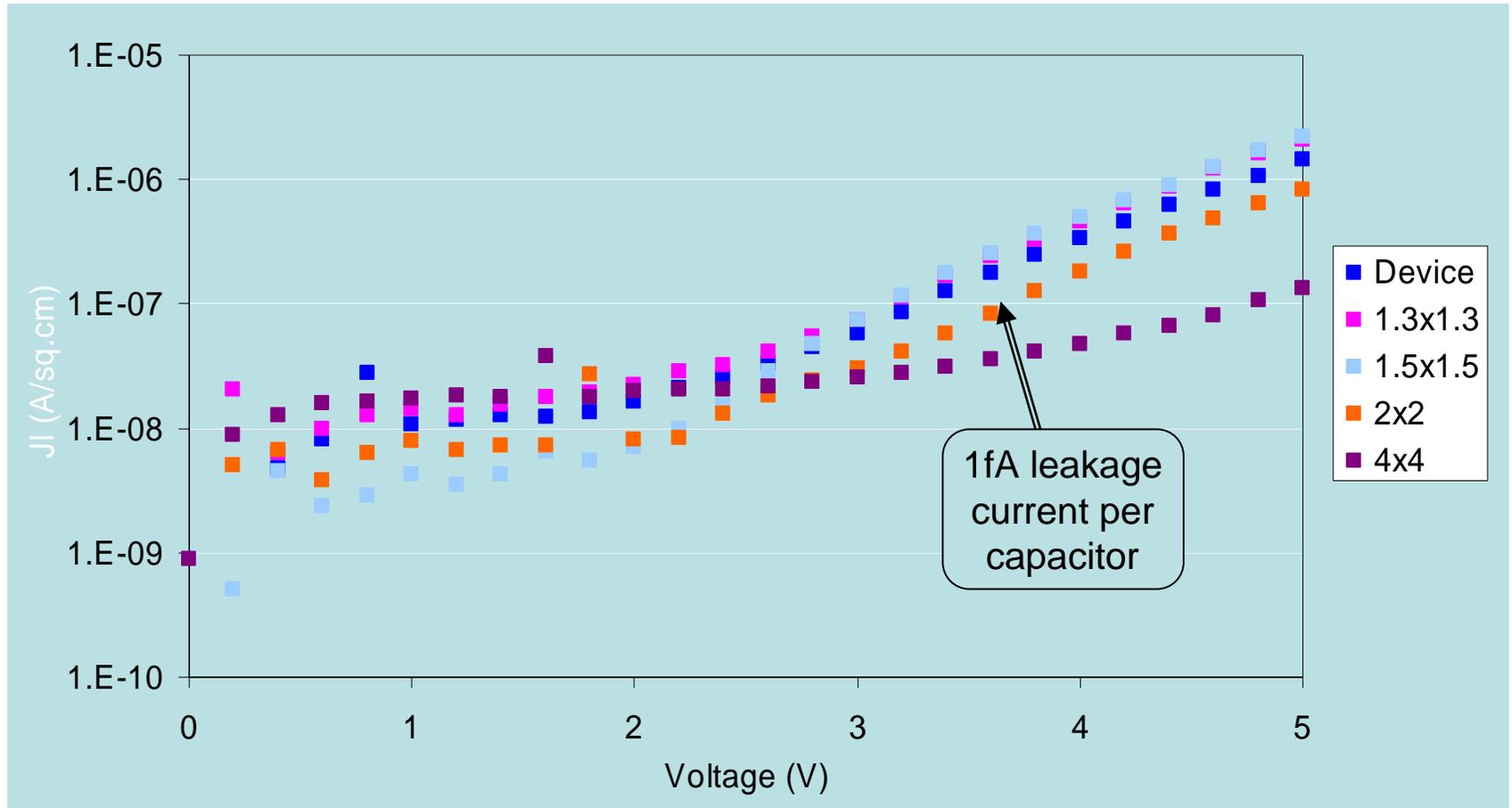
# Results

- Electrical testing shows negligible or no shift in transistor or capacitor parameters
  - Transistor  $V_t$  shift
  - Capacitor Leakage
  - Capacitor Polarization ( $P_r$ )

# SBT Hysteresis Behavior (Integrated Capacitor)

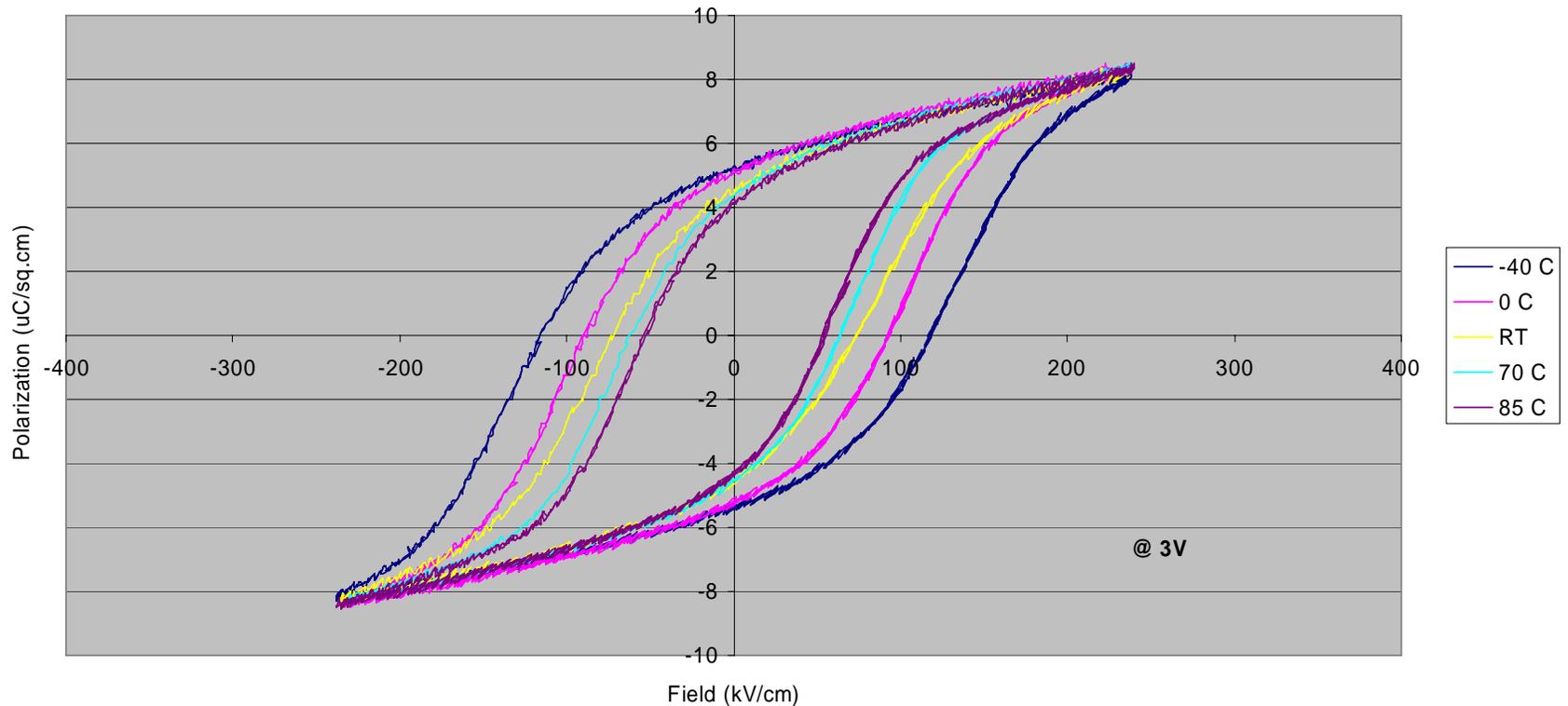


# SBT Leakage Behavior (Integrated Capacitor)

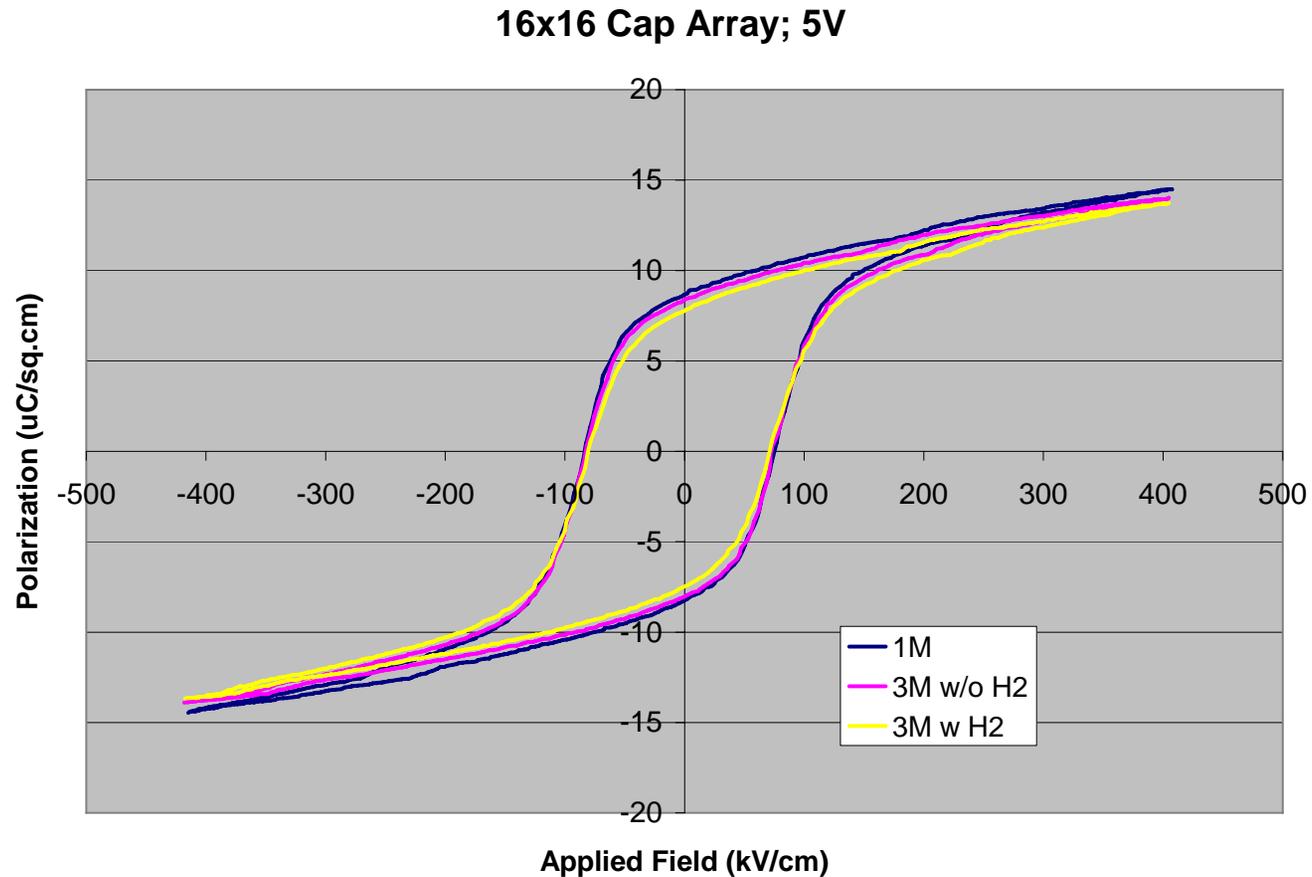


# Ferroelectric Properties

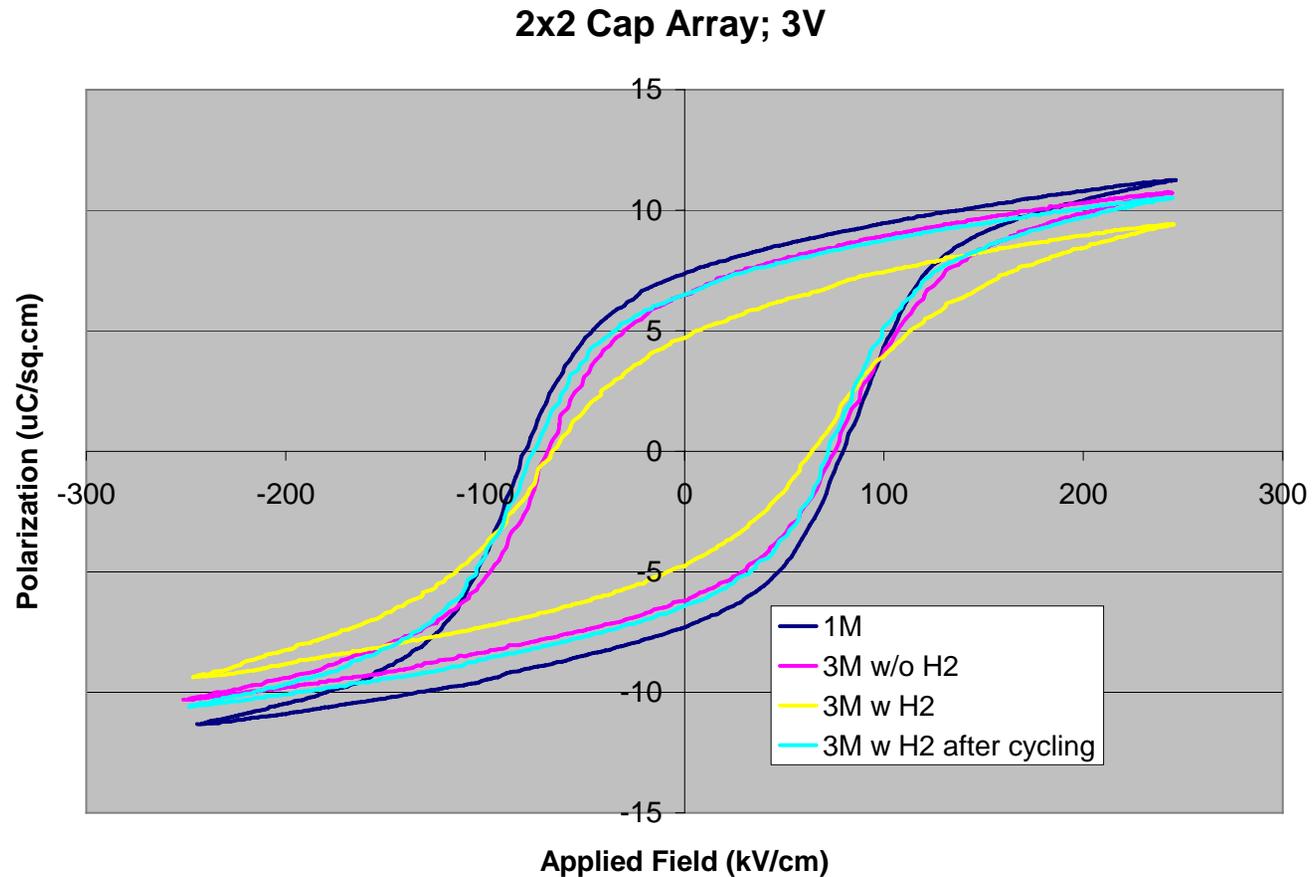
As a function of temperature



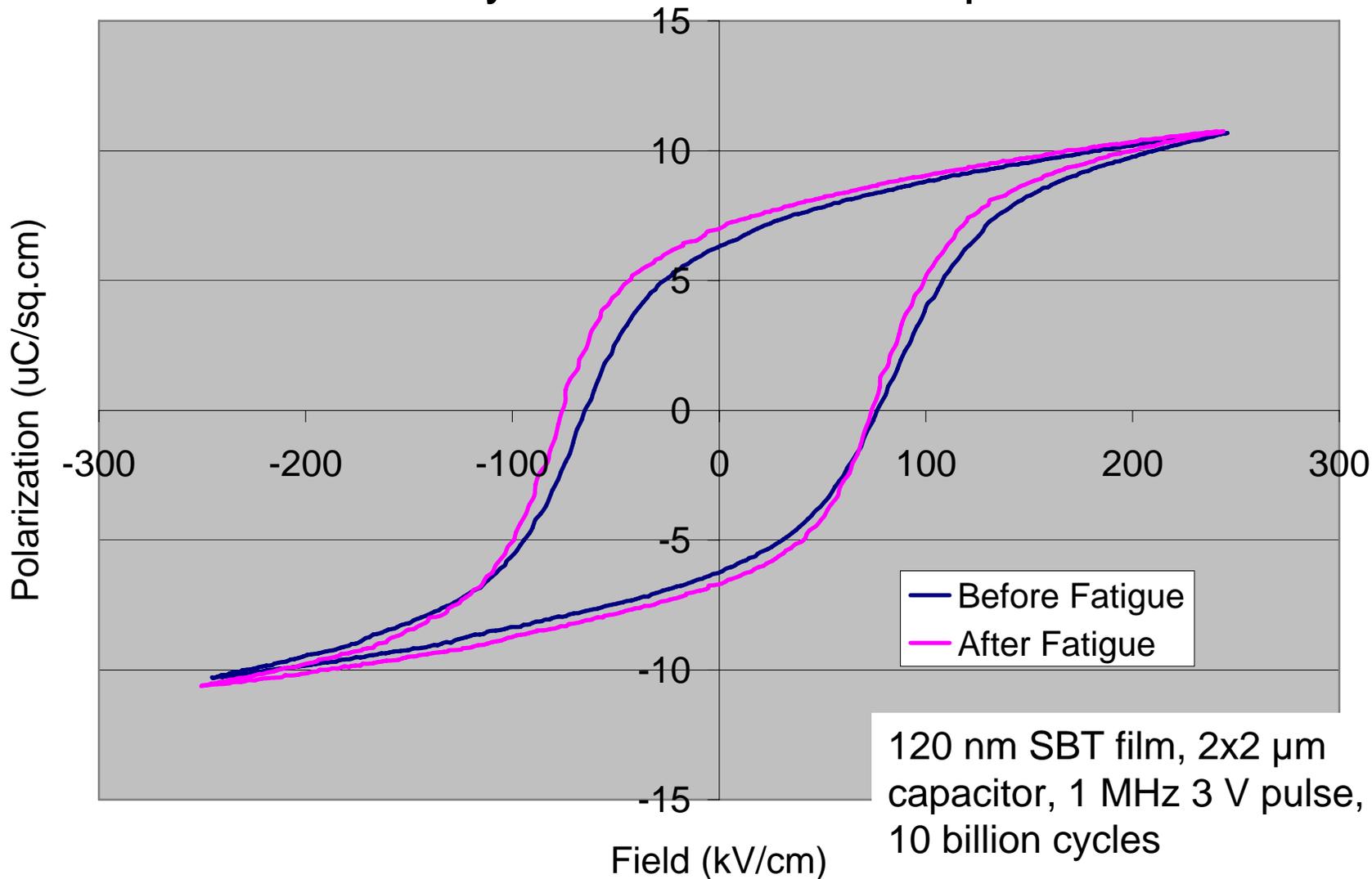
# H<sub>2</sub> Anneal Influence on Larger Fe-Cap



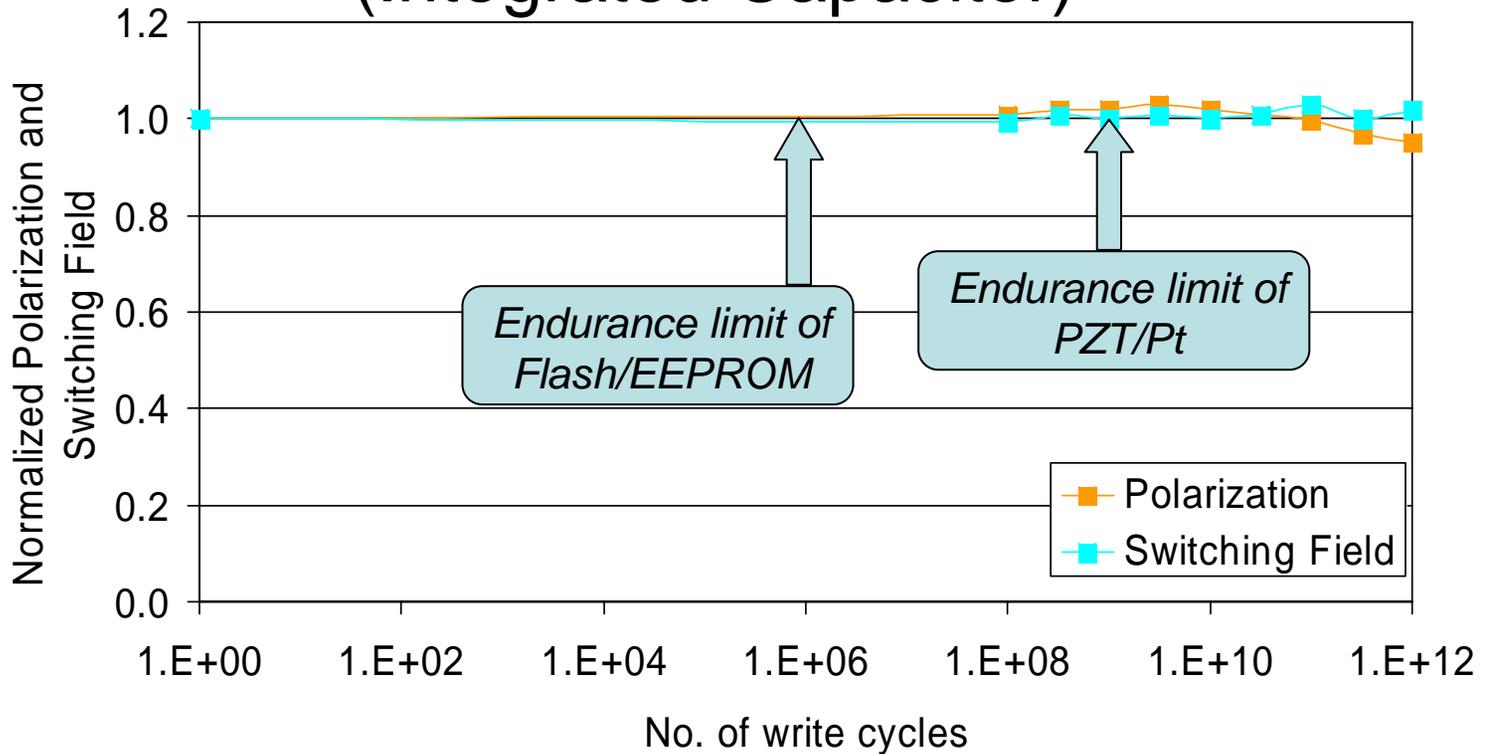
# Recovery of H<sub>2</sub> Anneal Degradation on Fe-Cap by Cycling



# Effect of Voltage Cycling on the Hysteresis of SBT Capacitor



# Endurance Characteristics of SBT (Integrated Capacitor)



***No significant drop in polarization values observed till 1e12 cycles (tested)***

# Process Integration Summary

- SOI Process development completed and adopted
  - Deep Contact
  - Two-step contact under Fe-Cap
- Thermal Budget for Fe-Cap is suitable for SOI integration
- SOI-specific process affects on Fe-Cap are only temporary and can be recovered by cycling < 50 times

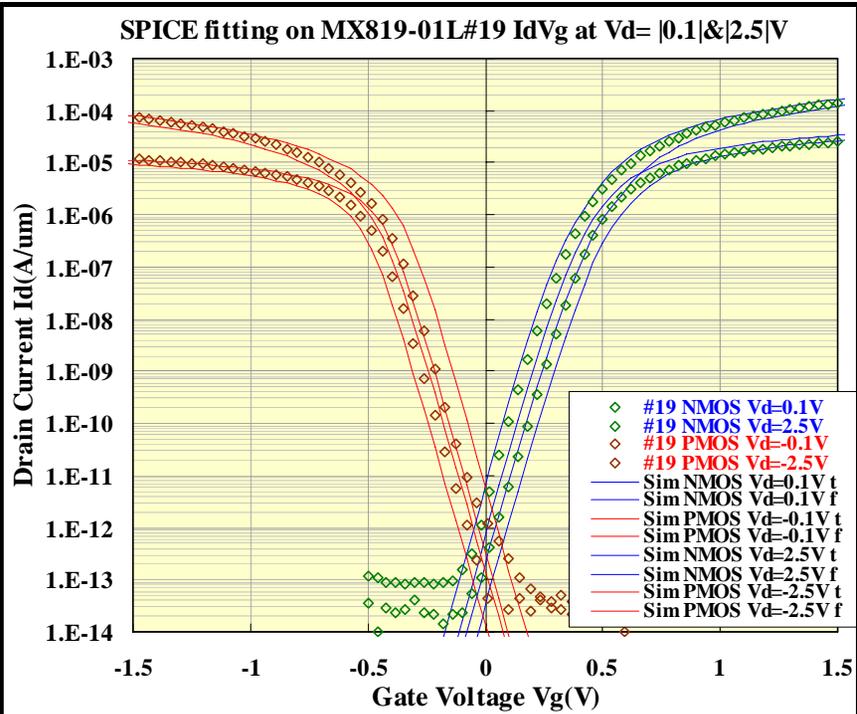
# SOI Transistors

Now that it has been shown that the  
Capacitors survive, what about the  
transistors?

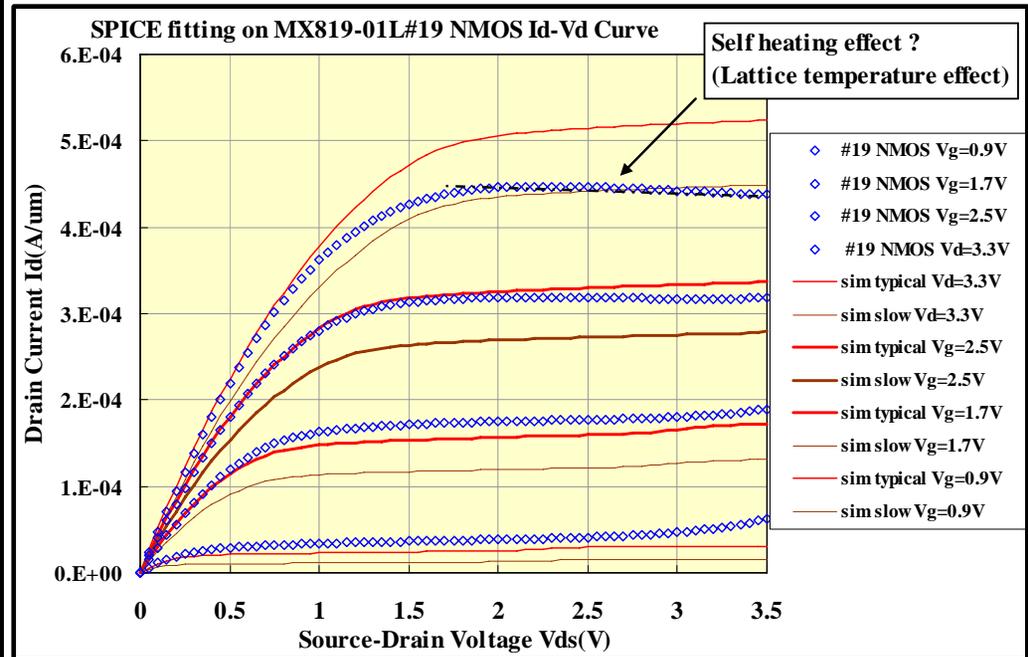
# Transistor Modeling

- A SPICE model was developed to verify that the effect of selected design and process changes can be determined *a priori*
  - Validate the model and then process the transistor
  - Compare
- Will the processing temperatures have a deleterious effect on the transistors
  - Will  $V_t$  shift far enough as to render them useless?

# SPICE Model Fitting compared against a Reference Transistor



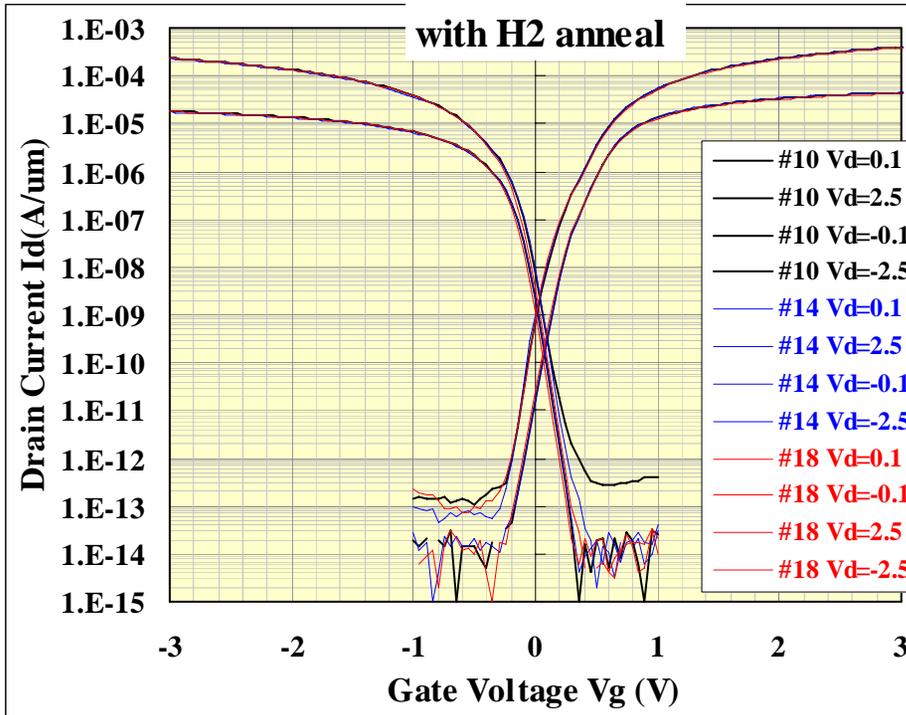
Id-Vg curve



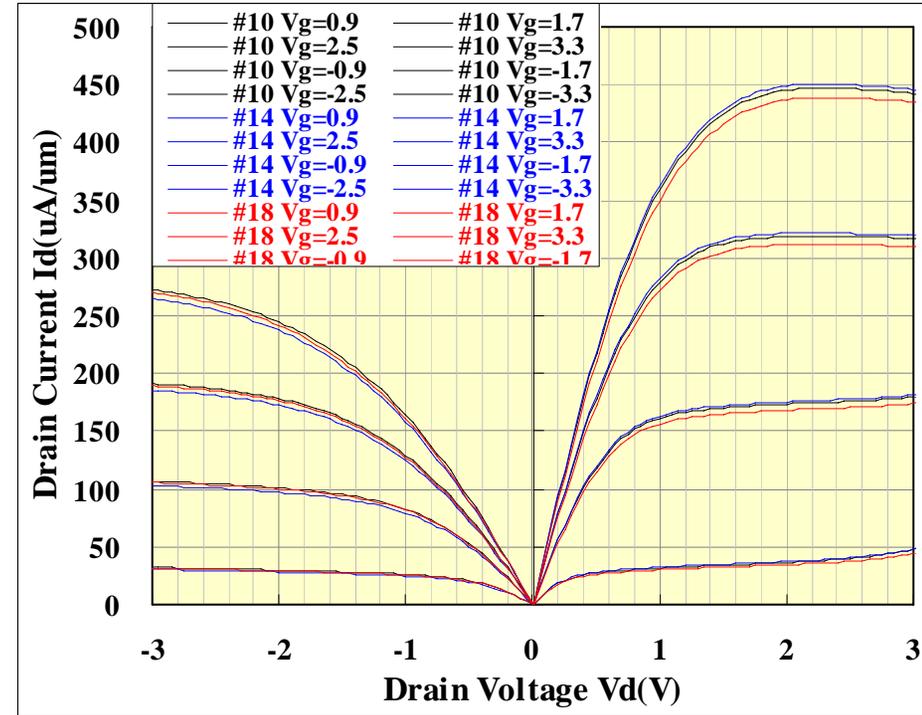
Id-Vd curve (NMOS)

**Confirmed: Observed performance is within Vt skew range predicted by SPICE model.**

# SPICE Model Fitting on the Reference Transistor – Effects of H2 anneal



**$I_d$ - $V_g$  curve**

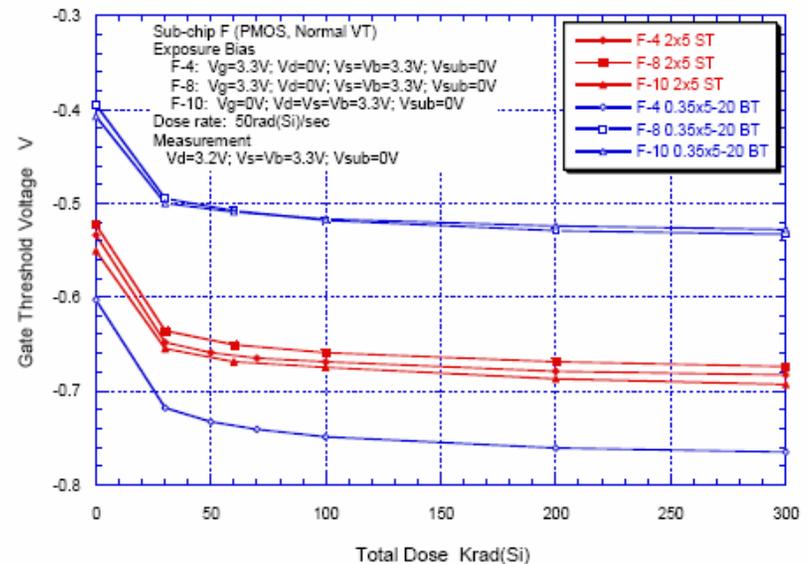


**$I_d$ - $V_d$  curve**

The variations among the wafers (6 chips on 3 wafers respectively) was confirmed to be within 7%

# Radiation Tolerance

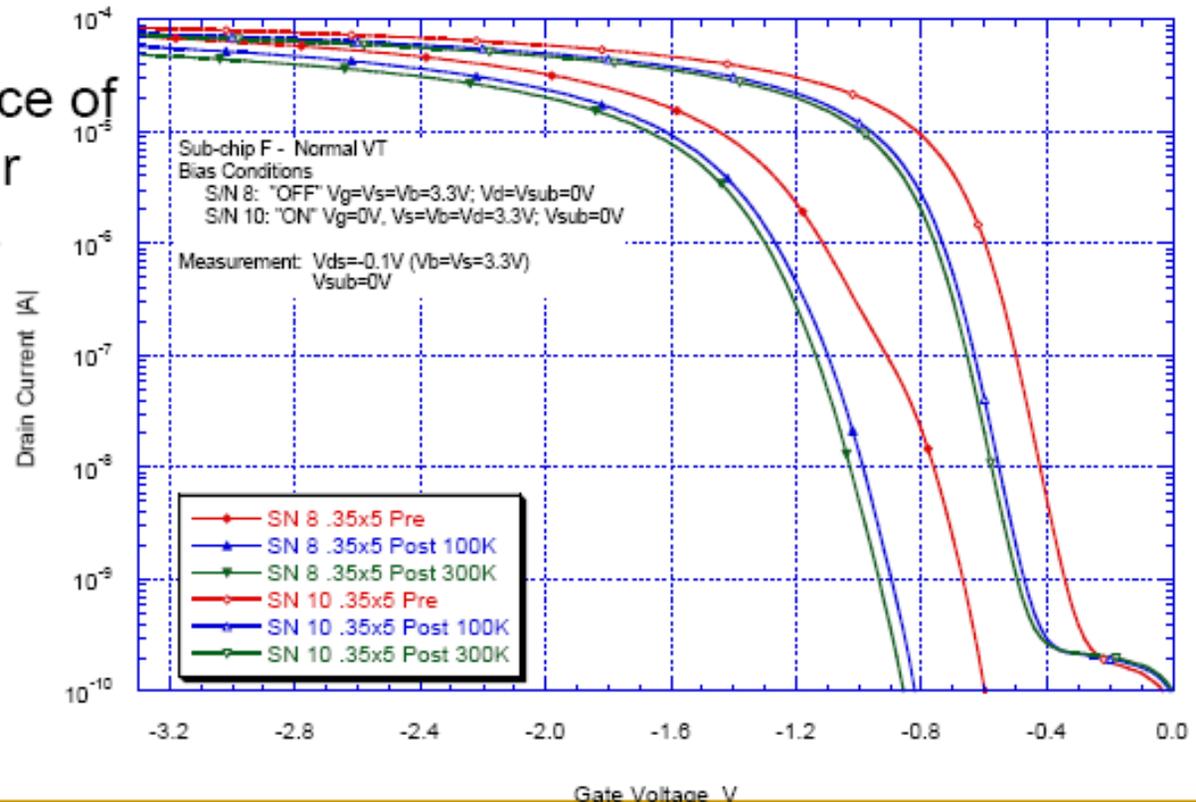
- Threshold shifts <200mV after 300Krad(Si)
- No dependence on exposure bias for conditions examined to date (PMOS ON, OFF with  $V_s=V_b=3.3V$ )



# Radiation Tolerance-2

## Short Channel Device

- No evidence of leakage for either bias condition evaluated



# Radiation Test Results

- Effect of SBT processing temperatures has little effect on the radiation characteristics of the transistors

# Conclusion

- We have shown that the incorporation of Ferroelectric capacitors on SOI wafer is possible
  - That there is some effect on the polarization of Fe-Cap by the SOI processing, but that it can be restored by cycling the capacitor
    - The capacitors have excelled leakage, endurance, retention, and polarization characteristics
  - That the performance of the transistors are predictable and not affected
    - The transistors have excellent radiation characteristics
      - Approaching 300 krads
      - Negligible and predictable  $V_t$  shift assures viable “hardness by design”

# Enabling Technology

- This breakthrough is an enabling technology for low power, radiation tolerant memory devices
  - Will permit the development of one truly-universal space-rated memory device
    - One replaces many and therefore the development costs are significantly reduced