

Advanced Mobility Avionics: A Reconfigurable Micro-Avionics Platform for the Future Needs of Small Planetary Rovers and MicroSpacecraft

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Abstract – Future small and micro-missions, such as Mars Scouts and Deep Space probes, require a new look at highly integrated, re-configurable, low power avionics. This paper will present our plans for developing a scalable, configurable, and highly integrated 32-bit embedded platform capable of implementing computationally intensive signal processing and control algorithms in space flight instruments and systems. This platform is designed to service the need of both small and large spacecraft and planetary rovers that will operate within moderate radiation environments. Some of the key characteristics of this platform are its small size, low power, high performance, and flexibility. This estimated 10 fold reduction in both size and power over state-of-the-art processing platforms will enable this new product to act as the core of a low-cost mobility system for a wide range of missions.

1. DESCRIPTION OF MODULE

The Micro Avionics Module will initially be based upon the commercially available Xilinx Virtex-II Pro Field Programmable Gate Array(FPGA). The resulting product will be a low power, highly scalable, microprocessor-core-based avionics package that can be used alone or within a network. The key characteristics of this Micro Avionics Module are:

- Small size. The module will be less than 10 cubic inches in volume.
- Low power. Depending on how the module is configured, a few hundred milli-watts to a few watts of power consumption are anticipated.
- High computational power. One, two, or four PowerPC 405 processors running at up to 400 MHz are embedded within the Virtex-II Pro gate array. The processors can be voted against each other for increased fault and radiation tolerance or run independently for additional processing capability.
- Support for off-the-shelf operating systems like VxWorks and Linux.
- High I/O count. Hundreds of I/O pins are available. Each is programmable for voltage swing, impedance, and single-ended or differential usage.
- Large number of re-configurable FPGA gates. Up to 8M gates that can be used to implement dedicated functions like brushless motor controller(s), IEEE-1394 interface(s), software

defined digital radio, [3] etc.

- Architectural provisions such as a temperature adaptive power supply or self-controlled local heating so that the components can operate in ambient temperatures that are outside their normal operating temperature.
- Networking capability. Implementing a network controller(s) within the FPGA portion of the Virtex-II Pro is very straightforward and allows multiple modules to be operated in a distributed manner across slow (e.g., I2C) and fast, low latency (e.g., gigabit ethernet) networks.

2. RELEVANCE TO SPACE MISSIONS

This technology will develop low cost, volume and power avionics package aimed at the above class of missions. This technology development task will develop a highly integrated Micro Avionics Module aimed at the avionics needs of both small and large spacecraft and planetary rovers that will operate within a moderate radiation environment. This task will enable low-cost mobility systems for future low cost planetary exploration. In addition this technology can be used on a carrier, an orbiter or a lander spacecraft, on a mission design that requires orderly separation between stages, such as lander and balloon, or cruise and landed stages. This technology is also applicable to large mobility systems, in that it enables a low-cost distributed system.

The applicability of this technology to large mobility missions such as Mars Science Laboratory is best illustrated by the use of the results of this development by the Mars Technology Program. The Micro Avionics Module will be at the heart of the Avionics for a next generation Rover Test Vehicle. This development will make use of four copies of our mobility avionics package, in a distributed system. There will be one module responsible for locomotion, a second module devoted to navigation and planning, a third module devoted to stereo vision processing, and a fourth module used as an appendage and mast controller.

Possible missions applications for this technology include:

- Mars Scouts
- Deep Space probes
- Spacecraft Adjunct missions
- Technology Demonstration missions
- Instrument Controllers
- Planetary Rovers – Micro Rovers
- Microspacecraft

3. VIRTEX-II PRO FPGA

The Virtex-II Pro is the next generation of the Virtex II family with embedded IBM PowerPC 405 Processor hard cores (PPC405), and RocketIO™ Multi-Gigabit Transceivers (MGT) pins. It natively supports the low voltage differential signaling (LVDS) serial interface on hundreds of signal pairs and is capable of running real time operating systems: VxWorks and MontaVista Linux, on its embedded PowerPC processor(s). There could be as many as four embedded processors on a single FPGA, each running at speeds up to 400MHz, 600+ DMIPS. In addition, each RocketIO™ MGT is capable of supporting data rates up to 3.125 Gb/s for high-speed serial transmission standards like Gigabit Ethernet, InfiniBand, RapidIO and PCI Express.

4. AREAS OF RESEARCH

Technology development will be conducted over a three year period with the research proceeding in stages, each culminating in a demonstration of achieved capability. Each stage consists of technology research, application, implementation, and demonstration. Work activities for each stage will be executed in parallel to enable regular demonstrations, so while demonstrating one level of capability, the next level is being researched and developed. Work has progressed in each of the following areas:

- Operating System Selection
- Distributed Control
- Stereo Vision Processing
- Dual Processor Voting
- Next Generation Research Rover Avionics

5. OPERATING SYSTEM SELECTION

The Mobility Avionics Module is being developed using the Xilinx Virtex-II Pro FPGA ML300 board. Two operating systems are available for this architecture: Wind River Systems Tornado II, and Monte Vista Software Embedded Linux. In order to get the task started quickly it was recommended that we start with the Monte Vista Linux Development environment. This allowed us to gain experience with the ML300 prototyping board since it seems to be the more mature product at this time, with the understanding that VxWorks is important to demonstrate for flight relevance. We will re-evaluate adding a VxWorks development environment in the future after we have had a chance to port a few applications to MonteVista.

6. DISTRIBUTED CONTROL

Using the Rocky 8 rover, the Mobility Avionics task demonstrated control of a distributed processing hardware architecture. Rocky 8 is an experimental robotic platform

designed to test software algorithms. For control, this rover uses a distributed approach where every motor has a dedicated processor. These processors are interconnected via a 100Kb/s I2C bus. For this demonstration we physically removed the Compact PCI chassis whose computer acts as the computational master on the I2C bus. For reference, this chassis and its associated chassis consumed on the order of 40W. Our electronics consumed on the order of 5 watts or less to perform the same task. We ported the 100,000+ line CLARAty code to execute on top of Linux, which was running on the PowerPC contained within the Virtex II Pro. We then demonstrated closed loop control of 12 motors at 50 Hz using the CLARAty Locomotor code running on the Virtex II Pro. We have demonstrated that we can run computationally intense code, which was ported over quickly from a VxWorks platform with a significant power and mass savings. Moreover, this allowed us to leverage the 5M\$+ CLARAty investment.

7. STEREO PROCESSING

Stereo image processing is an important step in rover navigation. Stereo images are used to generate range maps for hazard avoidance. The Mobility Avionics Module can be used for real time range map generation. Stereo Vision processing is done using the CLARAty [2] implementation of the JPL stereo processing algorithms. The stereo algorithms, as implemented in CLARAty, were ported to the MontaVista development environment. These algorithms can be used to process stereo imagery received via the ethernet interface, or imagery produced by cameras connected to a local firewire (IEEE-1394) interface. Timing tests show that 128x128 pixel images, the size used by MER hazard avoidance cameras, take 1 to 3 seconds to process. On MER these images take over a minute to process including transferring the raw image data from the camera. This demonstrates the increased processing throughput and improved data transfer rate. We have since further optimized this code and are now getting code getting 7.5Hz disparity on 160x120 images, including decimating from 640x480. This processing of the stereo images was done in software using the internal 300MHz processors of the Virtex II Pro. In the future we intend to port this code into to the hardware of the FPGA. In doing so, we expect to get a very significant improvement in stereo image processing.

8. SEU MITIGATION

This area of research focused on designing methods to mitigate the effects of SEUs on the Xilinx Virtex-II Pro. The task is in the process of developing a mitigation method that includes error detection, error correction and software notification. The SEU susceptible areas of the Virtex-II Pro can be logically divided into the following categories:

- Flip-Flops
- Configuration Memory

- Block SelectRAM
- PPC L1 cache
- PPC Registers and Misc Logic

Each of these areas of susceptibility has its own fault statistics and requires its own mitigation method. The first step in this process is to develop a total mitigation solution as quickly as possible. This method will be further refined in future work. The first solution is “quick and dirty” and may involve less than desirable techniques such as total device reset and reconfiguration as a means of error correction. This technique will allow us to have a radiation hard solution quickly for non-critical applications such as stereo processing. We will take advantage of previously developed mitigation techniques, such as the configuration read-back circuitry developed for MER. This circuitry reads back the configuration memory and compares a generated checksum to a known value. A total device reconfiguration is executed if the generated checksum does not match to a predicted value.

Work in this area has proceeded in a systematic manner facilitated by concentrating on the most susceptible areas of the device. Based on the data that were obtained from a previous SEU susceptibility test done on the Virtex-II family[1], which precedes the current Virtex-II Pro family, each group has the following normalized upset rate: Flip-flops (3%), Configuration Memory (22%), Block SelectRAM (11%), and PPC L1 Cache (64%). Since Virtex II family doesn't have PPC processor, the L1 Cache value was calculated using the highest upset rate among the groups. Based on the upset rate and intrinsic characteristics of each category, the appropriate error detection and mitigation methods can be chosen accordingly.

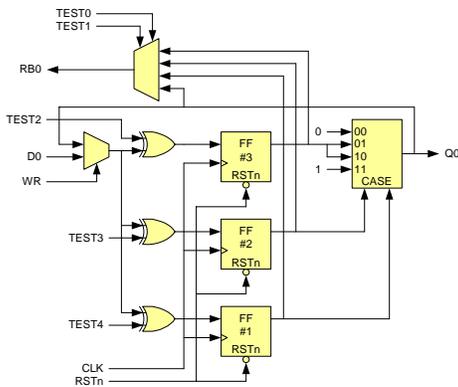


Figure 1: Generic TMR Voting

For the Flip-Flops section, Triple Module Redundancy (TMR) can be used for error detection and correction. This circuit is shown in figure 1. For the Configuration Memory, memory scrubbing can serve as a detection method and device reconfiguration can help to mitigate the error. For the Block SelectRAM, Parity/ECC has been proposed as the best detection mechanism and detected faults are to be mitigated by using error flag/

correction. As for the PPC L1 Cache which is the most error prone, processor-voting has been proposed as the detection method while mitigation is based on the processor-interrupt approach. The design implementations of these approaches will be investigated in the future phases of the project.

Processor Voting: With the availability of embedded PPC processors on the Xilinx Virtex-II Pro FPGA, processor voting can be an effective method for single fault detection and correction. By comparing results calculated from multiple processors executing the same program, a mismatch indicates the presence of a fault. This comparison can be pair-wise, or it may involve three or more processors simultaneously. We have completed the design and high-level simulation of a pair-wise single fault detection scheme as shown in Figure 2. In such a scheme, once a fault is detected by comparing the calculated result on the buses, both processors will be notified through the interrupt mechanism, and appropriate actions could be taken.

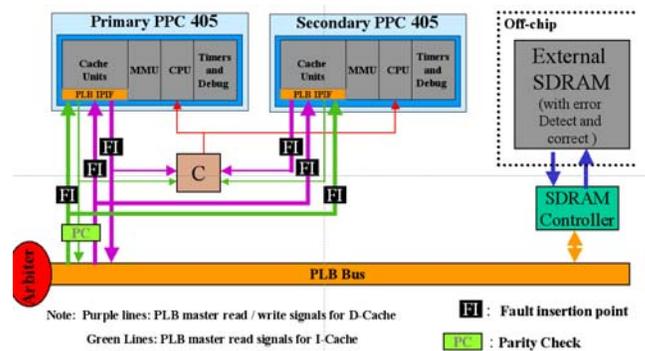


Figure 2: Processor Voting Hardware

In the future, we will expand the design schemes to include error correction as well using three or four processors. We will explore error mitigation methods such as pair-and-spare, triple-module redundancy, and quadruple-module redundancy. In addition, an efficient software based recovery mechanism will be studied and implemented as well.

9. PROOF OF CONCEPT: NEXT GENERATION ROVER AVIONICS

We are currently in the process of developing a two-board hardware system to replace the Xilinx ML300 development system. This two board hardware system is optimized for Mobility Research. The first of the two boards is the CPU board which supplies all the basic infrastructure for the system, including memory, I/O and extra busses. The second board is designed to provide the mobility platform application specific circuitry which includes motor drivers and analog to digital conversion. These two boards are illustrated in the following figures.

The CPU Board shown is for debugging purposes. The final version of this board will be in PMC format.



Figure 3: Debug CPU Board Front Side

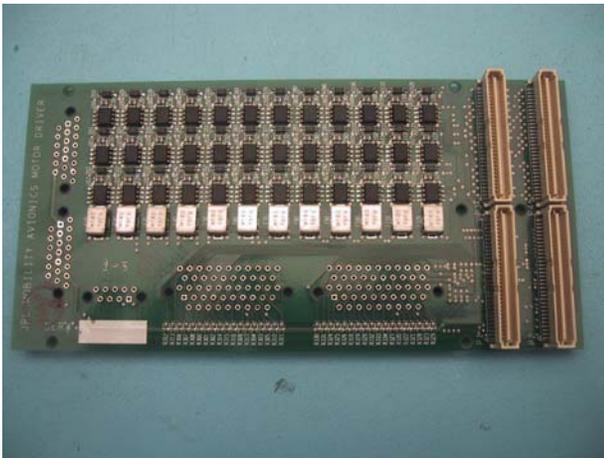


Figure 4: Motor Driver Board Front Side

10. CONCLUSIONS AND FUTURE WORK

Recent advances in semiconductor technology have enabled commercially available FPGAs to have multiple embedded micro-processor cores. In this study, we have successfully demonstrated the effectiveness of processor voting as a SEU mitigation technique for the embedded PowerPC of the state-of-the-art Virtex II Pro FPGA.

Future work will be focused on further development of Virtex II Pro SEU mitigation techniques, software techniques for SEU handling, vision processing and benchmarking. In the area of SEU mitigation we will be developing methods for detecting SEUs as they occur in various parts of the device, correcting the subsequent errors that our introduced and notifying the Flight Software as appropriate. Software techniques developed will focus on fault handling software and fault injection. Radiation testing will be done to verify the techniques developed. We are currently in the process of

incorporating some of the JPL stereo processing algorithms directly in FPGA hardware. In the area of benchmarking we will measure raw processor and stereo processing performance.

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