

VLSI Design of Turbo Decoder for Integrated Communication System-On-Chip Applications

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Abstract

A high-throughput low-power turbo decoder core has been developed for integrated communication system applications such as satellite communications, wireless LAN, digital TV, cable modem, Digital Video Broadcast (DVB), and xDSL systems. The turbo decoder is based on convolutional constituent codes, which outperform all other Forward Error Correction techniques. This turbo decoder core is parameterizable and can be modified easily to fit any size for advanced communication system-on-chip products. The turbo decoder core provides Forward Error Correction of up to 15 Mbits/sec on a 0.13-micron CMOS FPGA prototyping chip at a power of 0.1 watt.

1. Introduction

A great interest has been gained in recent years by a new error-correcting codec technique, known as “turbo coding” which has been proven to offer performance closer to the Shannon’s limit than traditional concatenated codes [1, 2].

As shown in Figure 1, the turbo code allows communication at lower E_b/N_0 (i.e. energy per bit to noise power spectrum level ratio). The turbo code achieves better coding gain than traditional codes. It is also a simple decoding strategy and allows uncomplicated hardware implementation. Therefore it has been adopted by important broadband communication applications and standards such as DVB-RCS (Digital Video Broadcast – Return Channel Satellite) and the 3G wireless communication.

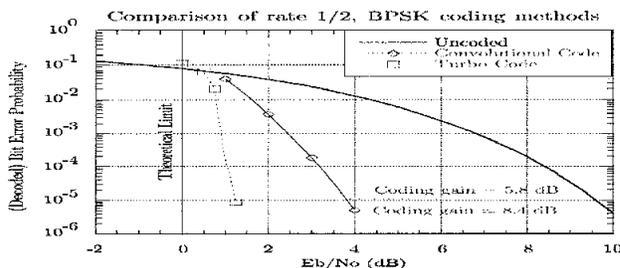


Figure 1 Turbo Code Performance [1]

This paper reports a high-throughput low-power turbo decoder core for integrated communication systems such as Digital Video Broadcast (DVB), satellite communications, wireless LAN, digital TV, cable modem, and xDSL systems. In section 2, we address the turbo decoder architecture and design issues. Section 3 describes detailed functional implementations of the turbo decoder. Section 4 presents the executable model of the turbo decoder in Verilog and its FPGA implementation.

2. Architecture Design of the Turbo Encoder

The turbo encoder is equivalent to two convolutional encoders plus, a look-up table (LUT) to store the interleaver addresses. The turbo decoder includes two soft output decoders plus a random access memory (RAM) for the interleaver/deinterleaver functions. The soft output decoders can be either Soft Output Viterbi (SOV) decoders or Maximum A Posteriori (MAP) decoders [2]. MAP decoders give 0.5 to 1.0 dB more coding gain than Soft Output Viterbi decoders and are approximately two times more complex in number of equivalent computations. The SOV algorithm is considerably simpler than the MAP algorithm. It is basically the Viterbi algorithm with some small changes. The largest change is in the add-compare-select (ACS) circuit where the difference between path metrics into a state is calculated. The difference for each state is stored along with the path decision. Trace-back occurs as normal with the absolute difference used to indicate the reliability of a decoded bit. A difference of zero indicates that the bit is very unreliable, while a large value indicates a reliable value.

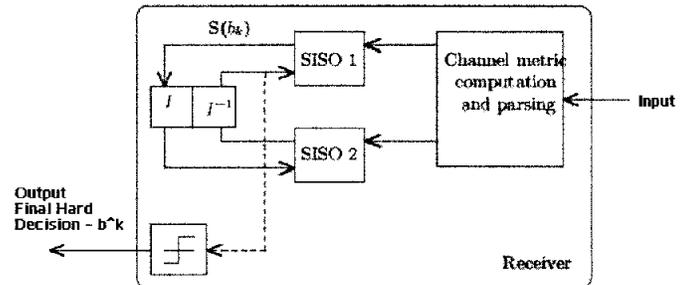


Figure 2 Block Diagram of Turbo Decoder.

Figure 2 shows a block diagram of turbo decoder of a receiver. The received sequence from the channel is first processed and parsed through the channel metric and parsing block. The output of this block is a sequence of estimates that indicate how close each received bit looks like a 1 versus a 0. On these estimates SISO1 generates “soft decisions” which tell what the probability of each received bit being a 1 or a 0 based on the given sequence of bits received. These soft decisions are then permuted to be input to SISO2. The SISO2 outputs “soft decisions” based on not only the estimates from the channel metric computing and parsing block but also the soft decisions from SISO1. These soft decisions are again interleaved and sent to SISO1. Now, SISO1 has more information to work than the last time it tried to decode the sequence and it can use this soft information hopefully do a better job this iteration.

This iterative decoding process is repeated either a fixed number (e.g. 10 times) of times or until some coverage criteria is met. Once finished, based on the soft decision, hard decisions are made. Intuitively, if the probability of a 0 is higher than that of 1 the hard decision will guess that a 0 was sent, otherwise it will guess that a 1 was sent. Notice that the SISO in general perform the following function. They take in as input information from the channel and soft decisions from the other SISO and output soft information. For this reason they are called Soft-Input/Soft-Output decoders.

3. Functional Design

Figure 3 shows the functional diagram of the SISO decoder. Descriptions of these functional blocks are presented in the following.

3.1. FSM

An important part of the code is the FSM or the control Machine. This describes the states used. This decoder uses 5 states as shown below.

- State0 (S0): Initial State.
- State1 (S1): Reads sequence for Interleave and de-interleave. The de-interleaving sequence is derived from the interleaving sequence.
- Wait State (SWAIT): Idle state which awaits the Start signal when channel info is available.
- State2 (S2): Reads ck1 and ck2 channel information. The channel information are read in a separate state from the interleaving sequence so that one can now read new channel info without having to read the interleaving/de-interleaving sequences again.
- State3 (S3): Perform the operations for Forward and Backward calculations in SISO.
- State4 (S4): Perform operations for ISOs, that is the Intermediate Soft Outputs and interleave or de-interleave them depending on the iteration. If iteration is 20 then proceed to S5 else start the SISO again at State S3.

When iteration reaches 20, it means that the information has run through SISO1 and SISO2 10 times.

- State5 (S5): Send out Hard Decisions based on the Final Soft- Outputs.

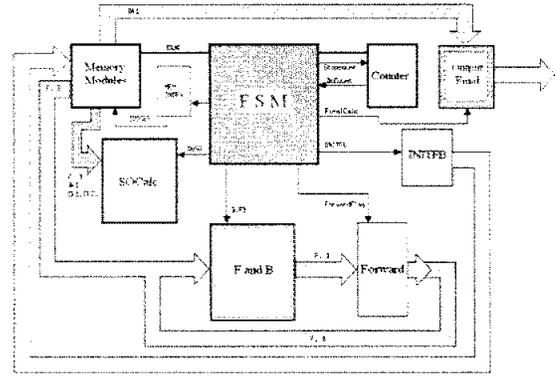


Figure 3 Functional Diagram of the SISO Decoder

State Diagram:

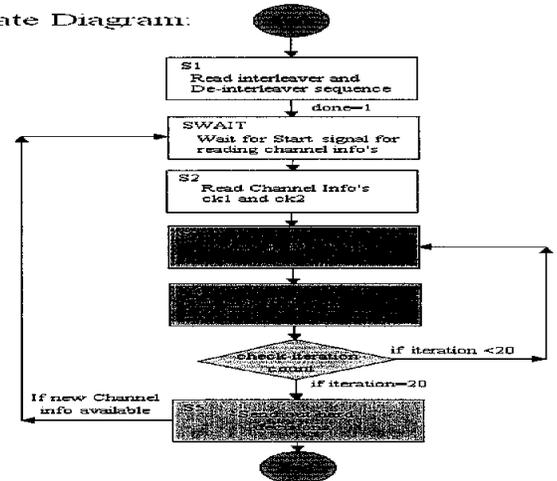


Figure 4: FSM of Turbo Decoder

3.2 Memory Implementation

Now, what is of extreme importance to the whole design is the way in which memory operates. Basically, at the beginning of a cycle (on the pos-edge of clock), any Read that needs to be done from memory is executed. However, the read is done with a small delay. The write is then done at the end of the cycle – on the following pos-edge of clock. The reason for the small delay in read is to ensure that both read and write are done during the same clock cycle using the same ‘Count’ value from the counter module.

3.3 Forward/Backward Implementation

The module used to calculate values for the Forward and Backward arrays is called the FANDB

module. It uses 8 ACS modules – four to calculate the Forward values and four to calculate the Backward ones in parallel. In this module, shown in Fig. 5, the critical path consists of one 1-bit compare unit, two 7-bit multiplexers, two 7-bit adders and an ACS unit. Basically, this module is simply combinational logic working asynchronously that takes in certain input values and puts out a stable output after a delay. An important point to be noted here is that the output from the FANDB module is saved in registers in the FORWARD module. The reason for this is to implement forwarding which is needed because in successive cycles, the next Forward/Backward calculation iteration, need the values “just” calculated; but one cannot write and read from the same memory location at the same time. Hence forwarding has been implemented.

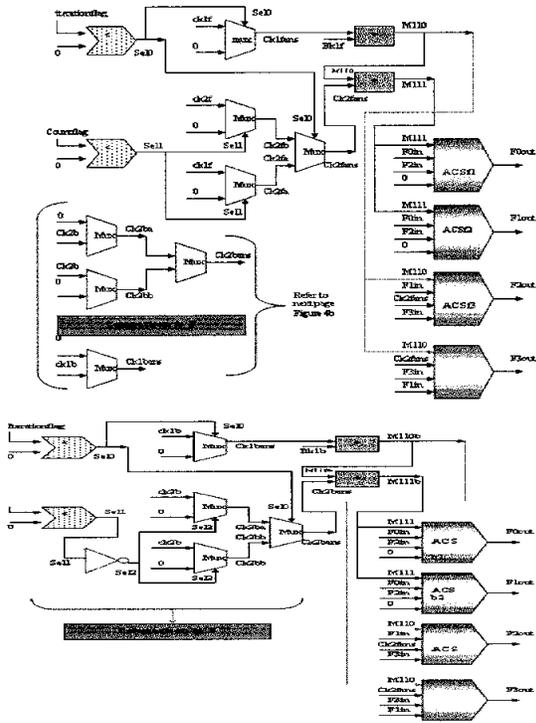


Fig. 5: Forward and Backwards calculation

3.4 SO Calculation Implementation

The SO calculation is done in the SOCALC module as shown in Fig. 6. It is similar to the FANDB module in that it is simply combinational logic which works asynchronously and simply spits out a constant result after a time delay. Here the critical path consists of a 1-bit compare unit, seven 7-bit multiplexers, four 7-bit adders, an ACS unit, two 7-bit compare units, a 4-bit compare unit, two 7-bit subtract units. It uses 4 ACS units total.

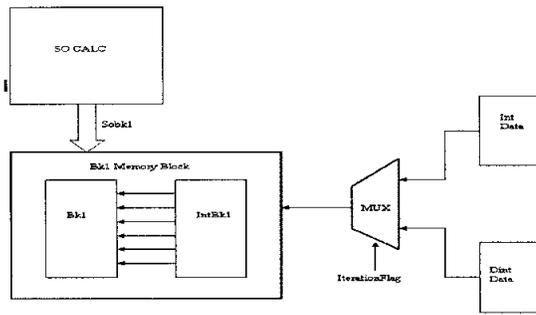


Fig. 6: SO Calculation

3.5 Add Compare Select (ACS) Module

The ACS module is implemented as shown in Fig.7. It uses the basic adder, compare, and multiplexer units.

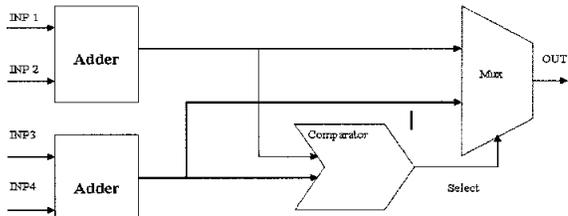


Fig. 7: ACS

3.6 Interleaver/De-Interleaver

The actual interleaver construction has a large influence on the performance at high SNR's. Therefore, finding good interleavers matched to the specific component codes used is important. That is interleavers where the low weight words for the first component code are not interleaved to low weight words for the second component code.

The graph shown in Fig. 9 is very critical in order to understand the influence of the interleaver design on the overall decoder performance. Essentially, the interleaver size increases, the decoder performance increases. But this only happens till a threshold or saturation value, after which, the performance enhancement reduces with respect to the hardware complexity. This basically means that after this interleaver size, the system obeys the “law of diminishing returns”. In our design, we observed this threshold interleaver size to be 1024 bits, and hence we have designed this size in our behavioral and structural model.

4. Executable Model in Verilog and FPGA Implementation

Figure 8 illustrates the structural model of the interleaver. Here, we use the 2-SISO model to increase the

speed of execution and hence use the iterative decoding algorithm which has been explained earlier. Our code was synthesized in Synopsys and design was further optimized to further improve area-timing constraints. The entire code is parameterized, which means the whole code can be modified easily to fit any size for advanced communication system-on-chip products. Simulation results are shown in Figure 10. A FPGA prototype chip of the turbo decoder core has been implemented. It provides Forward Error Correction of up to 15 Mbits/sec at a power dissipation of 0.1 watt.

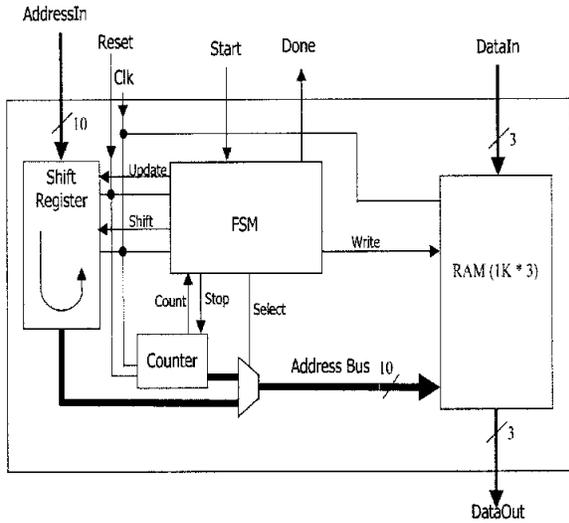


Figure 8: Interleaver

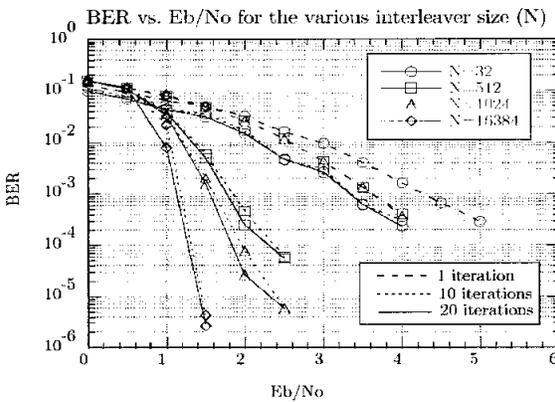


Figure 9: Interleaver Size

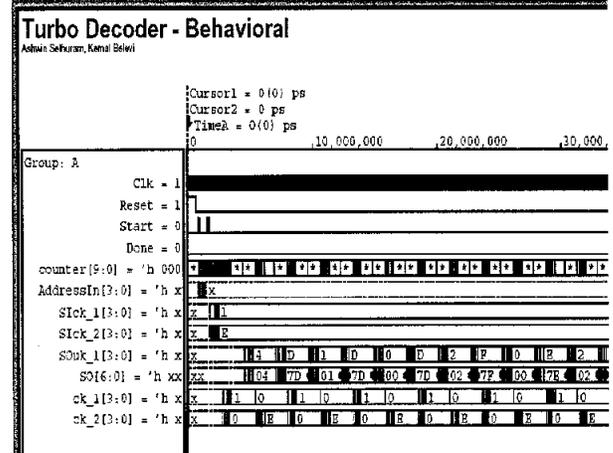


Figure 10. Simulation Results

5. Conclusion

A high-throughput low-power turbo decoder core has been developed for integrated system-on-chip applications. This turbo decoder core is parameterizable and can be modified easily to fit any size for advanced communication system-on-chip products. A FPGA prototype chip of the turbo decoder core provides Forward Error Correction of up to 15 Mbits/sec at a power of 0.1 watt.

6. Acknowledgments

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Development Costs:0 (Please estimate within 50K)	Additional Development Dollars Anticipated: 0

New Technology Description

Novelty
Describe what is new and different about your work. Attach supporting material if necessary.

- The turbo decoder is a high-throughput low-power core for communication system-on-chip applications.
- The turbo decoder is based on convolutional constituent codes, which outperform all other Forward Error Correction techniques.
- This turbo decoder core is parameterizable and can be modified easily to fit any size for advanced communication system-on-chip products such as satellite communications, wireless LAN, digital TV, cable modem, Digital Video Broadcast (DVB), and xDSL systems.
- A prototype chip of the turbo has been implemented into a 0.13-micron CMOS FPGA. This chip provides Forward Error Correction of up to 15 Mbits/sec at a power of 0.1 watt.

Technical Disclosure
Problem - Motivation that led to development or problem that was solved.

Turbo code is a key functional block of advanced communication systems. Due to its high computation complexity, turbo code implementation in software is too slow to meet high throughput requirements. Meanwhile, turbo code in ASIC is not flexible to integrate with other functional blocks of advanced communication system.

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New Technology Reporting Form

Solution

An advanced communication system based on turbo code has been proposed by using system-on-a-chip technology. It can meet high throughput, low power, light weight, small size, and high performance requirements.

The turbo code is the key functional core of the proposed communication system-on-a-chip design. A high-throughput, low-power, parameterizable turbo decoder core has been developed for this advanced communication system-on-chip design. Because this turbo decoder core is parameterizable and can be modified easily to fit any size for advanced communication system-on-chip products such as such as satellite communications, wireless LAN, digital TV, cable modem, Digital Video Broadcast (DVB), and xDSL systems.

Description

See the attached technical paper.

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