

# Open-Systems Architecture of a Standardized Command Interface Chip-Set for Switching and Control of a Spacecraft Power Bus

B. Ian Ruiz\*  
Gary R. Burke†  
Gerald Lung‡  
William D Whitaker§

*Jet Propulsion Laboratory; 4800 Oak Grove Drive, Pasadena, CA, 91101*

Robert M. Nowicki\*\*  
*ACRO Service Corporation; 4800 Oak Grove Drive, Pasadena, CA, 91101*

The Jet Propulsion Laboratory (JPL) has developed a command interface chip-set that primarily consists of two mixed-signal ASICs; the Command Interface ASIC (CIA) and Analog Interface ASIC (AIA). The Open-systems architecture employed during the design of this chip-set enables its use as both an intelligent gateway between the system's flight computer and the control, actuation, and activation of the spacecraft's loads, valves, and pyrotechnics respectively as well as the regulator of the spacecraft power bus. Furthermore, the architecture is highly adaptable and employed fault-tolerant design methods enabling a host of other mission uses including reliable remote data collection. The objective of this design is to both provide a needed flight component that meets the stringent environmental requirements of current deep space missions and to add a new element to a growing library that can be used as a standard building block for future missions to the outer planets.

## Nomenclature

<i>AIA</i>	=	Analog Interface ASIC
<i>ADC</i>	=	Analog to Digital Converter
<i>ASIC</i>	=	Application Specific Integrated Circuit
<i>CIA</i>	=	Command Interface ASIC
<i>DSA</i>	=	Deep Space Avionics
<i>EEPROM</i>	=	Electrically Erasable Programmable Read Only Memory
<i>HCD</i>	=	Hardware Command Decoder
<i>I<sup>2</sup>C</i>	=	Inter-Integrated Circuit
<i>I/O</i>	=	<i>Input/Output</i>
<i>IRAM</i>	=	Internal Random Access Memory
<i>JTAG</i>	=	Joint Test Action Group
<i>kB</i>	=	kilobyte
<i>MUX</i>	=	multiplexor
<i>POR</i>	=	Power on Reset
<i>RX</i>	=	Receive
<i>TLM</i>	=	<i>Telemetry</i>
<i>TX</i>	=	Transmit
<i>XRAM</i>	=	External Random Access Memory

\* CIA-AIA Cognizant Engineer, Avionics Systems Engineering Section, M/S: 198-138, AIAA Non-Member

† CIA Digital Design Lead, Avionics Equipment Section, M/S: 198-235, AIAA Non-Member

‡ CIA Analog Design Lead, Avionics Equipment Section, M/S: 198-326, AIAA Non-Member

§ AIA Design Lead, Avionics Equipment Section, M/S: 198-138, AIAA Non-Member

\*\* Firmware Design Lead, Space Science Data Systems Section, M/S: 171-264, AIAA Non-Member

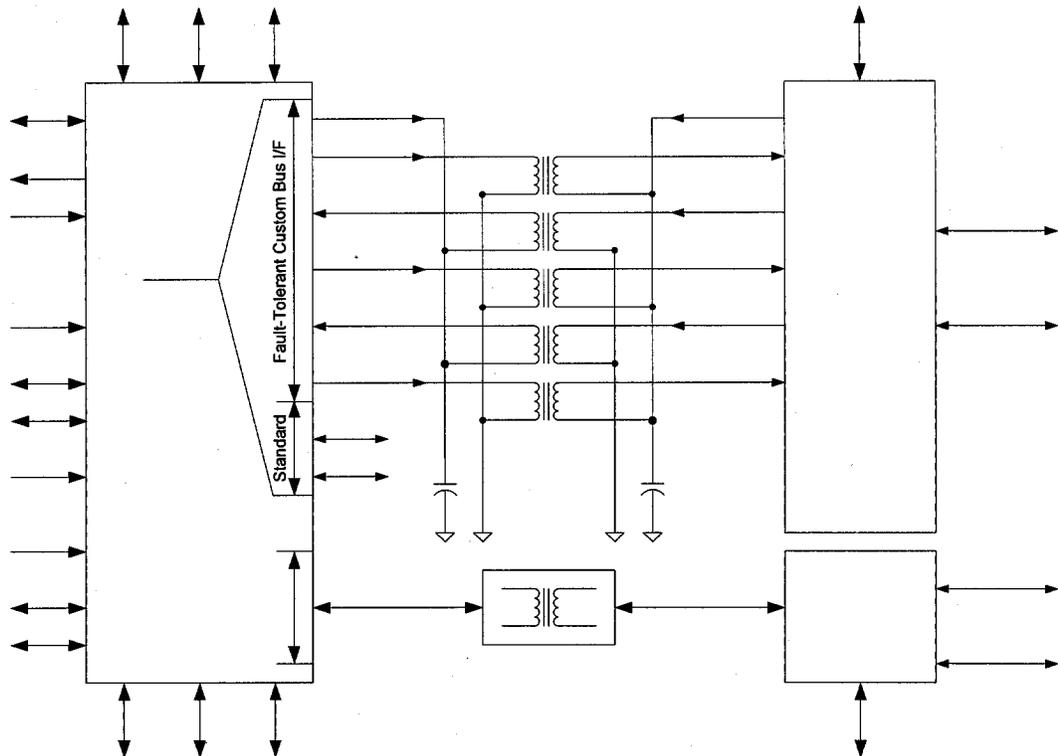
## I. Introduction

The Command Interface ASIC (CIA) – Analog Interface ASIC (AIA) chip-set is comprised primarily of two mixed signal ASICs, both of which have been developed and fabricated by the Jet Propulsion Laboratory (JPL). The CIA is currently undergoing both process and functional testing at Honeywell’s Solid State Electronics Center (SSEC) and JPL respectfully. The AIA has already been fully verified. This chip-set provides for the construction of a reliable radiation hardened electrically isolated multi-drop multi-master bus interface to a re-configurable control and data collection “building block” that can be used to regulate the power bus, actuate valves, fire pyrotechnics, and provide switchable power to the spacecraft loads. Furthermore, the open-systems architecture provides for a host of other mission uses such as remote data collection and instrument interface.

The CIA employs both gate-array and custom technologies. The gate-array portion of the ASIC contains a message processor which utilizes a microcontroller core executing embedded code, fault-protection and timing circuitry, multiple instantiations of discrete input/output signals capable of deterministic switching, and a hardware command decoder (HCD). The custom portion of the ASIC contains a means to cross-strap the required input power, thus allowing for power supply failures, power-on-reset circuitry based on the resultant cross-strapped power, an analog-to-digital converter (ADC), current and voltage conditioning circuitry enabling the chip to measure a spacecraft power bus, fault-protection circuitry, and a redundant transformer isolated bus interface to an AIA.

The AIA is a custom ASIC designed to provide ground isolation for one of the two redundant bus interfaces to the CIA. In addition, the AIA enables CIA based bus fault-protection features and makes longer bus lengths possible enabling spacecraft wide bus routing.

Figure 1 depicts a top-level diagram of the CIA-AIA chip-set.



**Figure 1. CIA-AIA Chip-Set Top-Level Block Diagram**

## II. Command Interface ASIC (CIA) Architecture

The Command Interface ASIC is a mixed-signal radiation-hard system-on-a-chip designed for high reliability applications. The CIA can be powered by redundant DC power supplies and is commanded via redundant standard commercial or custom I<sup>2</sup>C busses. As previously mentioned the CIA utilizes both gate-array and custom technologies. Furthermore, each of these two portions of the ASIC contains multiple functions. Figure 2 depicts these functions.

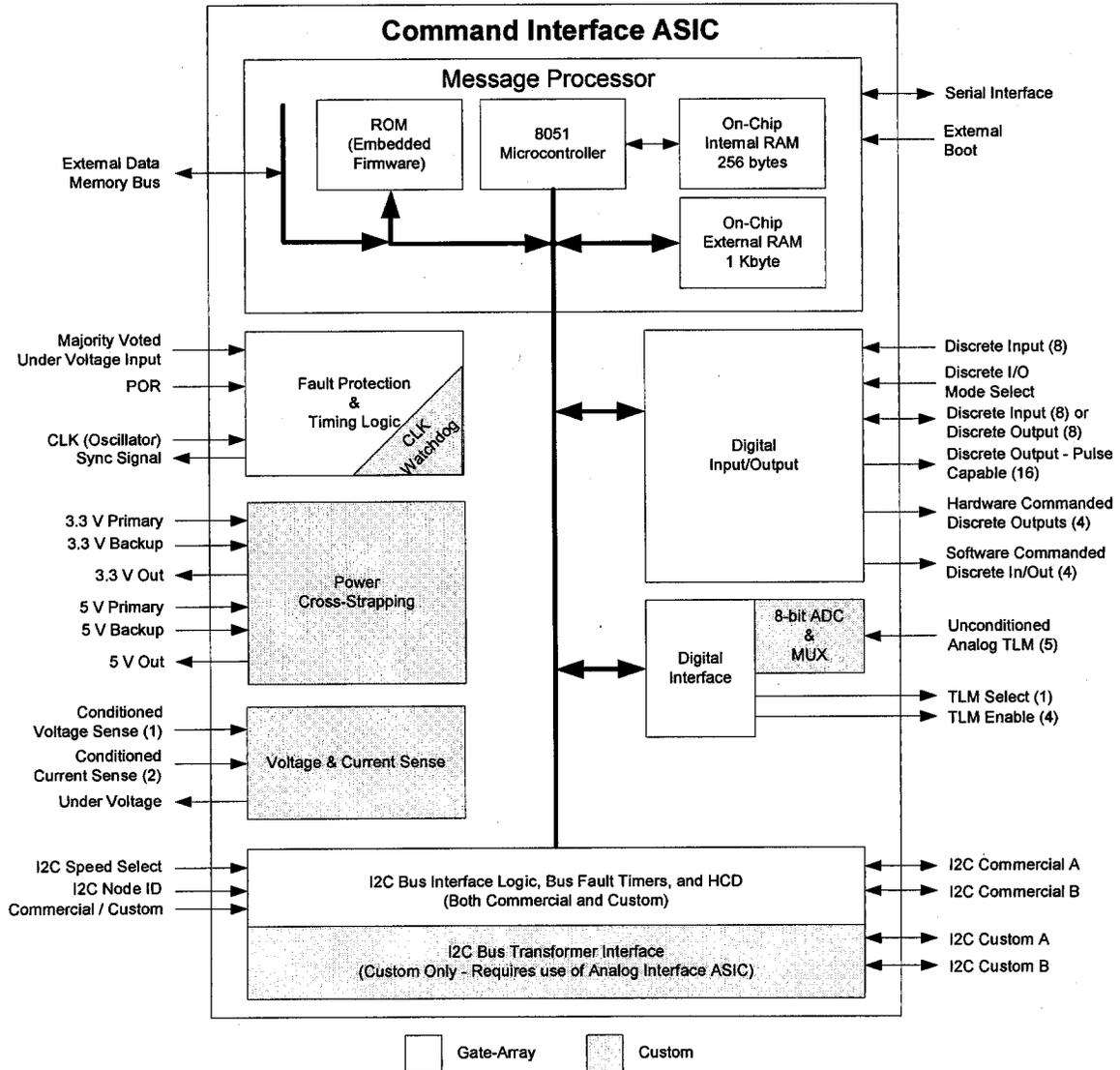


Figure 2. CIA Block Diagram

### Gate-Array Elements

The functions contained within the digital portion of the ASIC are the message processor, a collection of fault-protection and timing logic, discrete input/output signals, a digital interface to the embedded ADC, a collection of digital test circuitry, and both standard and custom bus interface logic.

#### 1. Message Processor

The message processor is composed of an 8051 microcontroller core. This core executes a command every 2-clock cycles vs. the nominal 8051 microcontroller that processes a command every 12-clock cycles. Furthermore, the message processor includes an on-chip ROM that contains embedded firmware for a power switching

application, 256 bytes of internal RAM, and 1kB of on-chip external RAM (XRAM). The internal RAM (IRAM) is connected to the 8051 via the internal data memory bus and is used as a scratch pad for the firmware. The ROM and 1kB of external RAM are connected to the 8051 via the external data memory bus, which is also accessible off-chip. A single pin can be used to communicate the location of the boot code (internal or external). This ability allows the CIA to execute code developed post production, thus enabling the use of the CIA in a multitude of other applications including remote data collection, instrument interface, and provided a highly reliable, radiation-hard EEPROM is used in-flight reprogram ability is possible. The message processor also provides a simple serial port (RX/TX), which is available as a firmware debugging tool, but could serve as an additional interface.

## 2. *Embedded Firmware*

The embedded firmware enables the use of the CIA-AIA chip-set as part of a power switching function developed by JPL for outer planets missions. Fundamentally, the embedded firmware provides a reliable startup, switch command and telemetry request receipt and verification, command execution, telemetry gathering, and periodic health monitoring. Two sections of code are used to provide these functions; the startup code, which is written in assembler, and the main processing loop, which is written in C.

Upon being reset by any number of external resets the assembly language startup code begins execution. It's function is to perform a ROM checksum over the entire ROM program space, pattern test internal registers and internal RAM (IRAM), and also pattern test the XRAM (both on and off-chip if any is present) leaving any required "save data" memory in place. The stack is assigned its final location and the assembly language code transitions to the main processing loop.

The main processing loop checks hardware status bits to differentiate between cold and warm boots, and proceeds accordingly. Interrupts are enabled and then the main processing loop is entered. The main processing loop is used to check for the arrival of both switch and telemetry request commands over the I2C bus, allow for processing of both established interrupts (I2C and 1.6 ms), and perform ongoing checksumming of the ROM code to insure it's integrity.

The I2C interrupt routines (one for each I2C bus) are used to collect incoming data bytes and form them into commands that are then passed up to the main line routine to process. The I2C interrupt routines are also used to load telemetry packets into the I2C hardware buffer when the CIA is running in transmit mode to pass previously collected telemetry to the bus master. All I2C interrupts result in the transfer or receipt of no more than 1 byte of data and/or status at a time.

The 1.6 ms interrupt routine is generated by the CIA timing logic and is used to perform the actual turning on/off of switches as specified in the received switch commands. This interrupt is also used in the processing of timed switch commands to identify if the time has arrived to initiate the pulsing of a given switch.

The flowchart in fig. 3 depicts the above-described firmware operation.

## 3. *Fault Protection and Timing Logic*

The Fault protection logic is responsible for responding to fault conditions by initiating either a "Hard Reset" or a "Warmboot" event. A hard reset is defined by all logic being set to an initial default state, all internal RAMs validated and initialized, and all registers cleared with the exception of one indicating the cause of the "Hard Reset". In addition, a hard reset will set all loads to their power-on-reset (POR) default state, which is determined via external hardware pins and has a load-shedding effect on the spacecraft. A warmboot is defined by a reset of the message processor, which does clear and initialize all internal RAMs, but does not change the current state of the switches, as this information is maintained in the "save data" area.

The 8051-watch-dog timer is part of the timing logic, is enabled during the boot-up process of the CIA, and must be reset every 1.6 ms by the 8051 embedded microcontroller. In the event of timer expiration a warmboot is initiated. In addition, this timer is disabled upon entering low power mode, which is a mode of operation that disallows most commanding (all except those that can be decoded and executed by the HCD) and all autonomous functions performed by the CIA in an effort to conserve power. The purpose of the 8051 watch-dog timer is to assure that the firmware is executing properly.



and enable signals allowing the user to significantly increase the number of analog channels monitored by making use of the five available unconditioned ADC inputs.

#### 6. I2C Bus Interface Logic and Bus Fault Timers

The I2C bus interface logic provides an interface between the 8051's 8-bit external data memory bus and a redundant set of 100kHz I2C buses, which can be accessed either directly or via a customized transformer interface. If accessed directly the user must adhere to the Philips Semiconductors I2C specification, which was intended for local communications, thus the line lengths should not exceed 2 meters and the sink capability of the drive transistors should not be expected to be greater than 3 mA. If accessed via the customized transformer interface the user must use an Analog Interface ASIC (AIA) per bus and adhere to the connection scheme and performance limits dictated by the AIA.

The I2C bus interface logic consists of two I2C intellectual property (IP) cores as well as additional fault tolerant logic. The fault tolerant logic consists of an auto turn-on timer and a fail-silent timer per bus. Both the auto turn-on timer and the two fail silent timers have 4 pre-determined programmable values.

**Table 1. Auto-Turn-On and Fail-Silent Timer Default Values.**

Auto-Turn-On Timer	Fail-Silent Timer 1 (Bus A)	Fail-Silent Timer 2 (Bus B)
30 seconds	1 second	1 second
<b>60 seconds</b>	<b>3 seconds</b>	<b>3 seconds</b>
2 minutes	7 seconds	7 seconds

The default values for each of the fault timers are bold in table 1. Upon expiration of the auto-turn-on timer the CIA will initiate a hard reset, which will return the switches to their POR default state. Upon expiration of the fail-silent timer the CIA disables (mutes) its transmission capability on the I2C bus connected to that timer, thus preventing bus babbling.

#### Custom Design Elements

The custom area of the CIA contains a means to cross-strap the required input power, power-on-reset circuitry feed from the resultant cross-strapped power, an analog-to-digital converter (ADC), current and voltage conditioning circuitry enabling the chip to measure a spacecraft power bus, fault-protection circuitry, and a redundant transformer isolated bus interface to an AIA.

##### 1. Power Cross-Strap

The CIA is capable of cross-strapping both power sources required (3.3V and 5V). The 3.3V supply is used to power the digital logic and a small portion of analog circuitry, and the 5V supply is used to provide power to the majority of the analog circuitry. Figure 4 depicts a very simplistic version of the cross-strapping method used within the CIA.

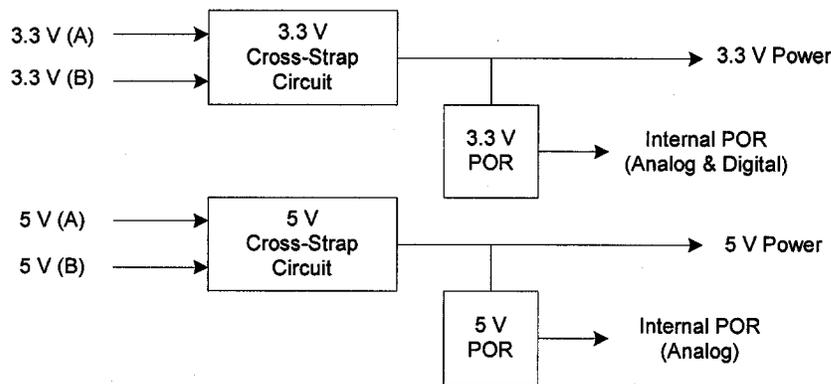
By default the cross-strapping circuit will always draw power from the "A" supply for the 5V version and from the "B" supply in the 3.3V version. In the event of an input power supply failure the circuit will switch to drawing power from the alternate source until it fails or until a hard reset takes place. Simulations have demonstrated a possible load sharing between the (A) and (B) supplies of for both the 3.3V and 5V cross-strap circuits when the input voltages are a small amount apart. As expected, this effect originates from the reduced input drive voltage available and is much more pronounced in the 3.3V cross-strap because of the reduced gate drive voltage.

##### 2. Power-On-Reset

Rather than monitoring the POR signals from the appropriate converters the CIA utilizes two power-on reset circuits as identified in fig. 4, one monitoring the +5v bus and one monitoring the +3.3v bus. When a rising edge surpassing either circuit's threshold is detected, a POR signal is issued. A POR signal is also issued upon detecting an under-voltage condition. The CIA will perform a "Hard Reset" based on the issuance of a 3.3V POR, but not the 5V POR as only the 3.3V POR is monitored by the gate-array portion of the ASIC.

##### 3. Analog to Digital Converter

The CIA contains an embedded 8-bit successive approximation analog-to-digital converter (ADC) with an 8-channel analog input voltage multiplexer. Although designed as a 5V circuit, the ADC has been customized within the CIA to accept 3.3V logic levels hence facilitating communication with the CIA 3.3V-based digital circuitry. This IP, obtained from Honeywell SSEC is considered confidential and proprietary.



**Figure 4. CIA Power Cross-Strapping.**

#### 4. Current and Voltage Conditioning Circuitry

The function of the current monitor circuits is to measure the charge and discharge current of a 22-36V power bus employed by the power system within a spacecraft. The CIA is equipped with two current monitor circuits configured to monitor the current passing through an off-chip sense resistor of 10

milliohms. Capable of measuring sense currents from 0A to 12A, the outputs from these two circuits are connected to two of the eight ADC inputs internal to the CIA.

Voltage monitoring of the external power bus and under voltage detection is performed by the CIA's Voltage Monitor/Under Voltage (UV) circuit. An off-chip resistor divider network translates the bus voltage range of 0V to 36V down to 0V to 2V and then drives the UV-monitor amplifier. Similar to the current monitor circuit, the amplifier output is connected to one of the eight ADC inputs internal to the ASIC. Under voltage detection is achieved by comparing the analog signal against a pre-set threshold thus determining whether or not an under voltage event has occurred. If detected, a digital signal is issued and delayed via an off-chip capacitor before it is forwarded to the CIA digital electronics.

#### 5. Fault-Protection Circuitry

The clock watchdog circuit monitors the 33MHz signal from the on-board crystal by sampling a quarter scale of the host 33MHz clock sent from the gate-array portion of the design to the watchdog circuit. Upon clock failure detection, the CIA holds the embedded microcontroller in reset and immediately asserts a default state set with hardware pins on the 16 software commanded discrete outputs hence eliminating the possibility of leaving a discrete output latched in an undesired state due to the loss of clock.

#### 6. Redundant Transformer Isolated Bus Interface to an AIA

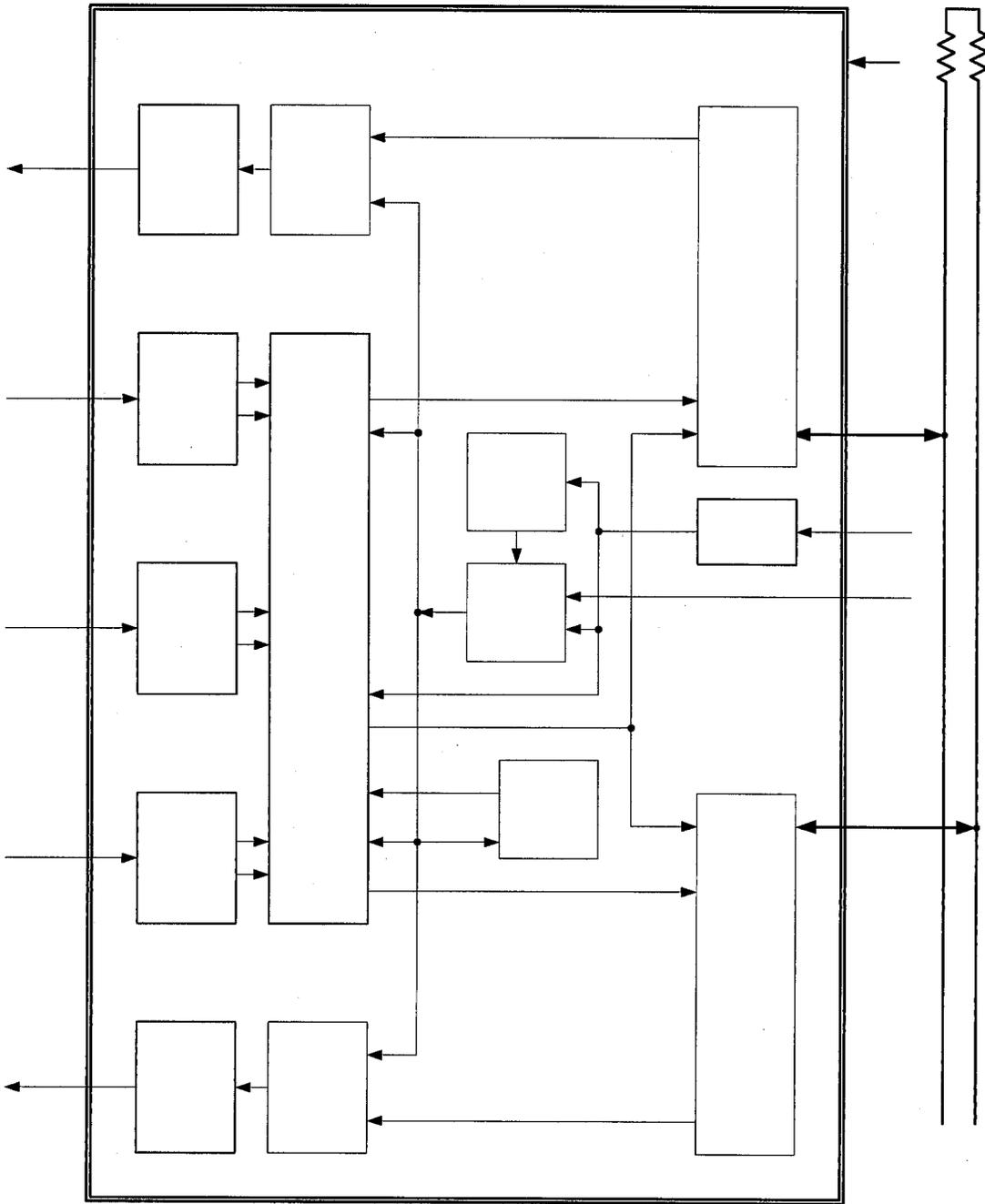
The analog portion of the CIA contains a pair of I2C receivers and transmitters, used in the AIA. The purpose of these receivers and transmitters is to allow for the connection of a proprietary transformer interface between the CIA and the AIA. The use of the AIA on each bus provides for slew rate control and a much larger sink capability than what the Phillips I2C specification calls out (30 mA vs. 3 mA).

### III. Analog Interface ASIC Architecture

The AIA is a custom ASIC designed to provide ground isolation for one of the two redundant bus interfaces to the CIA. In addition, the AIA enables CIA based bus fault-protection features, specifically fail-silent, and makes longer bus lengths possible enabling spacecraft wide bus routing. Figure 5 depicts the functional elements of the AIA.

#### A. I2C Bus Interface

There are two identical transceivers within the AIA ASIC that connect the AIA to the I2C data and clock buses. The transmitter portion is active pull-down, can sink 30 mA's, and is slew rate controlled. I2C bus pull-up resistors are located external to the AIA and are must be provided by the system. The fail-silent circuitry disconnects the AIA from the bus should either transistor fail in the on state. The receiver portion of the transceiver is a buffer that converts the slower slew rate I2C signals into digital level signals that are compatible with the AIA electronics.



**Figure 5. AIA Top-Level Block Diagram**

**B. I2C Transformer Interface**

Transformers are used to provide I2C and discrete signal isolation between the CIA and AIA. All the electronics to support the transformer interfaces will be contained in the two ASIC's. The CIA and AIA share I2C clock, I2C data, and a connect signal (heartbeat from CIA) across this interface. The clock and data interfaces each consist of 2 signals, one for CIA to AIA transfers, and the other for AIA to CIA transfers. The AIA clock and data transmitters (TX) provide I2C information to the CIA: a series of pulses for an asserted (LOW) on the I2C bus, and a steady 0 Volts for a de-asserted (HIGH) bus line. The AIA clock and data receivers (RX) require the CIA to maintain a pulse train across the interface for the AIA to drive the I2C bus to an asserted state (LOW). The connect signal from the CIA controls the pull-down transistor in the AIA I2C driver. The CIA must maintain a pulse train

across the connect interface for the AIA to enable the pull-down transistor, thereby allowing the AIA to drive the I2C bus.

### **C. Power-On-Reset Circuitry**

An active low power on reset (POR) pulse is supplied to the AIA from a power converter. The POR block within the AIA shall perform buffering and inverting of the input signal as is needed within the AIA. The buffered reset shall create the sequenced resets used by the Oscillator and the Oscillator Watchdog circuitry.

### **D. Fail-Silent**

Upon POR the fail-silent circuitry disables the fail-silent transistor in both the I2C clock and data transceiver transmitters so the I2C buses cannot be pulled to ground. Once the oscillator becomes active, and the POR input to the AIA is released, the fail-silent circuitry will allow the CIA full access to the I2C bus. If an oscillator failure is detected, the fail-silent logic de-asserts (HIGH) the outputs to the I2C bus, and disables the fail-silent transistors.

### **E. Internal Oscillator & Support Circuitry**

The AIA has a non-chip free-running oscillator or the user can supply an external oscillator. The oscillator control logic provides all the necessary divisions of the input frequency, performs the selection between the internal or external clock source, and converts the watchdog output to a logic flag, which is used to indicate an oscillator failure has occurred. In light of an oscillator failure, this circuit keeps the AIA in the fail-silent mode until the AIA receives a POR from the converter.

The watchdog monitors the AIA core clock for stuck-high or stuck-low failures. The watchdog monitors either the internal oscillator or the external oscillator depending on which is selected. The watchdog reports the failure of the oscillator after a timeout period expires. The failure is reported until the clock transitions resume, which returns the watchdog to the monitoring state.

## **IV. Applications**

JPL's Deep Space Avionics (DSA), formerly X2000, developed the CIA-AIA chip-set to fulfill two needs.

- 1) A single solution for the switching of loads, the actuation of valves, and the activation of pyrotechnics.
- 2) The regulation of the spacecraft power bus.

### **A. Switches, Valves, and Pyrotechnics**

The CIA-AIA chip-set with the embedded firmware provides for the switching of loads, the actuation of valves, and the activation of pyrotechnics. The switching of generic spacecraft loads is easily accomplished by issuing an I<sup>2</sup>C command that makes use of any of the previously described discrete outputs.

The actuation of valves such as attitude adjustment and the main engine require the use of the software commanded discrete outputs as they provide for a deterministic start and pulse duration. Furthermore, they provide for a hardware mechanism that locks out the ability to inadvertently issue a steady-state "on" to a valve.

Similar to valves the activation of pyrotechnics can be accomplished by making use of the software commanded discrete outputs. These outputs are used rather than outputs that can latch to a state for safety reasons.

It is important to note that the CIA-AIA chip-set serves as an intelligent gateway between the flight computer and another chip-set which actually connects to the high powered switch. In other words, the outputs of the CIA are digital discrete lines that range from 0 to 3.3V. The actual switch used to control power to the generic loads, valves, and pyrotechnics requires a high voltage interface which is provided by the Switch Control ASIC (SCA) chip-set, which has also been developed by JPL's DSA project. When used together these two chip-sets provide a full and robust solution.

### **B. Spacecraft Power Bus Regulation**

DSA developed preliminary firmware that would implement both a voltage as well as a current control loop in order to regulate the spacecraft power bus. This algorithm was coded in C and placed in an external PROM attached to the CIA, thus making use of the CIA-AIA chip-set in another application. The built-in conditioning circuitry attached to three of the eight ADC inputs provided a means for measuring the battery bus voltage, the charge current, and the discharge current on the spacecraft batteries. The power bus regulation firmware was executed on a prototype development in order to verify a software model, which was successful. Further testing will require a custom board with an AIA-CIA chip-set.

### C. Other Applications

Access to the external data memory bus allows for the addition of an external PROM, additional RAM, or additional memory-mapped I/O. The external data memory bus will allow for the addition of a 32kB external ROM, PROM, or EEPROM to hold code for the embedded microcontroller. As a point of reference the embedded code consumes less than 8kB. The embedded microcontroller can address up to 64 kB of external data memory or other memory mapped I/O. Thus, the addition of a 32kB external ROM and the 1kB of external RAM that is embedded in the ASIC allows for the further addition of up to 31kB of addressable memory.

Other missions at JPL have examined using the CIA-AIA chip-set as the front-end interface for other non-power instrumentation as well as remote engineering units, which function as a node typically remote to the avionics chassis that collects engineering telemetry.

### V. Conclusion

The CIA-AIA chip-set provides a reliable and robust solution for the switching of loads, actuation of valves, and activation of pyrotechnics. Furthermore, this chip-set was developed and designed to function as the spacecraft's means to regulate the power bus. In addition, the fault-tolerant open systems architecture of this chip-set enables a multitude of other mission uses. The CIA-AIA chip-set provides the following capabilities:

- 1) 1KB of on-chip RAM.
  - 2) Interface via two redundant Fault-tolerant I2C busses.
  - 3) On-chip 8-bit Analog-to-Digital converter.
  - 4) Fault-Tolerant Boot-Up Sequence in embedded micro-code.
  - 5) Continuous Health Checks in micro-code.
  - 6) Perform intelligent data sequencing and buffering tasks using an embedded 8051 microcontroller.
  - 7) Capable of accepting power from two redundant power sources.
  - 8) Capable of Addressing up to 64 KB (1KB on-ship) of external RAM or other memory mapped I/O.
  - 9) Capable of booting the embedded 8051 microcontroller from an external PROM.
- As a product the CIA-AIA chip-set can enable more rapid development for deep space avionics.

### Acknowledgments

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