Single-Event Upset in Highly Scaled Commercial Silicon-on-Insulator PowerPC Microprocessors

F. Irom and F. H. Farmanesh

***Abstract*—Single-event upset effects from heavy ions are measured for Motorola and IBM silicon-on-insulator (SOI) microprocessors with different feature sizes and core voltages. The results are compared with results for similar devices with bulk substrates. The cross sections of the SOI processors are lower than their bulk counterparts, but the threshold is about the same, even though the charge collections depth is more than an order of magnitude smaller in the SOI devices. The scaling of the cross section with reduction of feature size and core voltage dependence for SOI microprocessors is discussed.**

***Index Terms*—Cyclotron, heavy ion, microprocessors, silicon-on-insulator (SOI).**

I. Introduction

SINGLE-EVENT effects can be a significant problem for devices operating in space, particularly for microprocessors because of their complexity. Radiation tests are often required in order to allow estimates of upset rates caused by space radiation. The test results help to determine what kinds of effects are produced and how they can be detected and overcome.

In recent years there has been increased interest in the possible use of unhardened commercial microprocessors in space because they operate at higher speed, and have superior electrical performance compared to hardened processors. However, unhardened devices are susceptible to upset and degradation from radiation and more information is needed on how they respond to radiation before they can be used in space. Only a limited number of advanced microprocessors have been subjected to radiation tests, and the majorities have been older device types which are designed with much larger feature sizes and higher operating voltages than modern devices [1]–[7].

A basic method for improving the SEU immunity without degrading the performance is to reduce the SEU-sensitive volume. This can be accomplished through the use of silicon-on-insulator (SOI) substrates. For SOI processes the charge collection depth for normally incident ions is reduced by more than an order of magnitude compared to similar processes fabricated on epitaxial substrate. Because of the much smaller charge collection depth, the single-event upset (SEU) sensitivity of SOI devices is expected to be much better. However, other factors, such as lower operating voltages, reduced junction capacitance and amplification by parasitic bipolar transistors [8] may limit the degree of improvement in SEU sensitivity that can be obtained with commercial SOI processors. An early study of charge collection by Massengill, *et al.* [9], as well as more recent work on the sensitivity of SOI structures with no body ties to neutrons and alpha particles [10], [11] have shown that charge multiplication by the parasitic bipolar structure increases the collected charge by as much as a factor of ten compared to charge deposited by the primary particle interaction.

Commercial microprocessors with the PowerPC architecture are now available that use partially depleted SOI processes to improve performance. This paper examines SEU effects in advanced SOI processors from two manufacturers, comparing the results with advanced processors that use conventional isolation methods from each manufacturer. Results are presented for SOI processors with feature sizes of 0.18 and 0.13 μm.

II. Device Descriptions

The PowerPC 750 was co-designed by IBM and Motorola. It is a 64-bit processor that has evolved into improved versions (with different numerical designations) during the last five years, taking advantage of manufacturing improvements that have allowed the feature size and internal operating voltage to be reduced, as well as an increase in the overall functionality. We previously reported SEU measurements on earlier generation PowerPC 750 microprocessors from both manufacturers [1].

Commercial manufacturers have shown interest in using SOI technology for fabricating low-power, high-performance microprocessors. The Motorola PowerPC 7455 and IBM PowerPC 750FX are the first generation of the PowerPC family, which are fabricated with SOI technology. They are partially depleted and no body ties. The Motorola device has a feature size of 0.18 μm with a silicon film thickness of 110 nm and internal core voltage of 1.6 V. A low power version of this processor operates with internal core voltage of 1.3 V. The IBM part is fabricated with a more scaled process, using a feature size of 0.13 μm, silicon film thickness of 117 nm and core voltage of 1.4 V [12]. Both devices are packaged with "bump bonding" in flip-chip ball-grid array (BGA) packages. Recently, a more advanced version from Motorola, with a feature size of 0.13 μm, silicon film thickness of 55 nm and internal core voltage of 1.3 V, has been announced. SEU measurements with this device provide a direct comparison of the effects of scaling and process changes for current SOI processes with regard to radiation hardness for devices from a single manufacturer.

Table I summarizes the recent SOI generation of the PowerPC family. The feature size is reduced from 0.18 to 0.13 μm,

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The authors are with the Jet Population Laboratory, California Institute of technology Pasadena, CA 91109 USA (e-mail: farokh.irom@jpl.nasa.gov; farhad.f.farmanesh@jpl.nasa.gov).

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TABLE I
COMPARISON OF MOTOROLA AND IBM SOI POWERPC FAMILY OF ADVANCED PROCESSORS

Device	Feature Size (µm)	Die Size (mm^2)	Film Thickness (nm)	Core Voltage (V)
Motorola 7455	0.18	106	110	1.6
Motorola 7455*	0.18	106	110	1.3
Motorola 7457	0.13	98	55	1.3
IBM 750FX	0.13	34	117	1.4

* This is a special low power version of the Motorola SOI PowerPC 7455.

TABLE II
LIST OF THE ION BEAMS USED IN OUR MEASUREMENTS (RANGE AND LET ARE IN SI)

Ion	Energy per Nucleon (MeV/amu)	LET (MeV-cm^2/mg)	Range (µm)
^{20}Ne	40	1.2	1648
^{40}Ar	40	3.8	1070
^{78}Kr	40	14.2	601
^{20}Ne	25	1.7	790
^{40}Ar	25	5.4	491

with core voltage reduced from 1.6 to 1.3 V. The die size ranges from 34 to 106 mm^2, and transistors count ranges from 33 to 58 million.

III. EXPERIMENTAL METHODS

Radiation testing was performed at the Texas A&M accelerator. All irradiations were done using ions with normal incidence. This facility produces the long-range ions needed for SEU testing through thick materials. Particularly, the 25 and 40 MeV/amu beams are quite penetrating, and it is possible to do irradiations in the air rather than in vacuum. Undegraded Ion beam used in our measurements were listed in Table II.

The total thickness of the die for SOI PowerPCs is about 850 μm and the limited range of heavy-ion beams does not allow them to penetrate the package, except for ions with lower LET. The "flip-chip" design of the SOI PowerPCs does not allow the device to be "delidded" without destroying pad and bonding connections. In order to get around the delidding problem, the back surface of the PowerPCs was ground with a precision high-speed diamond grinding machine. This reduced the total thickness of the die for the Motorola 7455 processor from about 850 to 230 μm, which is thin enough to allow adequate penetration of the die using back irradiation with the high-energy ions available at the accelerator. The thinning process did not change any observed electrical parameters of the processor. The IBM processor, Motorola 7457 and low power version of Motorola 7455 were tested without thinning. This limits useable ions (see Table II) to those with a range greater than 850 μm, i.e., only the 40 MeV/amu Ne and Ar. Thus, the highest LET is limited to about 16 MeV-cm^2/mg. Corrections to the LET were made to account for energy loss of the ions when they traverse the back layer to the thin epitaxial region at the surface. This approach was used in earlier tests of the PowerPC 750, and there was good agreement for SEU results obtained from thin and unthinned PowerPC processors, after correcting for energy loss through the thinned substrate.

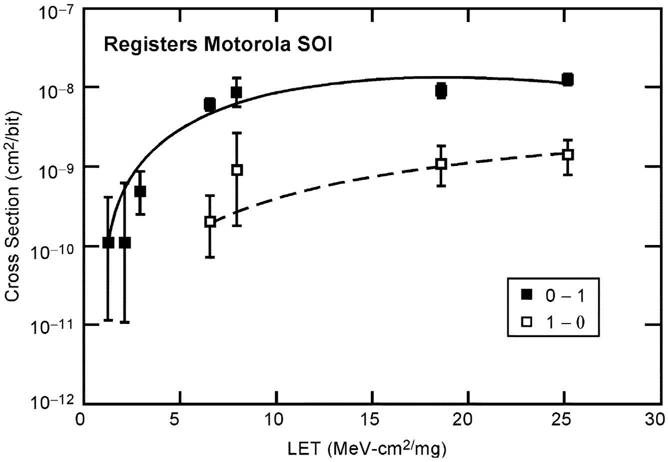

Fig. 1. Heavy-ion cross sections for registers $(\mathrm{FPR} + \mathrm{GPR} + \mathrm{SPR})$ of the Motorola SOI Powerpc 7455 for "1" to "0" and "0" to "1" upsets. The dashed and solid curves are only guides for the eye.

The test methodologies used to measure the upsets errors in the registers and D-cache are described in [1], [13], and [14] in detail. Tests were performed on two to three parts for each processor type.

In testing the register, the processor performs a one-word instruction infinite loop interrupted briefly every half-second to write a register snapshot to a strip chart in the physical memory. After the irradiation has ended, an external interrupt triggered a reporting routine to download the strip chart and compared the register contents with the pattern initially loaded, and counted state changes in the register.

A more complex method was required to examine errors in the L1 cache. Upsets in the cache were counted with special post beam software. The cache was initialized under specified conditions prior to irradiation and then disabled. Then a clearly recognizable pattern, designed to be distinctly different from contents of the cache, was placed in the external memory space covered by the cache. Comparing the cache contents after irradiation provided verification of the cache contents. Tag upsets, as well as upsets of the data valid flag, were detected by monitoring the distinctly different pattern. The tag and data valid upsets were thus distinguished and counted separately from upsets of the data bits themselves.

IV. TEST RESULTS

A. Register Tests

Motorola Processors: Fig. 1 displays results of cross section measurements for the Motorola SOI PowerPCs 7455 (feature size 0.18 μm) registers [sum of Floating Point Registers (FPR), General Purpose Registers (GPR), and Special Purpose Registers (SPR)] for "0" to "1" and "1" to "0" transitions. Note the pronounced asymmetry in the response. There is no SEU for "1" to "0" transitions up to LET of 6 MeV-cm^2/mg. The cross sections for the two logic directions are also different.

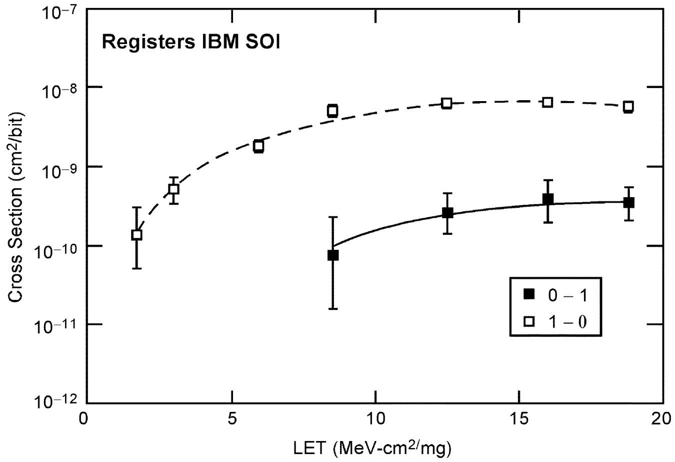

Fig. 2. Heavy-ion SEU cross section for the registers $(\mathrm{FPR}+\mathrm{GPR}+\mathrm{SPR})$ of the IBM750FX SOI PowerPC for "1" to "0" and "0" to "1" upsets. The dashed and solid curves are only guides for the eye.

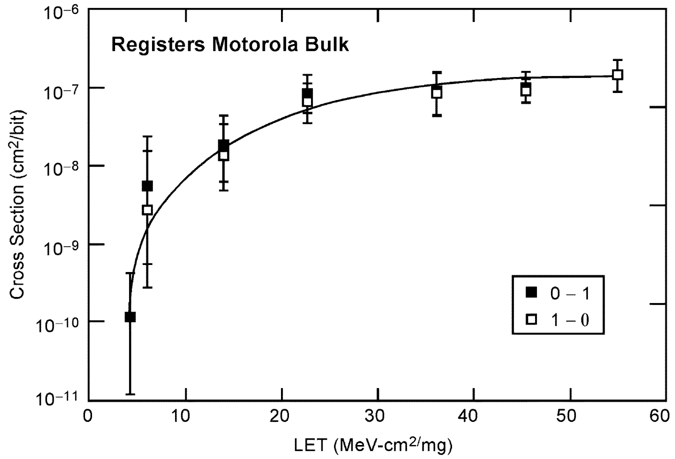

Fig. 3. Heavy-ion SEU cross section for the registers $(\mathrm{FPR}+\mathrm{GPR}+\mathrm{SPR})$ of the motorola PowerPC 7400 for "1" to "0" and "0" to "1." The solid curve is only guides for the eye.

We repeated SEU measurements on a special version of Motorola PowerPC 7455 that operates with a lower internal core voltage specification of 1.3 V. The asymmetry in registers was more pronounced.

Recently, we measured SEU on a new advanced version of the SOI processor from Motorola, the PowerPC 7457. This processor has a feature size of 0.13 μm and internal core voltage of 1.3 V. Similar asymmetry was observed for this processor.

IBM Processors: A similar asymmetry was observed between "0" to "1" and "1" to "0" upsets for the IBM SOI PowerPC registers $(\mathrm{FPR}+\mathrm{GPR}+\mathrm{SPR})$, although the asymmetry was reversed (worst for "1" to "0" upsets) compared to results for the SOI processor from Motorola. Fig. 2 shows the results. The saturated cross section for "1" to "0" upsets is 7×10^{-9} cm^2/bit. It is interesting to note that asymmetry was barely evident in register tests of the Motorola PowerPC 7400 processor, which has a bulk substrate, as shown in Fig. 3. The same test approach was used for both types of processors. The saturated cross section of the SOI processor is about 10^{-8}cm^2/bit, which is about an order of magnitude lower than that of CMOS epi PowerPC 7400, whose feature size is nearly the same as that of the 7455 SOI version. Similar differences in cross section between SOI and bulk technology devices were reported in [15] and [16].

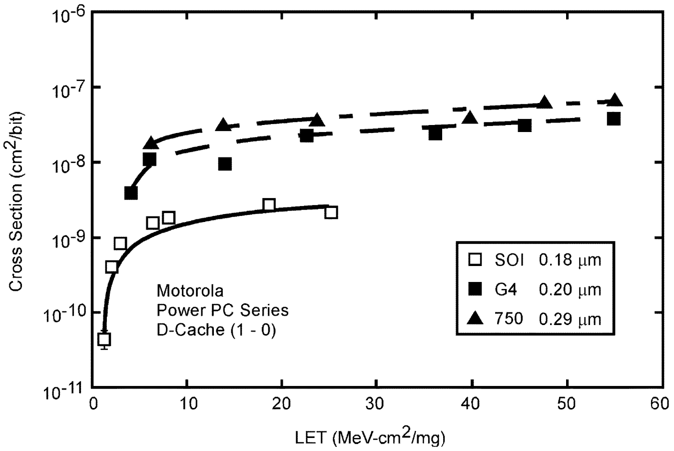

Fig. 4. Comparison of the heavy-ion SEU cross section for the data cache bits transitions from "1" to "0" of the motorola SOI PowerPC to those of the PowerPC 750 and 7400 (G4). The dashed and solid curves are only guides for the eye.

B. Cache Tests

Fig. 4 displays results of cross section measurements for the Motorola SOI PowerPC D-Cache for "0" to "1" transitions along with results for the two bulk processors. Even though the G4 processor has a much smaller feature size than the PowerPC 750 (as well as lower core voltage), the LET threshold ($\mathrm{LET_{th}}$ is defined as the maximum LET value at which no effect was observed at an effect fluence of 1×10^7 ions/cm^2) is likely not very different. The cross section of the G4 is slightly lower, which is consistent with the reduced cell area. These results suggest that scaling between 0.3 and 0.2 μm feature size has little effect on SEU sensitivity.

The LET threshold of the SOI processor is about 1 MeV-cm^2/mg, and appears to be slightly lower than the LET threshold of the bulk processors. That result is somewhat surprising. The saturation cross section of the SOI is more than an order of magnitude lower than that of the bulk processors. These differences between the bulk and SOI processors will be discussed further in Section V. The large number of storage locations within the data cache allows more statistically significant numbers of be measured, decreasing the error bars due to counting statistics. For the data points where statistical error bars are not shown, they are smaller than the size of the plotting symbols. The cross section for "1" to "0" transitions is the same as that for "0" to "1" transitions.

Recent measurements of the D-cache SEU on the SOI PowerPC 7457 show that, similar to the previous D-cache SEU measurements, the cross section for "1" to "0" transitions is the same as that for "0" to "1" transitions. Fig. 5 compares results of the D-cache for the Motorola 7457 with results for the PowerPC 7455. It is somewhat surprising that the SEU results for the two SOI processors are so similar, given the difference in feature size and core voltage. Similar agreement was observed between D-cache results for the IBM PowerPC 750FX and the Motorola PowerPC 7455 [13]. These results suggest that scaling between

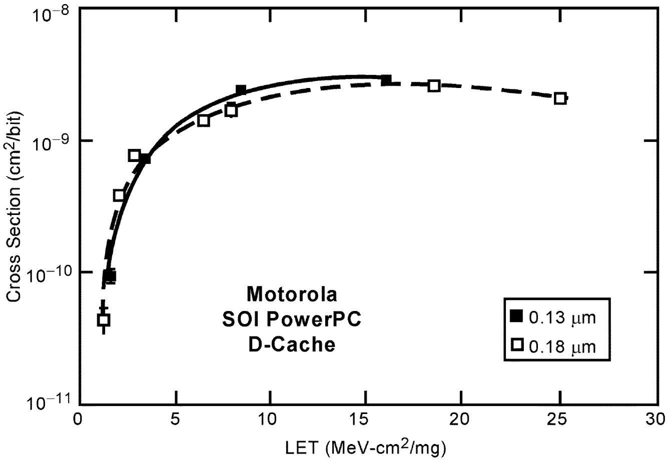

Fig. 5. Heavy-ion SEU cross section for the D-cache of the motorola 7455 and 7457 PowerPCs. The dashed and solid curves are only guides for the eye.

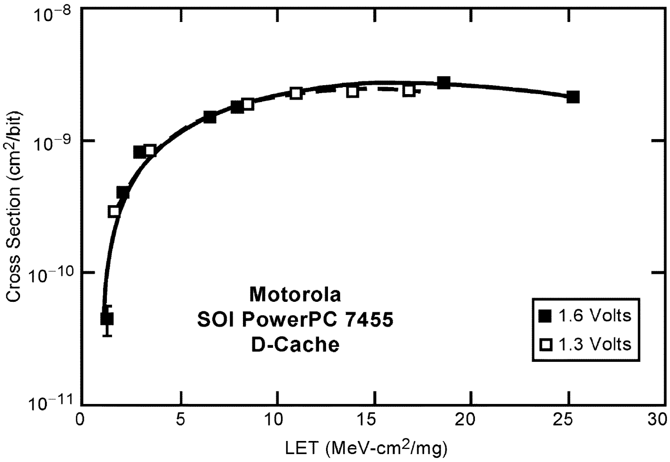

Fig. 6. Comparison of the heavy-ion SEU cross section for the D-cache of the motorola 7455 with two different internal core voltages. The dashed and solid curves are only guides for the eye.

0.18- and 0.13-μm feature size has little effect on SEU sensitivity. However, this trend may not continue as device sizes and core voltages are changed to even lower values.

We also repeated SEU measurements on a special version of the Motorola PowerPC 7455 that operates with lower internal core voltage specification, of 1.3 V. Fig. 6 compares the result of the measurements on the Motorola PowerPC 7455 with core voltage of 1.6 V [13] with the results of the Motorola PowerPC 7455 with a core voltage of 1.3 V [14]. There is no change in SEU cross section for D-cache.

V. DISCUSSION

The main advantage of SOI is marked reduction in the thickness of the silicon region for charge collection. To first order, this should decrease the collected charge by more than an order of magnitude compared to bulk/epi devices with equivalent feature size, increasing the threshold LET by at least a factor of ten. However, charge amplification from the parasitic bipolar transistor that is inherent in partially depleted SOI increases the charge by a significant factor. Although the charge amplification effect can be reduced by adding body ties to the structure that increases the area. Neither of the SOI processors in our studies uses body ties.

TABLE III
COMPARISON OF MOTOROLA AND IBM POWERPC FAMILY OF ADVANCED PROCESSORS

Device	**Feature Size (µm)**	**Film Thickness (nm)**	**Core Voltage (V)**	**Cross Section (cm^2/bit)**
Motorola 7455†	0.18	110	1.6	~2x10^{-9}
Motorola 7455†*	0.18	110	1.3	~2x10^{-9}
Motorola 7457†	0.13	55	1.3	~2x10^{-9}
IBM 750FX†	0.13	117	1.4	~2x10^{-9}
Motorola 7400	0.20	Bulk	1.8	~5x10^{-8}
Motorola 750	0.29	Bulk	2.5	~8x10^{-8}

* This is a special low power version of the Motorola SOI PowerPC 7455.

† SOI technology.

Feature sizes, silicon film thickness and internal core voltages are critical factors for SEU in SOI. Reduction in feature size and core voltage should reduce the SEU sensitivity. Decreasing the silicon film thickness increases bipolar gain, and reducing the internal core voltage limits the degree of improvement in SEU sensitivity that can be obtained with commercial SOI processors. Table III shows the feature sizes, film thickness, internal core voltages, and saturated cross section for the SOI and bulk generations of the PowerPC family.

Scaling for high-performance technologies depends heavily on reducing feature size, but also requires a reduction in power supply voltage [17]. Considerable work has been done showing that the critical charge for scaled devices is expected to be lower for more advanced devices [18]. This often leads to the conclusion that SEU will be far more severe for highly scaled devices. However, this has not been observed for high-performance devices such as microprocessors [19]. Other factors cause less charge to be collected as devices are scaled to smaller feature size.

As discussed in the Introduction, the threshold LET of commercial processes has changed very little with scaling, and is only slightly influenced by the concerns of mainstream manufacturers with atmospheric radiation. However, the saturation cross-section has steadily decreased with smaller feature size. Fig. 7 shows how the cross section for D-cache has changed over several generations of the PowerPC family [the abscissa is a logarithmic (base 2) inverse of scale reflecting the approximate doubling of feature size over various generations of CMOS devices]. The dashed lines show a slope of minus one half, reflecting the assumed dependence of area on the square of the feature size. There is a decrease of nearly a factor of ten in cross section with the transition to SOI processes. The gate and drain area of transistors in the IBM cache (provided by the manufacturer) are shown for comparison. The total cross section is slightly less than the sum of the areas of the drain and gate, which agrees with results obtained by the Sandia group in micro beam studies of devices from their SOI process, with 0.35 μm feature size [20].

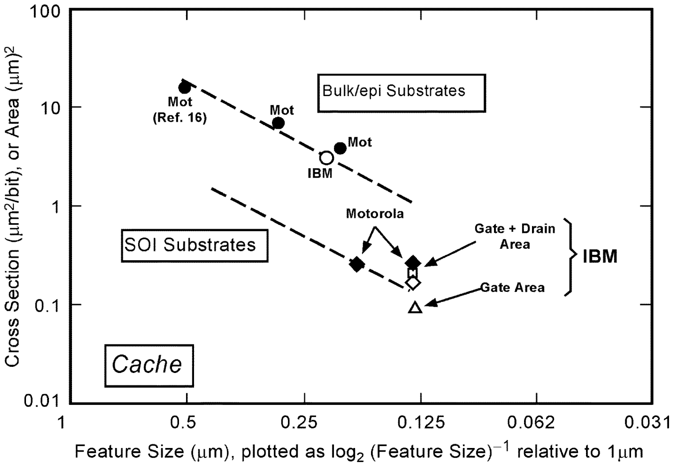

Fig. 7. Scaling trends for upset in D-cache (and basic SRAM designs) for PowerPC processors.

Silicon film thickness is a critical factor in SOI SEU. From the standpoint of electrical device design, there is a tradeoff between bipolar gain and the history effect (which causes switching waveforms to depend on previous switching waveforms). The history effect can be reduced by decreasing film thickness, but that increases bipolar gain. IBM has determined that a film thickness of 117 nm is an optimum design point [12], [21]. The film thickness of the Motorola 7455 was found to be 110 nm. Thus, the film thicknesses of the two SOI processors in the present study are very similar. However, the feature size of the IBM device is much smaller -0.13 μm—compared to the 0.18 μm feature size of the Motorola device. Thus, it is somewhat surprising that the SEU results for the two SOI processors are so similar, given the difference in feature size and core voltage.

Fig. 5 displays the comparison of D-cache measurements for the Motorola 7457 and 7455. There is a very good agreement between the data. Also, there is a good agreement between these data with D-cache result of the [13] for IBM 750FX. The similarity between D-cache results of the Motorola 7457 and IBM 750FX is somewhat surprising. The feature size and core voltage of two processors are the same. However, the film thickness of the Motorola 7457 is much smaller -55 nm—compared to the 117 nm film thickness of the IBM 750FX. These results might suggest that scaling between 0.18 and 0.13-μm feature size has no change in bipolar gain sensitivity. A similar conclusion is reported in [22].

Fig. 6 compares SEU cross-sections for the PowerPC D-cache operated with two different internal core voltages (1.6 and 1.3 V). Clearly there is good agreement between the two sets of data; however, one might expect the data set for the lower core voltage specification to have the larger cross section because of noise.

Charge collection will be lower when feature sizes are reduced below about 0.25 μm, because the lateral distribution of charge from the ion track of a highly energetic ion (i.e., galactic cosmic ray) will extend beyond the active area. The decreased junction area and lower voltage (required from scaling laws) both contribute to the reduced charge collection. This suggests that charge collection efficiency may be one of the reasons that the overall SEU sensitivity of advanced processors is only slightly affected by scaling. The decrease in critical charge is compensated by smaller area, along with decreased charge collection efficiency.

Although it is useful and instructive to make comparisons of SEU results as microprocessors within a given family evolve, one must remember that these are complex devices, not test structures. Other factors in the processor design may also affect the way that different processors in the series respond to radiation. There are also different requirements for various registers and functions within the device. For example, access time is a critical requirement for on-board cache, but cache SEU results may not be representative of other types of registers within the device.

The combination of the transition to SOI technology and the decrease in feature size reduces the error rate in deep space by more than a factor of 30 compared to error rates calculated for the Motorola PowerPC 750 (bulk/epi substrate with 0.29 μm feature size) [1]. The error rate in deep space (solar minimum) decreases from 10^{-6} to 3×10^{-8} errors per bit day, and would be approximately halved by taking the asymmetric cross section into account. That is a significant reduction.

VI. CONCLUSION

This paper presents the results for high-performance commercial microprocessors that are fabricated with SOI processes. Even though the silicon film thickness is below 0.2 μm, the threshold LET values of the SOI processors are nearly the same as those of bulk/epi processors from the same manufacturers, indicating that little improvement in SEU sensitivity has resulted from the move to SOI technology. There is not a change in SEU cross section for the SOI processors with feature sizes of 0.13 and 0.18-μm. These results suggest that scaling between 0.18 and 0.13-μm feature size has little effect on SEU sensitivity. However, one might expect to see reduction in saturated cross section when there is a drastic change in feature size e.g., 0.06 μm (next generation of SOI). For SOI processors with the same feature size and silicon film thickness, but with different internal core voltage specifications, no significant changes were observed in upset rates. The upset rates of these devices are low enough to allow their use in space applications where occasional upsets can be tolerated.

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