



Electronic
Parts
Engineering

VirtexII 3000 FPGA Dynamic Burn-In Test For Military And Aerospace Applications

Sponsored By NASA Electronic Parts and Packaging Program (NEPP)

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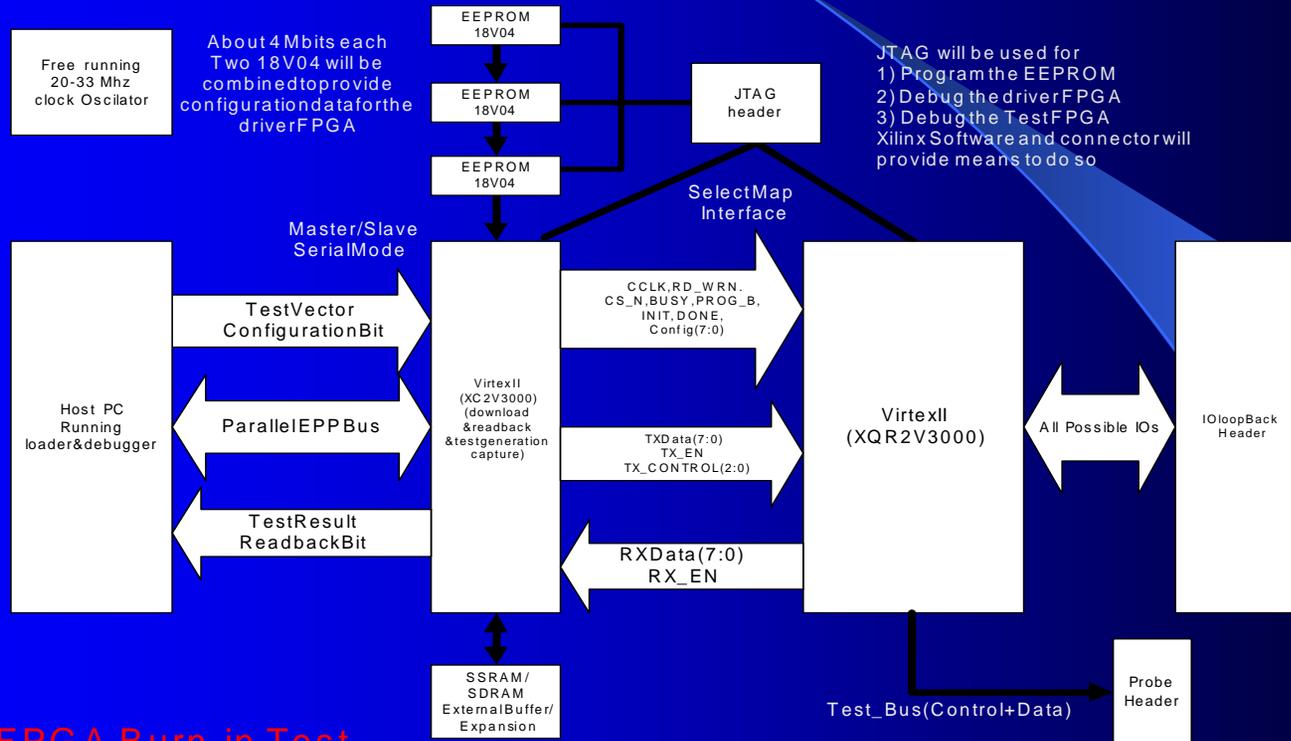
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System Block Diagram



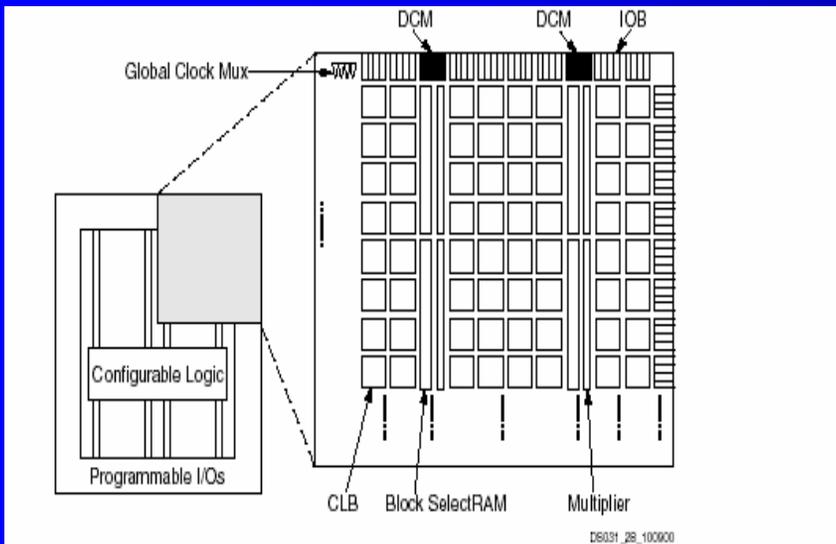
**FPGA Burn-in Test
Hardware & Circuitry
Rev 2**

JTAG will be used for
 1) Program the EEPROM
 2) Debug the driver FPGA
 3) Debug the Test FPGA
 Xilinx Software and connector will provide means to do so

Two Basic Operational Modes:
 1) Driver FPGA does the checking, test vectors shift into the test FPGA and results come back and are verified at the same time
 2) Host PC software does the check, test shifts in, result comes back and is stored in either the Driver FPGA's internal memory or external memory and for later retrieval

Building Blocks of VirtexII 3000

1. 3 Million system gates.
2. 14,336 slices, 3,584 CLB (Configurable logic blocks).
3. 448 Kbits of Distributed RAM
4. 96 Multiplier blocks
5. 96 Block select RAMs (18K bits each with 1,728 Kbits total)
6. 12 DCM (Digital Control Management), 16 Global Clock Multiplexor Buffers
7. 720 Maximum IO pads



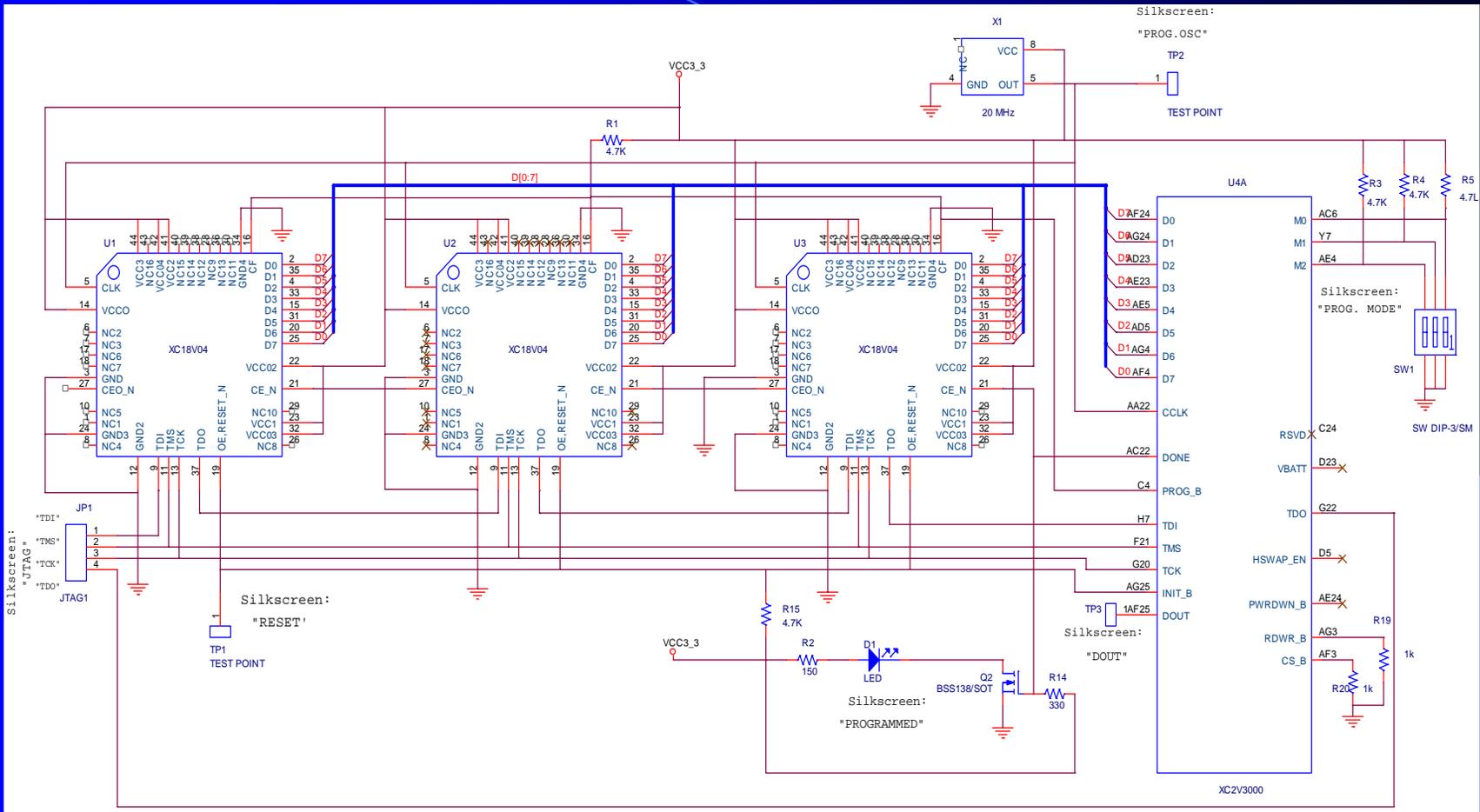


Driver FPGA Responsibilities

- Host PC/EPP Parallel Interface
- Test FPGA Download/Readback Interface
- Test Vectors Sending/Retrieving Interface
- Internal/External Test Vectors Interface
- Fault Detection Interface



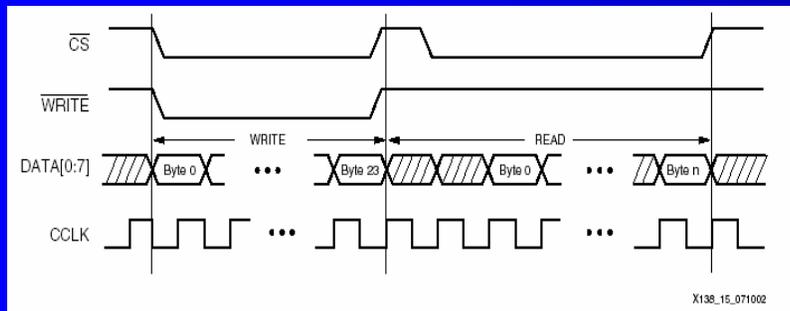
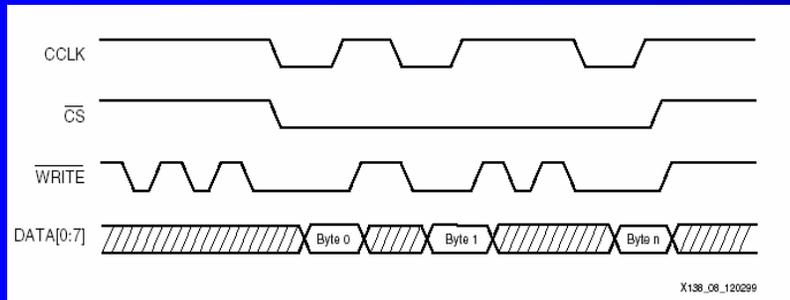
Driver FPGA Download



- Three Cascaded XC18V04 EEPROM Used (4,194,304 bits each)
- JTAG/Parallel Program Chain
- Master/Slave Serial Mode
- Automatic FPGA Configuration after each Power Cycle



Test FPGA Download



- Slave Select Map (8 bits Parallel) Mode
- Non-Contiguous CCLK Strobe Download
- Support ReadBack
- 17 Pins Mictor/Cable for Download Control/Data pins (expandable to 38)
- LED Notification of download



Sample Test (Burn-In) FPGA Designs

- Shifters: it will utilize as many as possible the LUTs (as SRL16s) and FFs to do bit Shifting around the entire chip.
- FIFOs: it will utilize as many as possible all the block RAMS and LUTS (as distributed RAMs) to 'FIFO' in and out data around the entire chip 8 bit wide.
- Calculators: it will occupy the entire chip with multiple 8 bits CRC engines and will Calculate CRCs for any given streams of data provided by the driver FPGA thus to test the arithmetic units inside the test FPGAs in addition to the previous two major tests.



Examples of Test FPGA Resource Utilization 1

- SHIFTER Design Summary:

- Number of Slices: 14,334 out of 14,336 or 99%
- Number of Slices containing unrelated logic: 5,237 out of 14,334 or 36%
- Number of Slice Flip Flops: 18,241 out of 28,672 or 63%
- Total Number 4 input LUTs: 9,000 out of 28,672 or 31%
- Number used as Shift registers: 9,000
- Number of bonded IOBs: 28 out of 516 or 5%
- IOB Flip Flops: 17
- Number of GCLKs: 1 out of 16 or 6%
- Total equivalent gate count for design: 722,067
- Additional JTAG gate count for IOBs: 1,344



Examples of Test FPGA Resource Utilization 2

- FIFO Design Summary:
 - Number of Slice Flip Flops: 1,885 out of 28,672 or 6%
 - Number of 4 input LUTs: 7,320 out of 28,672 or 25%
 - Logic Distribution:
 - Number of occupied Slices: 8,035 out of 14,336 or 56%
 - Number of Slices containing only related logic: 8,035 out of 8,035 or 100%
 - Number of Slices containing unrelated logic: 0 out of 8,035 0%
 - Total Number 4 input LUTs: 15,694 out of 28,672 or 54%
 - Number used as logic: 7,320
 - Number used as a route-thru: 182
 - Number used as Shift registers: 8,192
 - Number of bonded IOBs: 31 out of 516 or 6%
 - IOB Flip Flops: 21
 - Number of Block RAMs: 96 out of 96 or 100%
 - Number of GCLKs: 1 out of 16 or 6%
 - Total equivalent gate count for design: 6,894,037
 - Additional JTAG gate count for IOBs: 1,488



Examples of Test FPGA Resource Utilization 3

- CALCULATOR Design Summary:
 - Number of Slice Flip Flops: 8,447 out of 28,672 or 29%
 - Number of 4 input LUTs: 19,681 out of 28,672 or 68%
 - Number of occupied Slices: 10,733 out of 14,336 or 74%
 - Number of Slices containing only related logic: 10,733 out of 10,733 or 100%
 - Number of Slices containing unrelated logic: 0 out of 10,733 or 0%
 - Total Number 4 input LUTs: 19,686 out of 28,672 or 68%
 - Number used as logic: 19,681
 - Number used as a route-thru: 5
 - Number of bonded IOBs: 31 out of 516 or 6%
 - IOB Flip Flops: 21
 - Number of GCLKs: 1 out of 16 or 6%
 - Total equivalent gate count for design: 195,211
 - Additional JTAG gate count for IOBs: 1,488

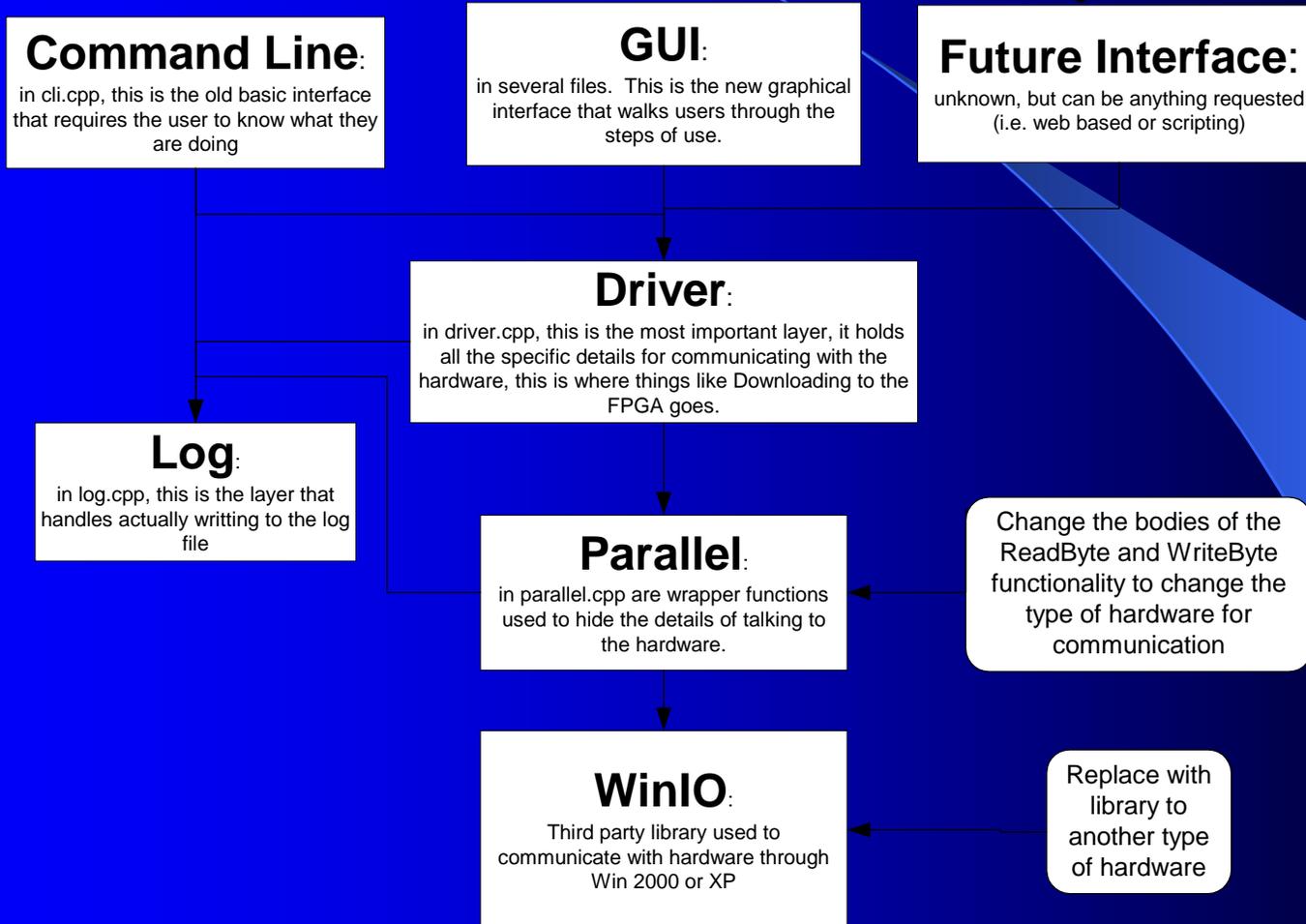


Highlights of Software Functions

- Graphical Interface operates under Windows2000
- Configure the test FPGA including download of the test program
- Setup the Driver FPGA's test Vector, then, read test results and give start/stop command
- Collect and report the test result by displaying the total error count
- Only three registers (8 bit each) to deal with -Control, Status, and Data with each a unique address as 0x01, 0x02, 0x03
- Two cycles, Data Cycle followed by Address Cycle



Software Flow & Hierarchy





Software Flow & Hierarchy (con't)

- The interface layer is replaceable
- The hardware layer and 3rd party access to hardware is replaceable.
- The log layer is not replaceable, but is POSIX compliant.
- The driver layer is where all the intelligence goes and is the core of the system



Software Tools

- The software was developed using Microsoft Windows's Visual Studio .NET
- The graphical components are in C++ and the non-graphical components are in C
- WinIO is a third party library that was chosen to gain direct hardware access under Windows 2000 and XP.
- The command line version was developed first and replaced by the graphical version.

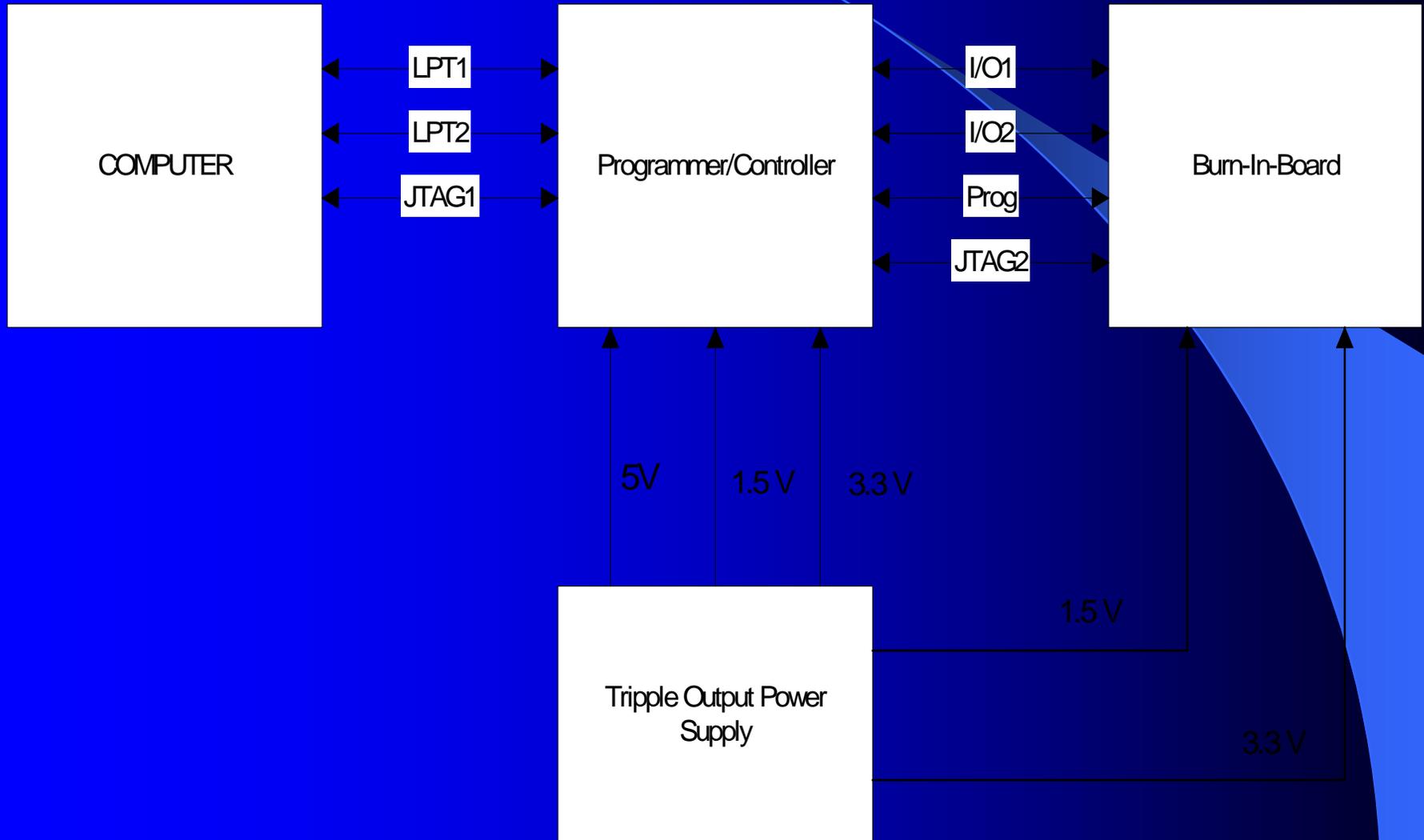


Hardware

- Printed Circuit Boards Design

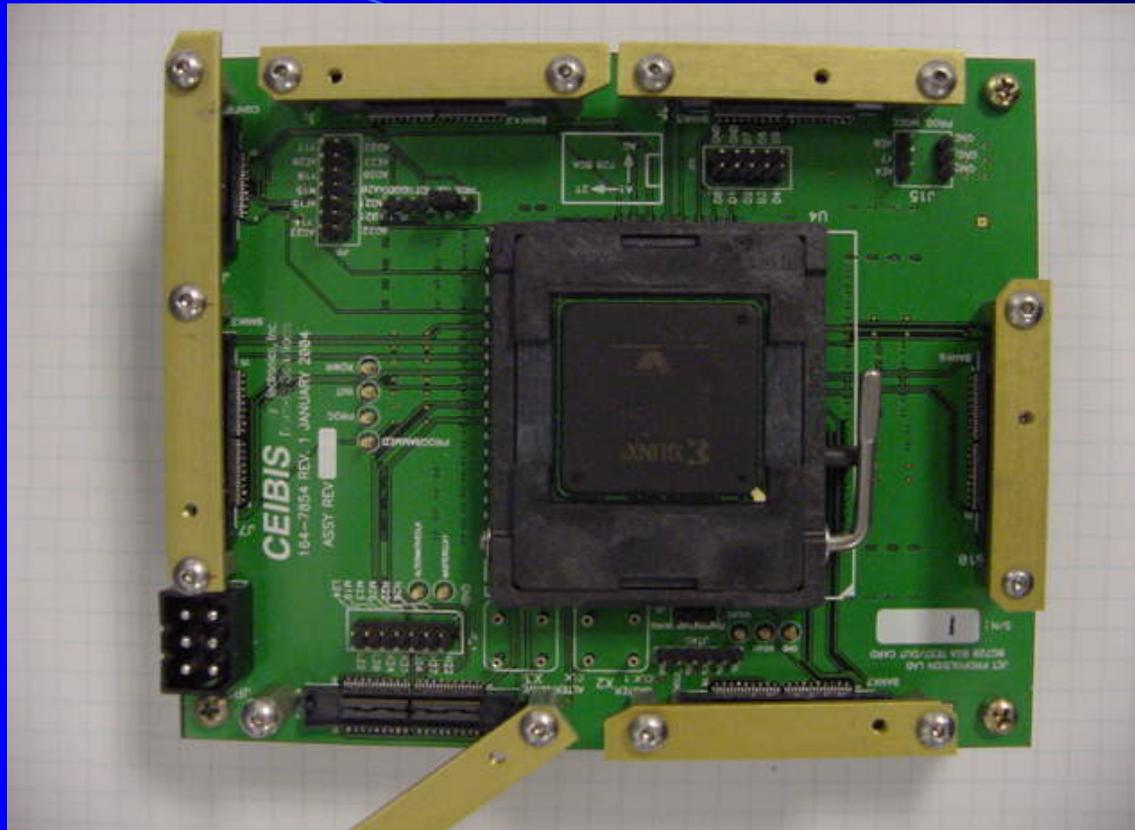


Test Bench Block Diagram

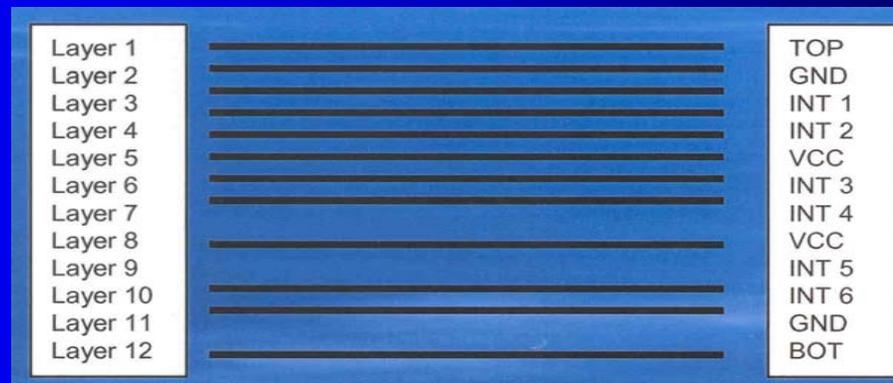




BURN-IN (TEST) PCB



PCB CROSSECTION



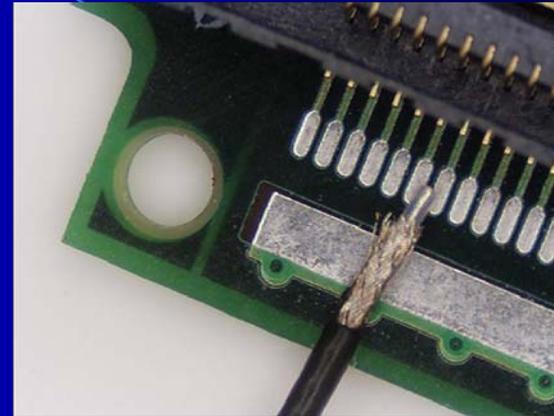
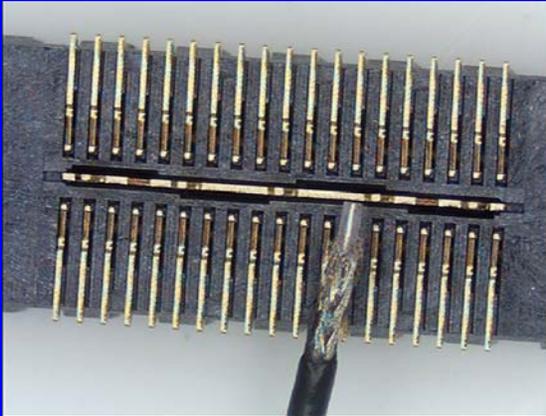


Burn-In Board Features:

- High reliability BGA burn-in socket (Center)
- Sockets for two optional high reliability oscillators
- Seven 50 Ohm high density connectors with clamps (six for data and one for configuration)
- Test points headers
- Clock and configuration selection jumpers
- JTAG connector
- Special purpose feedback lines (to configuration board)



Interconnect Cable



High density Mictor connector

4 layer Interface Board

Industry does not offer any transmission means (Cable) to satisfy specifications

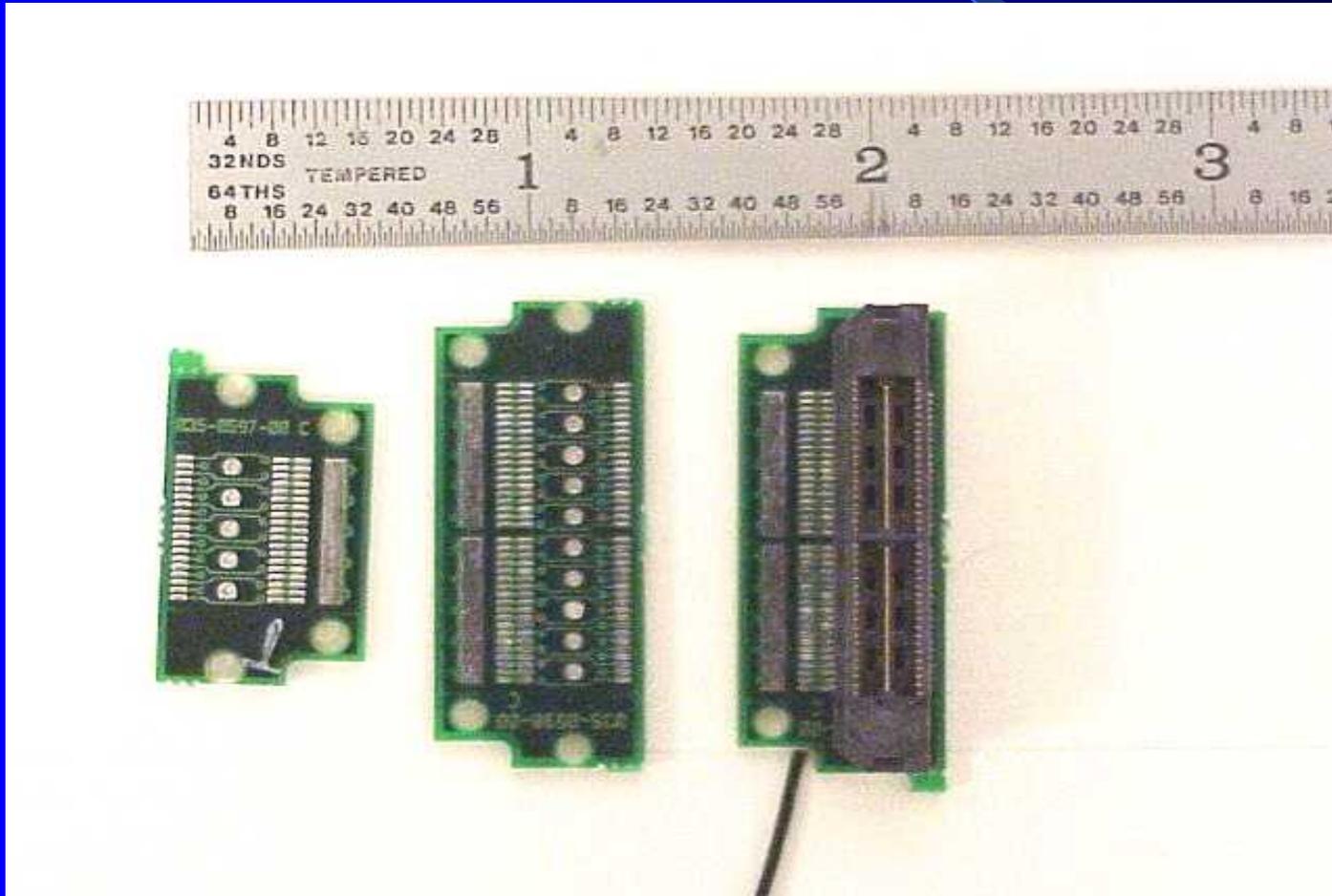
Cable assembly is based on Teflon astro-boa-flex^R III designed for space applications.

It offers:

- High frequency (rated up to 12 GHz) operation and high signal Integrity
- High temperature and controlled impedance
- Surpasses requirements of MIL-C-17



Connector Boards





Summary

- 2 PCB Boards for driver FPGA and test FPGA have been designed
- A special power supply designed for test system
- Graphical software control application has been written
- Hundreds of hours of testing have been performed at room temperature
- 200 hours of burn-in at 85 degree C performed
- Plan to perform at 125 degree C as well as SEU radiation test