Coded Performance of a Quaternary GMSK Communication System

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ABSTRACT – This paper investigates the performance of a coded quaternary Gaussian minimum shift keying (GMSK) signal with the Low Density Parity Check (LDPC) code. Performance simulation results for a frequency division multiple access (FDMA) communication system employing the LDPC-coded quaternary GMSK signal and an LDPC-coded QPSK signal are presented for a wide range of adjacent channel interference levels. It is shown that the LDPC-coded quaternary GMSK signal can have significant performance advantage over the LDPC-coded QPSK signal in an FDMA system with severe adjacent channel interference.

1. INTRODUCTION

Gaussian minimum shift keying (GMSK) is a form of continuous phase-modulated (CPM) signals with constant envelope and spectral occupancy that can be made narrow via suitable pre-modulation filtering. Constant envelope signals are compatible with saturated amplifier operation without the concomitant side-lobe re-growth of amplitude-modulated signals when passing through a saturated amplifier. Thus, employing a GMSK signal in a communication system allows the transmitter amplifier to operate at maximum output power without compromising the designed spectral occupancy of the signal. The narrow spectral occupancy and rapid side-lobe roll-off provided by the GMSK signal make it an attractive signaling format to use in FDMA communication systems where total system bandwidth is constrained and adjacent channel interference needs to be minimized. To date, binary GMSK signals of moderate bandwidth efficiency has been successfully implemented in various commercial wireless communication systems, while binary GMSK signals of higher bandwidth efficiency has been adopted in the design of future military satellite communication systems.

Using a symbol alphabet consisting of four distinct symbols per signaling interval, quaternary partial response GMSK signals, like QPSK signals, have the potential of further improving the bandwidth efficiency of a bandwidth-limited communication system. However, the power efficiency of quaternary GMSK signal is generally inferior to the binary GMSK signals with the same BT product due to increased inter-symbol interference in the signal. Thus, in systems where a quaternary GMSK signal is used it is advantageous to employ powerful forward error-correction (FEC) codes such as Turbo codes or Low Density Parity Check (LDPC) codes to improve the power performance of the communication system. As described in [1], LDPC codes have better block error performance than that of the Turbo codes, thus making them attractive choices for high-speed data transmission systems in which very low frame error probability is required. This is mainly due to the fact that the minimum distance of an LDPC code increases proportionally to the code length with high probability[2]. In addition to their excellent block error performance, highly parallel LDPC decoder architecture is realizable by directly instantiating the LDPC decoding algorithm to hardware, resulting in a very high speed LDPC decoder hardware[3]. The primary purpose of this paper is to provide a LDPC-coded performance comparison between the quaternary GMSK signal and a filtered QPSK signal for an FDMA system where a non-linear transmit amplifier is employed in each channel, and where adjacent channel power differential ranges from benign to severe levels. A performance comparison of the LDPC and Turbo codes with the quaternary GMSK signal for the additive white Gaussian noise (AWGN) channel is also provided.

This paper is organized as follows. Section 2 briefly describes a soft bit metric demodulator that enables soft decision decoding of a coded quaternary GMSK signal. Section 3 describes the encoding and decoding algorithms of the LDPC code. In section 4 the simulation model of the FDMA communication system is described. Simulated performance results of an LDPC-coded FDMA system employing a saturated transmit amplifier at each channel are compared for the quaternary GMSK signal and a filtered QPSK signal for various adjacent channel interference power levels. Lastly, simulated performance results of the LDPC- and Turbo-coded quaternary GMSK signal for the AWGN channel with no adjacent channel interference are compared. Section 5 concludes the paper.

2. QUATERNARY SOFT BIT METRIC DEMODULATOR

In this section we give a brief description of the quaternary GMSK soft bit metric demodulator employed in this investigation. The reader is referred to [4] for a detailed

discussion. Figure 1 shows the structure of a three-filter soft bit metric demodulator for a quaternary GMSK signal with a modulation index h=1/4. The complex envelope of the received GMSK signal with channel disturbance is denoted by $z_r(t)$ in Figure 1.

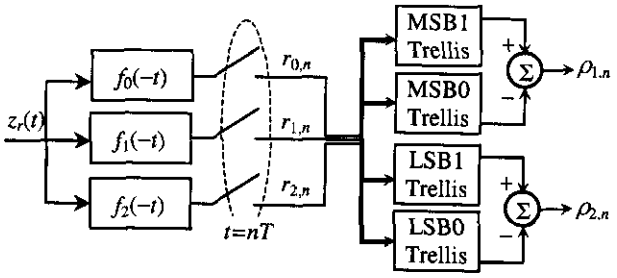

Figure 1. Quaternary GMSK 3-filter Soft Bit Metric Demodulator.

The three receiver filters, called the principal Laurent filters, are easily obtained from the modulation index h and the GMSK pre-modulation filter pulse response $f(t)$ via the following computations:

$$g(t) = \int_0^t f(\tau)d\tau \quad (g(LT)=1)$$

$$c(t,a) = \begin{cases} \sin(\pi a - \pi a g(|t|))/\sin(\pi a), & |t| \le LT \\ 0, & |t| \ge LT \end{cases}$$

$$h_0(t,a) = \prod_{i=1}^{L} c(t-iT,a)$$

$$f_0(t) = h_0(t,h)\cdot h_0(t,2h)$$

$$f_1(t) = h_0(t+T,h)\cdot h_0(t,2h)$$

$$f_2(t) = h_0(t,h)\cdot h_0(t+T,2h)$$

where T is the symbol duration and LT is the support of the pulse response $f(t)$. Assuming ideal symbol time and carrier phase synchronization the soft bit metrics of the quaternary GMSK signal at symbol times are computed from the Laurent filter outputs by operating the Viterbi algorithm over two pairs of 'state-constrained' trellises as shown in Figures 2 and 3. Each of these trellises has four states, defined as the 2-bit pattern associated with a quaternary symbol, with MSB and LSB denoting the most- and least-significant bit, respectively. For $0 \le t < nT$, both the 'MSB1' and 'MSB0' trellises in Figures 2a and 2b are 'propagated' in an exact manner as the unconstrained four-state trellis of a MLSE demodulator. For the nth symbol, an MSB=1 state transition constraint is imposed on the MSB1 trellis while an MSB=0 constraint is imposed on the MSB0 trellis. Each of these MSB trellises re-merges into an unconstrained trellis at symbol time $(n+1)T$ and continues to propagate in an MLSE-like manner for another (N_d-1) symbol intervals, with $N_d \ge 1$ being an adjustable parameter. As detailed in [4], the Viterbi algorithm seeks maximum signal correlation across the time interval $0 \le t < (n+N_d)T$ for each of the MSB trellises, and differencing the two resulting survivor path weights yields the MSB soft decision metric with a decision delay of N_dT. The LSB soft decision metric is obtained in a similar manner via the 'LSB1' and 'LSB0' trellises in Figures 3a and 3b. It should be noted that there is no need to store the survivor path states when exercising the Viterbi algorithm over each of the four constrained trellises: only the cumulative survivor path weights need to be updated. Also, as the unconstrained MLSE trellis portion over the interval $0 \le t < nT$ is common to all four constrained trellises, the associated processing needs only be performed once.

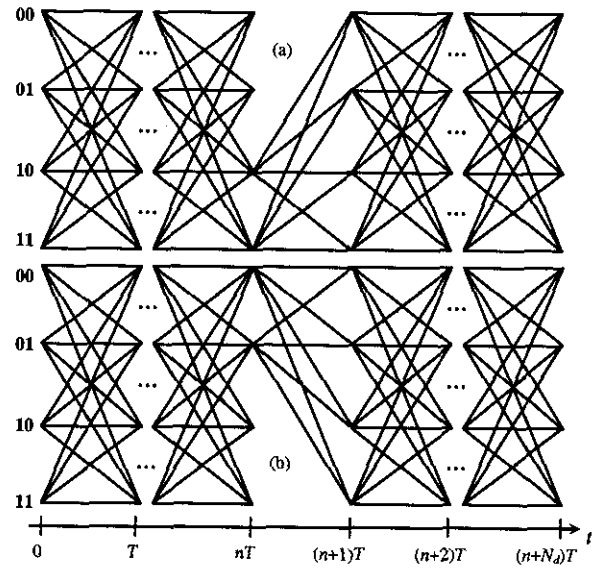

Figure 2. MSB Constrained Trellises: (a) MSB1, (b) MSB0.

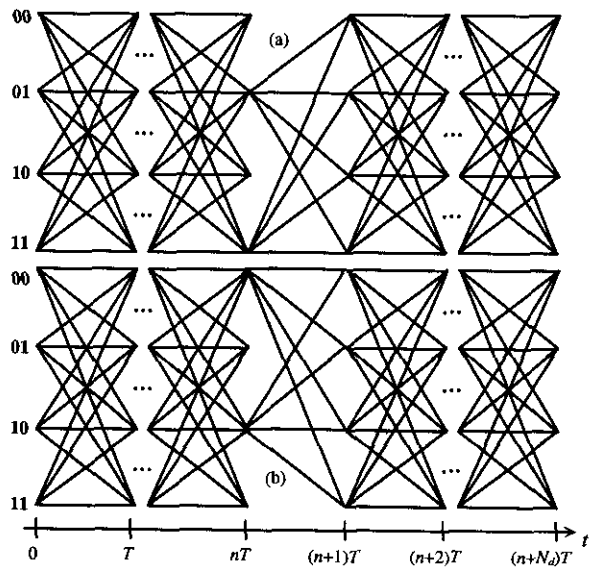

Figure 3. LSB Constrained Trellises: (a) LSB1, (b) LSB0.

The choice of the decision delay parameter N_d depends on the projected bit error rate at the decoder input, which in turn depends on the choice of FEC code and the ultimate

objective BER. As an example, for a quaternary GMSK signal with $BT=1/3=1/L$, $h=1/4$ and a projected decoder input BER of 10^{-2} or greater, using an N_d value less than 3 results in considerable performance degradation with respect to the MLSE demodulator, whereas virtually no demodulation performance improvement can be gained by using an N_d value greater than 3. The choice of $N_d=3$ is also sufficient for a quaternary GMSK signal with $BT=1/2=1/L$ and $h=1/4$.

3. LDPC CODE

LDPC codes and the associated iterative decoding algorithm were proposed[2] by Gallager in 1962. LDPC codes have been almost forgotten for about thirty years, in spite of their excellent properties. However, LDPC codes are now recognized as good error-correcting codes achieving near Shannon performance limit[6].

LDPC codes are defined as codes using a sparse parity-check matrix with the number of 1's per column (column weight) and the number of 1's per row (row weight), both of which are very small compared to the block length. LDPC codes are classified into two groups, regular LDPC codes and irregular LDPC codes. Regular LDPC codes have a uniform column weight and row weight, and irregular LDPC codes have a nonuniform column weight. We describe an LDPC code defined by an M x N parity-check matrix H as (N,K) LDPC, where $K = N-M$ and the code rate is $R = K/N$. LDPC codes can be decoded by using a probability propagation algorithm known as the sum-product or belief propagation algorithm. LDPC codes have better block error performance than Turbo codes, because the minimum distance of an LDPC code increases proportional to the code length with a high probability. Such a property is desirable for the high-bit-rate transmission that requires very low frame error probability.

An LDPC code typically is represented by a bipartite graph, usually called Tanner graph, between N variable (or message) nodes in one set and M check (or constraint) nodes. This is illustrated in Figure 4. LDPC codes can be effectively decoded by the iterative belief-propagation (BP), also known as sum-product, algorithm. The structure of BP decoding algorithm directly matches the Tanner graph: decoding message is computed on each variable node and check node and iteratively exchanged through the edges between the neighboring nodes. It is well known that BP decoding algorithm works well if the underlying Tanner graph does not contain too many short cycles. Thus, it is typically required that the random Tanner graph should be 4-cycle free, which is easy to achieve, but the construction of random Tanner graph with higher order cycle free is not trivial. Besides their excellent performance, another important reason why LDPC codes attract so many attentions is that the BP decoding algorithm is inherently fully parallelizable and the computation associated with each node (variable node or check node) is very simple, thus a great potential decoding speed can be expected. It is clear the efficient hardware LDPC code decoder/encoder implementation is one of the most crucial issues determining the extent of LDPC application in the real world.

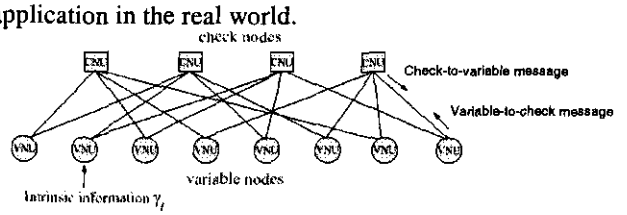

Figure 4. Tanner Graph Representation of an LDPC Code.

We can summarize the BP algorithm as follows:

1. Initialize each variable node with the intrinsic (or channel) information obtained from the received bit and, based on this, compute the variable-to-check message;
2. Deliver the variable-to-check message from variable nodes to check nodes along the edges of Tanner graph;
3. Each check node generates the check-to-variable message based on all incoming message from connected variable nodes;
4. Deliver the check-to-variable message from check nodes to variable nodes along the edges of the Tanner graph;
5. Using the incoming message and intrinsic information, each variable node updates the estimate of the corresponding bit and generates the outgoing variable-to-check message;
6. Repeat steps 2 through 5 until either (a) the current estimated block is a valid codeword, or (b) a fixed number of iterations have occurred.

4. SIMULATION RESULTS

Figures 5 and 7 show a 3-channel model of the rate-1/2 LDPC-coded FDMA communication system used in the simulation. A quaternary GMSK modulation with $BT=1/2$ is used in Figure 5, and a square-root raised cosine (RRC) filtered QPSK modulation with $\beta=0.33$ roll-off factor is used in Figure 7. Each channel in both FDMA systems employs a transmit traveling-wave tube amplifier (TWTA) with AM/AM and AM/PM characteristics shown in Figure 6. The 3-channel model is deemed adequate for the purpose of assessing the effect of adjacent channel interference (ACI) on system performance since the total interference power seen by any given channel in an FDMA system is dominated by the two closest neighboring channels. Figure 9 gives a notional illustration of the 3-channel ACI simulation models shown in Figures 5 and 7. In Figure 9 Δf denotes the carrier spacing between the neighboring channels, and A_I denotes the power differential of the channels.

The LDPC code used in the simulation is a rate-1/2 regular LDPC code. A block length of 1024 information bits is used for the simulation. The use of a block channel interleaver is optional for the LDPC code. This is because an LDPC code effectively has a built-in channel interleaver due to the random-like connectivity between its code symbols and its parity constraints. The LDPC-coded performance of the two modulations operating with a saturated transmit amplifier is shown in Figure 8 for various values of adjacent channel power differential. It is seen that, for benign ACI condition, the performance of the quaternary GMSK system is slightly inferior to that of the RRC-filtered QPSK system, whereas the former performs significantly better than the latter under severe ACI condition. The inferior performance of the RRC-filtered QPSK signal is attributed to the spectral re-growth caused by the saturated transmit amplifier, whereas the spectral occupancy of the constant envelope GMSK signal remains unaffected.

Finally, the BER performance of a rate-1/2 regular (3,6) LDPC code and an irregular [(2,3,6),6] "multiple edge-type" (MET) LDPC code, as well as a popular near rate-1/2 Turbo code, are compared in Figure 10 for the GMSK system in the AWGN channel without ACI. The information block size of both LDPC codes is K=1024 bits. The Turbo encoder used is based on the standardized Consultative Committee for Space Data Systems (CCSDS) Turbo encoder[7], consists of two 16-state convolutional encoders, connected with an algorithmically described interleaver. Information block size K is 1020 due to trellis termination. Unlike LDPC code, block channel interleaver of the same size as the Turbo encoder block is required for Turbo coded modulation system. It is observed that, for the AWGN channel without ACI, the irregular MET LDPC code performs nearly as well as the Turbo code, whereas the performance of the regular (3,6) LDPC code is about 0.5 dB worse.

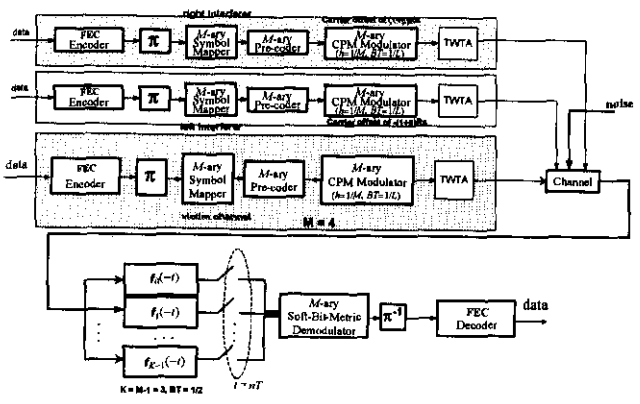

Figure 5. Coded Quaternary GMSK FDMA Communication System.

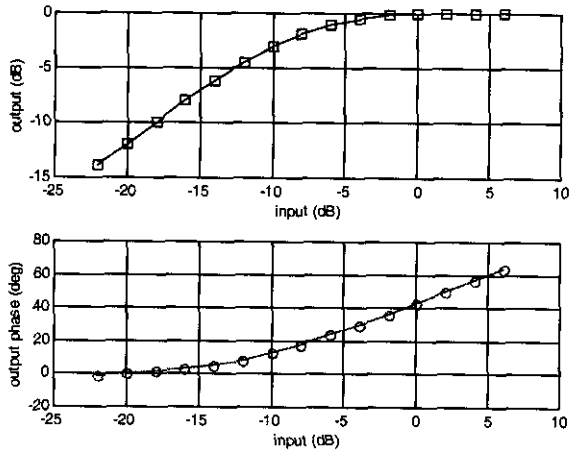

Figure 6. Transmit TWT Amplifier AM-AM, AM-PM Characteristics.

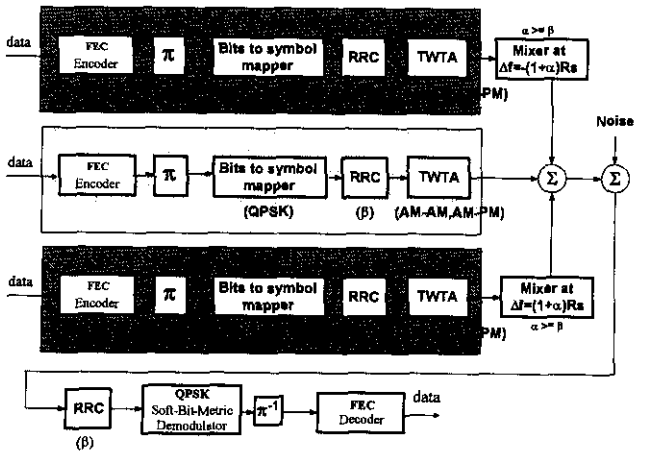

Figure 7. Coded RRC-filtered QPSK FDMA Communication System.

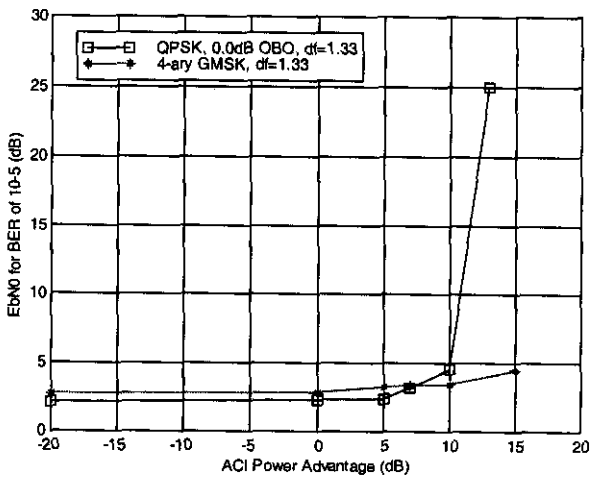

Figure 8. LDPC-coded Performance Comparison in ACI.

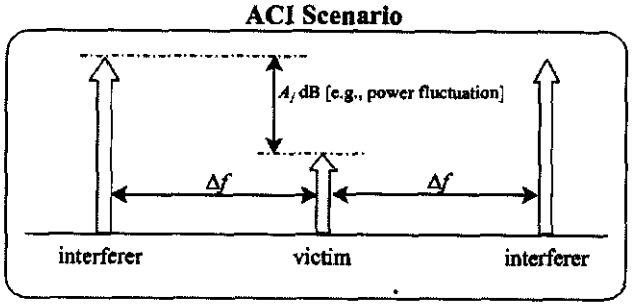

Figure 9. Notional ACI Simulation Model.

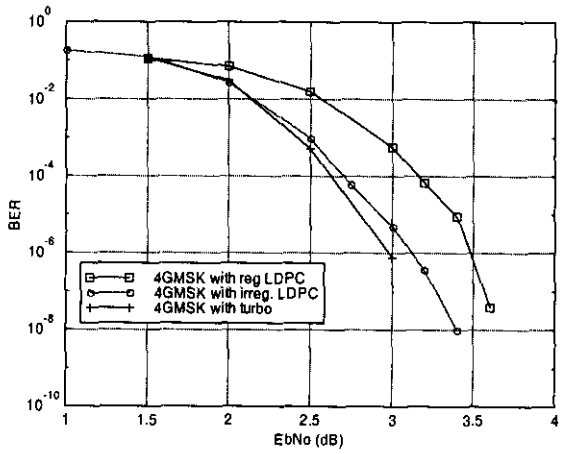

Figure 10. Coded Quaternary GMSK Performance in AWGN.

5. Conclusions

This paper has presented performance simulation results for an FDMA communication system employing an LDPC-coded quaternary GMSK signal and an LDPC-coded QPSK signal for various adjacent channel interference levels. It is shown that, with benign ACI condition, the LDPC-coded QPSK signal performs slightly better than the LDPC-coded quaternary GMSK signal, whereas in moderate to severe ACI condition, the LDPC-coded quaternary GMSK signal can have a significant performance advantage over the LDPC-coded QPSK signal. Given the excellent performance of the LDPC-coded quaternary GMSK waveform and the availability of high speed parallel LDPC decoder hardware, this coded modulation proves attractive in the design of FDMA communication systems in which saturated transmit amplifiers are employed, very low bit error rate is required and moderate to severe adjacent channel interference is anticipated.

ACKNOWLEDGMENTS

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