

Instructions

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## SEU Mitigation Testing of Xilinx Virtex II FPGAs



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The research done in this paper was carried out at the Jet Propulsion Laboratory, California Institute of Technology, under contract with the National Aeronautics and Space Administration (NASA), under the NASA Electronic Parts and Packaging Program (NEPP), Code AE and the collaboration of Xilinx Inc. and The Aerospace Corp.

*Abstract* - Re-configurable programmable logic is widely accepted and used in space flight applications but are susceptible to single-event upset. Three upset detection and mitigation schemes have been tested on the Xilinx Virtex II XC2V1000 in heavy-ion and proton irradiation to control and mitigate SEUs. An analysis of a simple design using mitigation schemes such as Triple Modular Redundancy (TMR), partial reconfiguration or both will demonstrate the effectiveness of these methods.

## Introduction

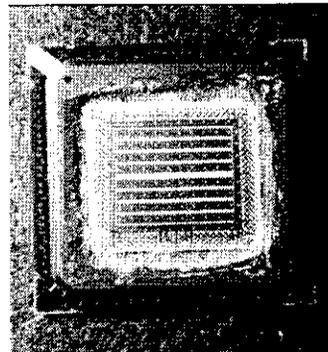
- Usage of field programmable gate arrays (FPGA) in space systems is *increasing* due to flexibility, on-orbit programmability and recovery of in-flight failures
- Advancing technologies allow for higher speed, lower power consumption. More cost effective than discrete logic devices
- The Xilinx Virtex II FPGA is an SRAM-based reprogrammable FPGA with partial reconfiguration and readback capability
- Static memory elements (latch, flip-flop, RAM) are susceptible to single-event upset (SEU)
- Mitigation techniques can be applied to control or remove the effects of SEU
- Objective: To verify the effectiveness of the mitigation techniques on a simple design using heavy ions and protons

## History

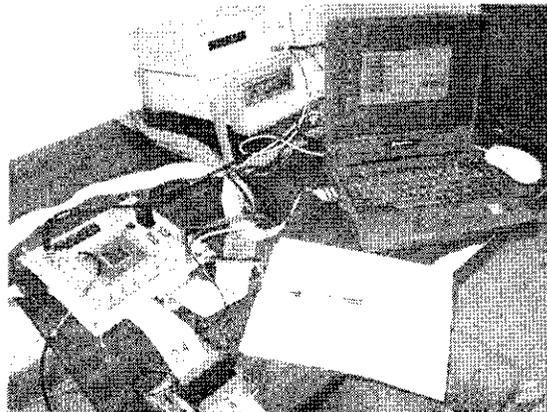
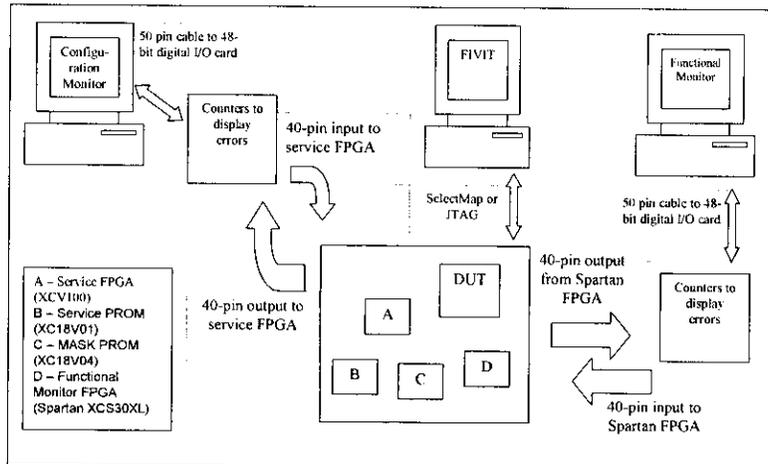
- 2 test methods for FPGA single-event-effects testing
  - Static: monitoring configuration upsets without toggling clock, inputs, outputs of a fully configured device during irradiation
  - Dynamic: monitoring configuration and functionality of a configured device during irradiation
- Comprehensive static testing has been conducted and reported at MAPLD, 2002 [1]
- Two dynamic tests have been done at Crocker Nuclear Laboratory and Lawrence Berkeley National Laboratory to understand SEU sensitivity in this test mode
- An on-going test effort is currently being led by the Xilinx Consortium to study the radiation performance of other Virtex II capabilities and device types

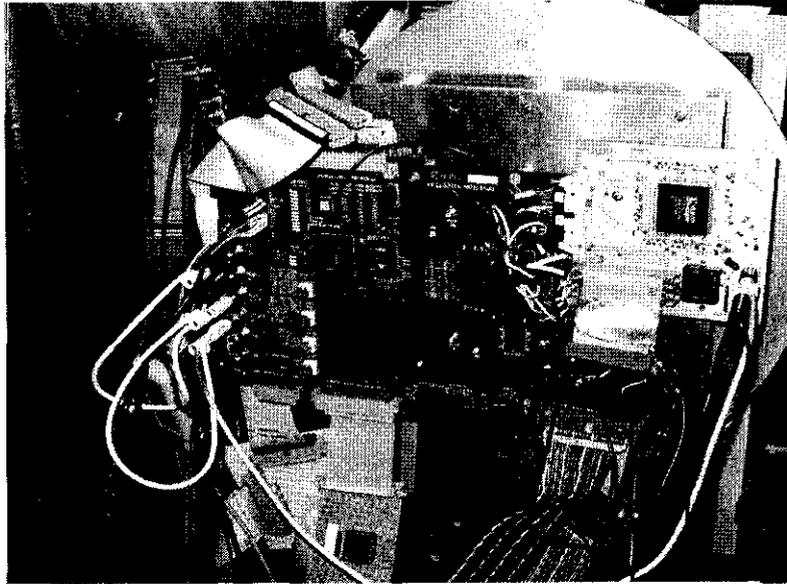
## Device Type Information

- Virtex II XC2V1000
- 256 pin wire-bond standard ball gate array (BGA) package
- 0.15/0.12 um CMOS 8 layer process
- 2.8M configuration bits, 40 block RAMs (737,280) bits, 432 maximum I/Os
- Special test samples – manufactured with mask intended for XQR devices without epitaxial layer



# Test Setup





- Test setup is composed of the DUT board, Configuration Monitor and Functional Monitor
  - DUT board is a Xilinx development board with an on-board FPGA
  - The on-board FPGA also known as “service FPGA”, acts as the “Configuration Monitor” – constantly detects and removes errors from the configuration bitstream through readback and partial reconfiguration
    - Readback – the ability to readback data from the configuration memory post-configuration
    - Partial reconfiguration – also known as “scrubbing”, ability of device to be partially reconfigured by reloading only the crucial segment of the configuration bitstream [2]
    - Neither function disrupt the operation of the device
  - The “Functional Monitor” is another Xilinx FPGA used to generate test vectors to the DUT and compare DUT outputs with expected values
- Custom Visual Basic software on separate host computers are used to control and record the activity of the Configuration and Functional Monitors
- Custom counters were also used on both monitors to display the errors as they occurred

## Test Design

- Non-mitigated: Eight simple shift registers using 500 flip-flops each (40% of available flip-flops)
- Mitigated: Eight shift registers using 500 flip-flops each, four have TMR implementation (80% of available flip-flops)
- Test vectors are chosen by the user: pattern of all zeroes, ones, or checkerboard

## Test Results

- Background
  - 1<sup>st</sup> mitigation technique: Triple Module Redundancy (TMR)
    - Implements three full copies of the base design in the FPGA
    - SEUs and single-event transients (SETs) can be removed by performing a bit-wise “majority vote” on the output of the triplicate circuit (flip-flop or entire logic design)
  - 2<sup>nd</sup> mitigation technique: Partial reconfiguration (PRC)
    - Partially reconfiguring the configuration bitstream prevents the accumulation of errors, a cause of functional failure in the programmed design
- Summary
  - Most recommended technique: TMR & PRC
    - This study shows that when both techniques are used in conjunction, the design is shown to be functionally immune to upsets
    - Functional failure is defined for the dynamic test to be a

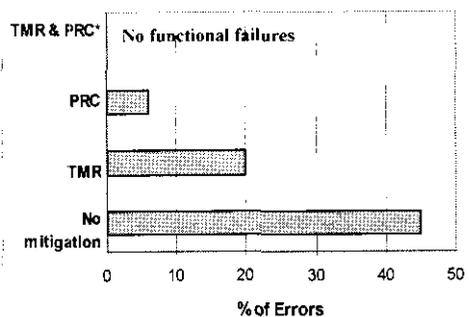
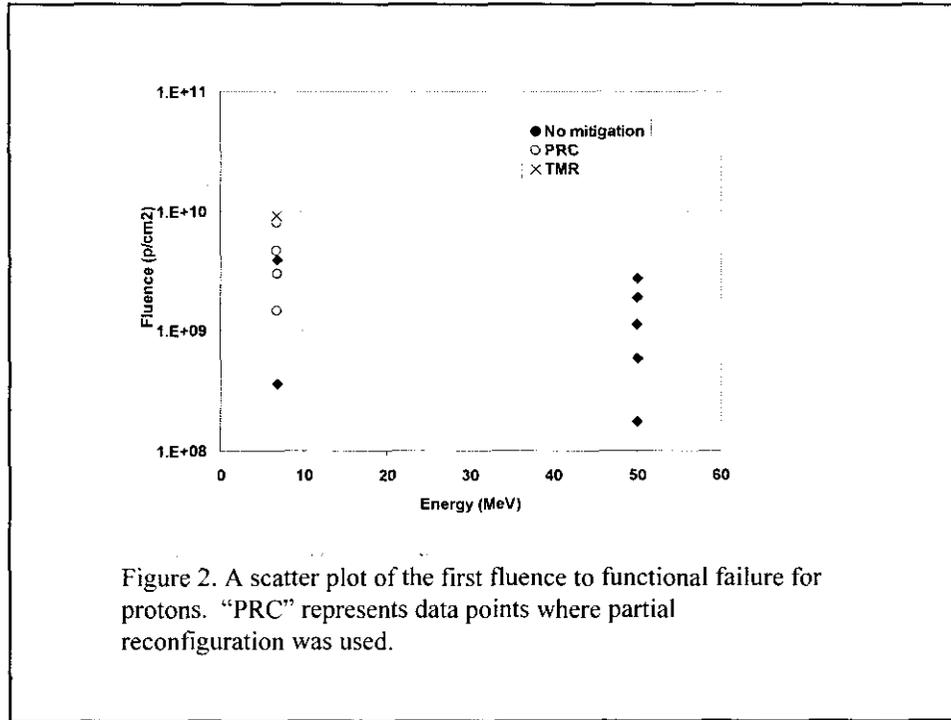


Figure 1. A comparison of frequency of functional errors to total runs for different shift register designs.

- Figure 1 show the average results from five runs for each design tested in protons
- The comparison shows an improvement of roughly 25% for the TMR design, 40% for the design implementing partial reconfiguration and no functional errors for the design employing both TMR and PRC
- However, although no functional errors were seen during the dynamic test of the TMR and PRC design, one single bit error for one shift register chain was noted during one beam run
  - Possible causes: Two simultaneous bit flips to the TMR voter circuit, ion strike to the input/output blocks



- Test vehicle first used at Crocker Nuclear Laboratory for proton testing
- All three mitigation designs were tested at 6.8 MeV
- The scatter plot of average first fluence to failure in Figure 2 shows an approximate factor of two difference between the non-mitigated and mitigated designs
- Best results were obtained from the DUT programmed with the TMR and PRC design; no functional errors were observed

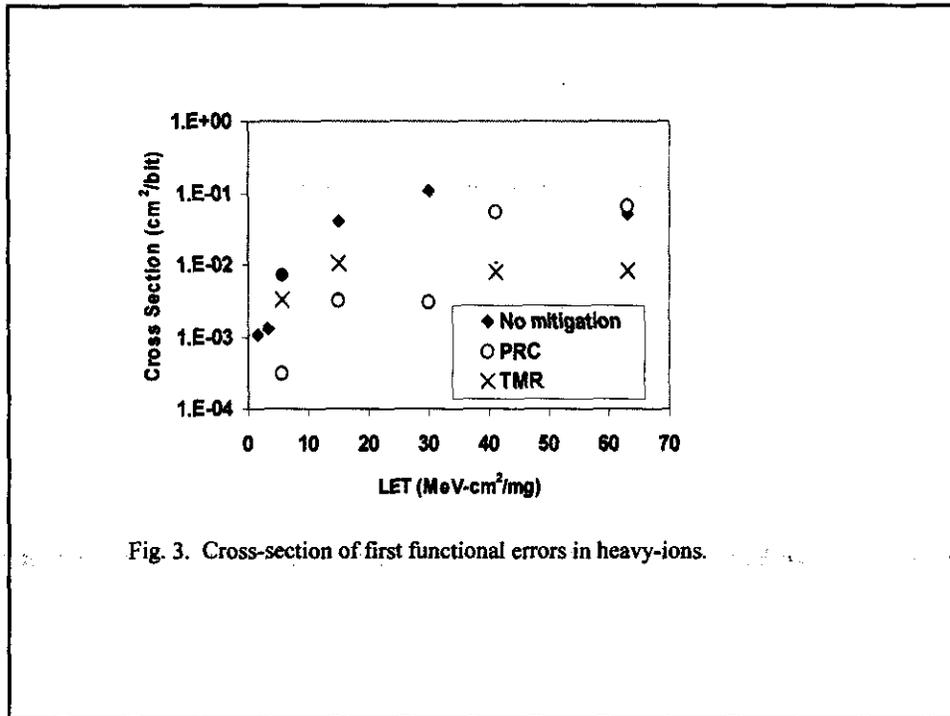


Fig. 3. Cross-section of first functional errors in heavy-ions.

- The comparison of average cross-section for first functional errors in heavy ions in Figure 3 shows a varied scattering, a function of Poisson's probability distribution, a mathematical computation of the probability of atypical events in a given time period
- Cross-section of non-mitigated data points are about a magnitude higher than that of a TMR design
- Present data has limited statistics, additional testing is required

## Single-Event-Functional Interrupts (SEFIs)

- Besides upsets to the static memory logic, there are three noted SEFIs in which the DUT is susceptible
  - Power-on-reset (POR) SEFI
  - Select Map SEFI
  - JCFG SEFI
- SEFI events occur when an ion strikes the power-on-reset, Select Map or JTAG circuitry
- Criteria for a SEFI event: a complete reconfiguration of the device is required before returning to normal operability

POR	
<b>Effects</b>	Clearing of configuration memory and loss of state data
<b>Detection</b>	Done pin transitions low, I/O becomes tri-stated, no user functionality available
<b>Recovery</b>	Standard configuration. No power cycle necessary.
Select Map	
<b>Effects</b>	Loss of communication with configuration logic. Configuration error detection and non-evasive correction unavailable.
<b>Detection</b>	Non-response to data readbacks
<b>Recovery</b>	Standard configuration. No power cycle necessary.
JCFG	
<b>Effects</b>	Loss of communication with configuration logic. Configuration error detection and non-evasive correction unavailable.
<b>Detection</b>	Read access to configuration memory returns constant value.
<b>Recovery</b>	Standard configuration. No power cycle necessary.

- The dynamic test vehicle had two SEFI detection mechanisms
  - POR detection was made possible by constantly monitoring the state of the “DONE” pin of the device
  - Simple feed-through signals in the DUT placed in close proximity can indicate when the configuration memory has accumulated excessive errors
  - No Select Map detection was provided since only JTAG was used
- Two SEFI events were recorded during dynamic testing in heavy ions:
  - POR: DONE pin transition to low, functionality is lost
  - JCFG: Unable to read or write to the configuration memory, scrubbing is disabled
- The mechanism of SEFIs are independent of mitigation and are inherent in the device. Proper mitigation and device redundancy can be used to remove all possibilities of single-event upset and

## Conclusion

- Three mitigation techniques have been implemented for the XC2V1000
- Comparison of frequency of functional failures demonstrate the benefit of using both TMR and PRC mitigation techniques
- More testing will be done on designs of greater complexity as part of the on-going test effort. Results will be made publicly available upon completion.

#### ACKNOWLEDGMENT

The authors wish to thank Travis Minto, Duc Nguyen and Michael O'Connor of Jet Propulsion Laboratory for their support of this work.

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