

New Process and Pixel Structure of an SOI-CMOS Imager

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Abstract

We present architecture, process design and results from test pixels of a new Active Pixel Sensor (APS) imager implemented in 0.8 μm SOI-CMOS technology. The conventional partially-depleted SOI-CMOS process has been altered by adding one lithography for buried oxide window opening and two implants into the handle wafer. Results on front illuminated photodiode arrays show that the Quantum Efficiency (QE) are 2-10x improved in peak and red spectral response, respectively, compared to bulk APS imagers. Dark current tests on photodiodes and pixels indicate a periphery-dominated and voltage-dependent leakage current of 5-20 nA/cm^2 at 3V. Pixel linearity error of $\sim 4\%$ is observed at 80% of saturation. Test results indicate directions for further reduction of the dark current.

Introduction

In spite of spectacular progress in making large format imagers using bulk-CMOS foundries,^{1,2} several major challenges remain for the conventional CMOS APS technology. The limitation that the photodiodes have to be built together with the continuously scaling down CMOS devices has prevented APS imagers from achieving the high performance of their CCD counterparts.³

SOI can provide ideal solution for high performance APS. Besides the features of low capacitance (resulting in high conversion gain), small threshold modulation, (meaning high dynamic range), and radiation hardness, it can provide separate sites for MOSFETs and photodiodes, so that to meet their conflictive material requirements simultaneously.

We have previously reported on photoresponse from SOI-based photodiodes using "inside-the-BOX" approach.⁴ Subsequently, others have reported on a similar structure, but with low quantum efficiency and large dark current.⁵ In this paper, we present the design and process optimization to improve both QE and dark current. In order to verify efficacy of the structure and process techniques, several different types of pixels with different implant placements, various cathode area and perimeters have been implemented.

Structure and Process

Shown in Fig. 1 is the typical structure of the pixel.

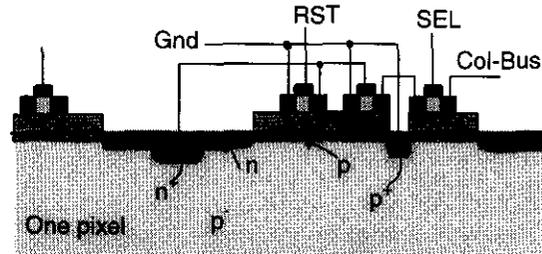


Fig. 1 Structure of the improved SOI APS pixel. The n^+ region, which is cathode of photodiode, is surrounded by shallow and low dose n-type doping. The other surface area of the handle-wafer is implanted with p-type "pinning" doping for eliminating surface effect on dark rate.

Unibond SOI wafers with low handle doping ($6.5 \times 10^{12} \text{ cm}^{-3}$) are used. P-type and n-type surface doping with typical surface densities from 10^{17} to 10^{18} cm^{-3} are introduced to maintain equilibrium for the surface, so that to eliminate the dark current caused by interface generation-recombination. Back-gate effect can also be effectively reduced by this measure.

Conventional partially-depleted SOI technology was slightly amended to enable the new structure. Shown below in Fig.2 are the main revision steps of the process flow. The boron "pinning" doping is implemented prior to all the other steps so it causes no interference to the process. Window (BOXCUT) opening through the buried oxide needs an additional lithography step. Shallow n-doping is followed by it, but the p+ and n+ doping are implemented together with the drain/source of MOSFETs.

Results

Shown in Fig. 3 are results of Athena and Atlas simulation for the photodiode's doping profile and potential distribution. The over 20 μm depletion region depth leads to a remarkably improved QE curve ranging from 400 nm to over 1000 nm, as shown in Fig. 4. Considering the fill factor of the test structure, the inner QE is close to 1 at visible band. The dark current of photodiodes is about 5-15 nA/cm^2 at 3V. As shown in Fig. 5, the dark current exhibits clear cathode perimeter dependence, indicating strong possibility for further improvement. Fig. 6 is the linearity and mean variance curves obtained in conversion gain test.

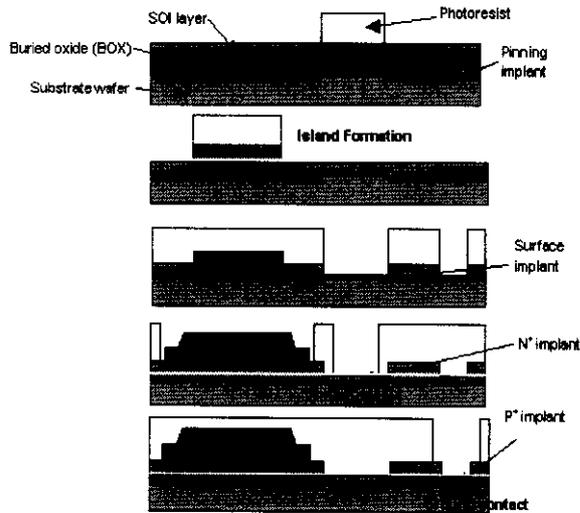


Fig. 2 Key steps for incorporating the photodiode into the SOI process flow

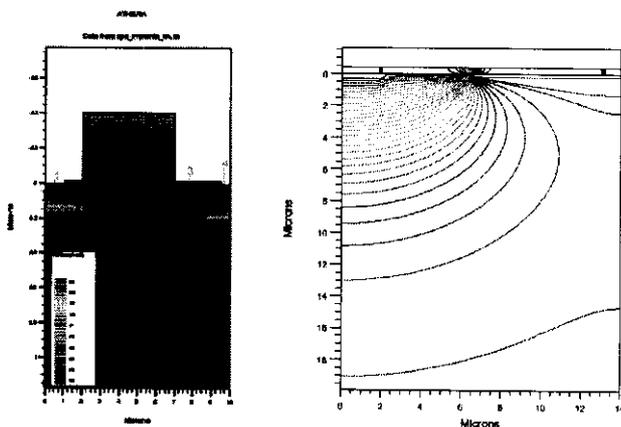


Fig. 3 Simulation results for doping profiles (left) and potential diagram of the photodiode (right, cylindrical coordinates)

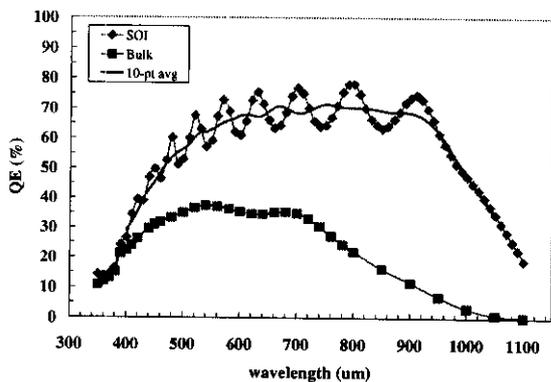


Fig. 4 QE of SOI photodiode (oscillation is caused by transmittance of 2 μm thick oxide) compared to bulk APS

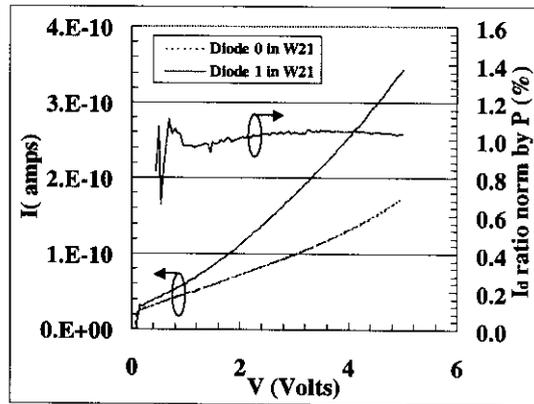


Fig. 5 Dark currents from two photodiodes with different cathode perimeters (P)

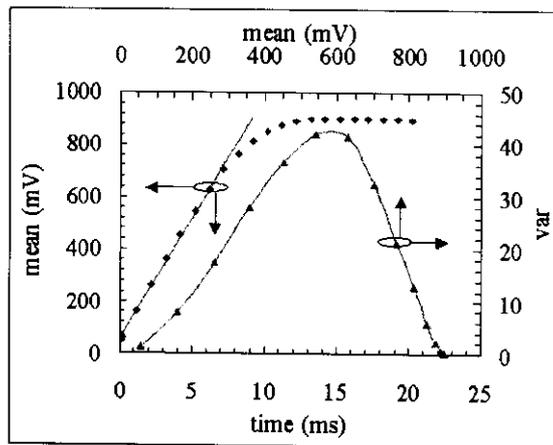


Fig. 6 Linearity and mean variance curve for conversion gain test.

Conclusion

We have demonstrated a novel SOI APS structure with broad response and high QE. Technology revision is insignificant and easy to realize. Dark current of photodiodes built at high resistivity handle-wafer is at an acceptable level. Analysis shows that it can be largely improved by optimizing the technology condition for surface doping.

References

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