Solder Joint Fatigue Study Under Low Temperature Martian Conditions

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Abstract—[1,2] Electronics, without requiring heater power or enclosure in a centralized "warm electronics box," will need to survive mean surface temperatures of -120°C to +20°C for an extended (>2 years) Martian mission and an operational temperature up to 85°C. These surface temperatures range over one Martian day or typical cycle. Since the electronics will need to survive extended thermal cycles (3x life of 2010 cycles) under these conditions, thermally induced fatigue is a significant concern. The solder joint reliability of connectors with Sn60Pb40 finish and In80Pb15Ag5 solder on a printed wiring board was investigated. Between 638 to 1431 cycles from -120°C to +85°C, a small number of leads failed on a printed wiring board with a silicone conformal coating. Scanning Electronic Microscopy analysis revealed crack initiation at the lead finish and In80Pb15Ag5 solder interface in at least one case with martensitic phase transformation of tin/lead solder and the loss of ductility in the tin phase at low temperatures as the failure modes. Another failure region was composed of several intermetallic compounds with intermetallic embrittlement as a failure mode. This fatigue study determines the corresponding failure modes of the thermally stressed components at each failed interface.

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1. INTRODUCTION

Traditionally the electronics on Mars mission rovers have been centrally located and enclosed in a heated enclosure known as a "warm electronics box" (WEB). The WEB protects the electronics from the large temperature excursions present in the Martian environment, where the mean average surface temperature fluctuates from -120ºC to 20ºC over the period of one Martian "day" (SOL[3]).

A distributed, non-heated architecture is being pursued on the electronics of rovers to be used in future Mars missions. In this architecture, the electronics, consisting of low cost, commercially available, and space qualified electronic packaging assemblies, are placed close to the system they interact with (thus the term distributed) and are no longer confined in heated enclosures.

These electronic packaging assemblies will have to operate and survive in an electronics functional range of -120ºC to 85ºC (including margin) for an extended mission of 670 Martian SOLs. A 3x life thermal cycle test of 2010 cycles from -120ºC to 85ºC (including margin) is required to qualify the electronics packaging and investigate reliability and robustness. Under these conditions thermally induced fatigue and the low temperature environment have been identified as high risk potential failure modes, as the required thermal cycle temperature range of -120ºC to 85ºC and the required number of cycles (2010) exceeds the typical Mil-Spec rating of -55 °C to 125°C for a few hundred cycles.

2. BACKGROUND

Extreme fatigue conditions can affect the reliability of the joints or component attachments within the electronics packaging assembly. Solder and solder joints have a large number of potential failure modes as they must perform a combination of mechanical, electrical and material property functions flawlessly over an extended period of time. In the particular case of tin-lead (SnPb) solder joints used in low temperature Martian conditions, the main failure modes are creep, low cycle fatigue, degradation of the mechanical properties of the solder at low temperatures and martensitic phase transformation between the phases within the solder.

1 0-7803-9546-8/06/$20.00© 2006 IEEE
2 IEEEAC paper 1310, Version 7 , Dec. 9, 2005

3 One SOL is approximately 24 hours and 38 minutes

The solder experiences strain due to the difference in coefficient of thermal expansion (CTE) between the printed wiring board (PWB) and the component, and the large temperature excursions [1]. Although thermally induced stresses due to the difference in CTE would seem to dominate, significant thermally induced local stress within the eutectic lattice are developed due to the mismatch between an isotropic α-lead (Pb) cubic crystal structure (f.c.c.) and the anisotropic β-tin (Sn) body-centered tetragonal (b.c.t) structure[2].

Martensite is known to form during quenching of austenitized iron-carbon alloys through a diffusionless process [3]. Rapid cooling causes atomic movement within the austenite f.c.c unit cell and transformation to a single phase of martensite with a b.c.t unit cell. Since Sn-Pb solder has the same unit cell structures, it is strongly suggested that a martensitic transformation can occur. SnPb solder has the same unit cell structures as austenite (f.c.c.) with α Pb-phase and martensite (b.c.t) β- Sn-rich phase [2]. Under low temperature conditions below -110ºC, the tin phase becomes brittle [2].

Crack growth and propagation may occur in the intermetallic phase, or at the interfaces, which form the bonded joint. A primary crack at the package-solder interface and a secondary crack at the solder-board interface are known to form in Ball-Grid Array (BGA) joints [4]. Fatigue cracks are also known to form underneath surface mount leads on Thin Small Outline Packages (TSOPs) under thermal shock conditions [4].

In [5], the fatigue crack growth occurred at the intermetallic compound and Sn63Pb37 bulk solder interface after thermal cycling from -35ºC to 125ºC due to shear stress from CTE mismatch between the board and chip carrier. It is known that intermetallic compounds are typically more brittle than bulk solder [1,6], thus fatigue crack growth is likely to occur in the intermetallic compound due to joint embrittlement [2].

3. PACKAGING MATERIALS SELECTION

The 37- pin Nanonics Dualobe® connector[4] (nano-connector) with surface mount BeCu (UNS C17200, TM02 Temper per ASTM B194) leads was chosen with a standard Sn60Pb40 finish over a Cu strike per SAE-AMS-C-81728. The following packaging materials were chosen after an extensive materials selection process, and survivability results from thermal cycling (-120ºC to 85ºC) chip-on-board assemblies in [7,8]. In80Pb15Ag5 solder (Indalloy #2-Indium Corporation) was selected because of its thermal fatigue resistance and minimized leaching when soldering to Au.[5] Dow Q1 4939 1:10 silicone coating was chosen for its high compliance and function as a good moisture barrier. The polyimide printed wiring board (PWB), as an organic material, has optimal material properties. It is commonly used in space applications.

The packaged assembly of the nano-connector soldered to the polyimide PWB is shown in Figure 1.

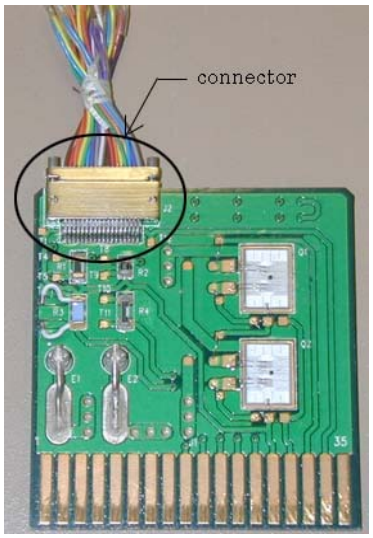

Figure 1: Nano-connector soldered onto a polyimide PWB

4. TEST VEHICLE DESIGN, ASSEMBLY, TESTING

The nano-connectors with surface mount leads were attached to polyimide PWBs. The 8- layer polyimide PWB had a thickness of 1.60 mm +/- 0.127 mm. The PWB had wire bondable Au plating (1.016-1.524 μm) at 99.97% purity with a Ni underplate (2.54 – 5.08 μm) per SAE-AMS-QQ-N-290 Class 2, over a top Cu layer (~107 μm). A hot soldering iron at approximately 260°C was used to solder the In80Pb15Ag5 wire which has a liquidus temperature of 154°C for a few seconds [9]. Prior to soldering the nano-connector leads onto the Au pads with Indalloy Tacflux 012 RMA (Rosin Mildly Activated) flux from Indium Corporation, the leads and Au pads were pre-tinned with In80Pb15Ag5. The polyimide PWBs were cleaned with ethyl alcohol and brushed carefully. Dow Q1-4939 1:10 silicone coating was applied and cured at 80°C for 4 hours [9]. Continuity measurements were taken before and after conformal coating. The test vehicles were thermal cycled in the environmental test chamber, Tenney Model T6C-LN2, as shown in Figure 2. Each cycle, programmed between -130°C to 92°C, averaged a 5°C/minute ramp rate. Figure 3 shows a thermal cycle temperature profile of four thermo-couples that were used to ensure each test vehicle was subjected from -120°C to 85°C. The test vehicles were thermal cycled between -120°C to 85°C and held at each temperature for at least 10 minutes.

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[4] Personal Communication with Scott Cairns at Tyco Electronics

[5] Master Solder Alloy Properties Table, from the Indium Corp.website<http://www.indium.com/products/oldalloychart.php> accessed November 2, 2004

Figure 2: Tenney Model T6C-LN2 Environmental Chamber

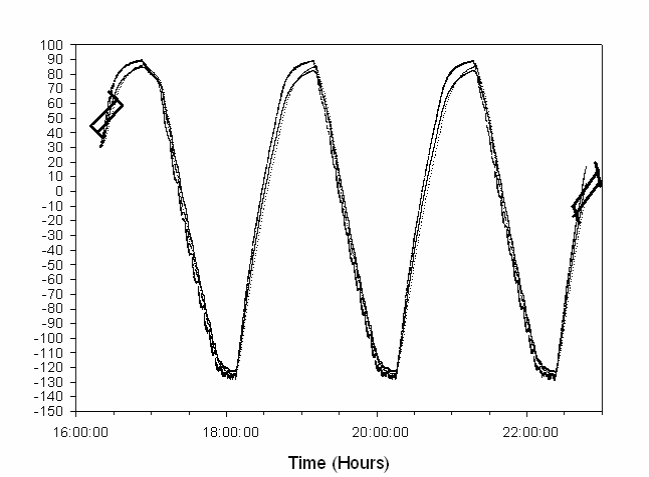

Figure 3: Thermal cycle temperature profile

The nano-connectors were continuously and periodically manually verified for functionality. For the purpose of this paper, the manual measurements are presented. The 37-surface mount leads on the nano-connector were daisy chained to form a continuous circuit as shown in Figure 4. Measurements continued every 250-300 cycles after an initial manual measurement at 500 cycles. High resistance values or infinity indicating electrical opens were defined as failures. For a statistical analysis, the number of nano-connector lead failures was calculated. The plug attached to the connector body was removed and the lead pairs were probed. Under high magnification, each lead of the pair was inspected for cracks in order to determine the failed lead. Failures due to assembly defects and handling were eliminated from this analysis.

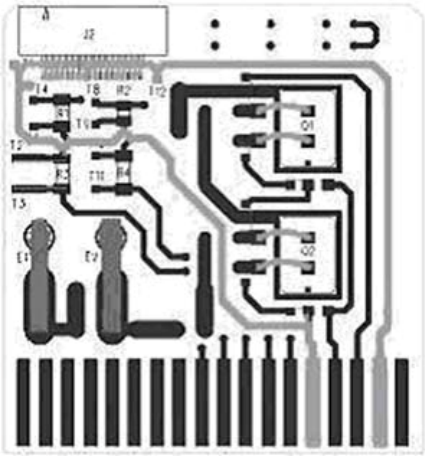

Figure 4: Nano-connector circuit

After functionality measurements and a visual inspection were performed, the failed components were analyzed using Scanning Electron Microscopy (SEM). A selected sample was cross-sectioned, potted, and analyzed using the Hitachi S-4500 and LEO, Zeiss Supra 50 VP, scanning electron microscopes (SEM) with an IXRF Systems Energy Dispersive Spectrometer (EDS) elemental X-ray analyzer.

5. RESULTS AND DISCUSSION

Between 638 and 1431 cycles, nano-connectors with In80Pb15Ag5 solder and Dow Q1 4939 1:10 silicone coating on polyimide exhibited open circuits. During this period, a total of 13 out of 1110 lead contacts on 4 out of 30 nano-connectors failed with this specific material combination. Optical and Scanning Electron Microscopy (SEM) results have indicated that lead lifting was the cause of the open. The actual cause of failure was due to micro-cracking. Figure 5 shows a top view of a lead and subsequent cracking along the interface of the foot and the Au pad which failed between 638 and 863 cycles.

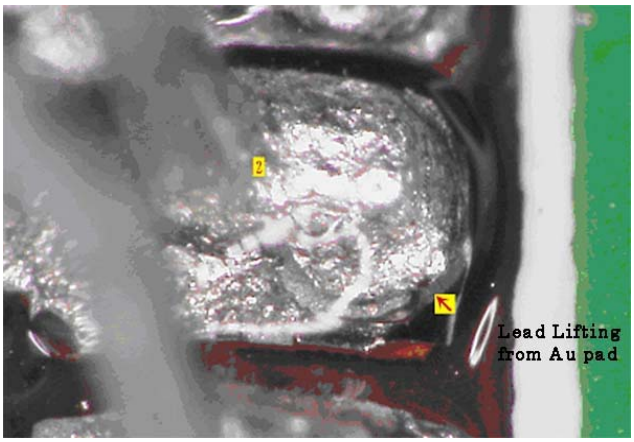

Figure 5: Top view lead lifting on PWB- P048 at 175x

A cross-section of a lead that did not fail in Figures 6 and 7 revealed a probable crack initiation site at the Sn60Pb40 lead finish and the In80Pb15Ag5 solder interface in at least one case. It appears that the crack began in the lead finish and propagated into the In80Pb15Ag5 solder or possible intermetallic that formed at that interface. This particular crack is underneath the lead toe, however, the failed lead in Figure 8, with a magnified backscatter image in Figure 9, showed the crack propagated through this interface at the heel or highest stress point on the package. This corresponds to the primary crack propagation from the heel of the TSOP solder joint [4].

Crack initiation in the lead finish may have occurred due to a martensitic phase transformation which resulted in a Sn-phase at low temperatures down to -120°C. Local stresses and volume changes within the microstructure due to phase transformation to a Sn rich phase (b.c.t) and loss of ductility of the Sn phase caused the failure. It is suspected that both mechanisms caused crack propagation and separation of the interface. It is undetermined if the crack began in the Sn-phase, but most likely occurred due to both failure modes.

A secondary crack propagated at the In80Pb15Ag5 solder and PWB interface as shown in Figures 9. This crack propagated into the second failed region in proximity to the Cu/Ni/Au (1.016-1.524 µm) plating interface. It is possible that the fatigue failure occurred at this interface due to fatigue stress. Repetitive thermal cycling caused cyclic strains in the solder joint mainly due to the magnitude of the change in temperature of 205°C and the difference in CTE between the BeCu lead, In80Pb15Ag5 solder, and the PWB. Even though the BeCu lead and polyimide PWB have closely matched CTE of 16.7 ppm/°C[6], and 16.50 ppm/°C in the x, y-direction [10], respectively, the In80Pb15Ag5 solder has a CTE of 28 ppm/C[7].

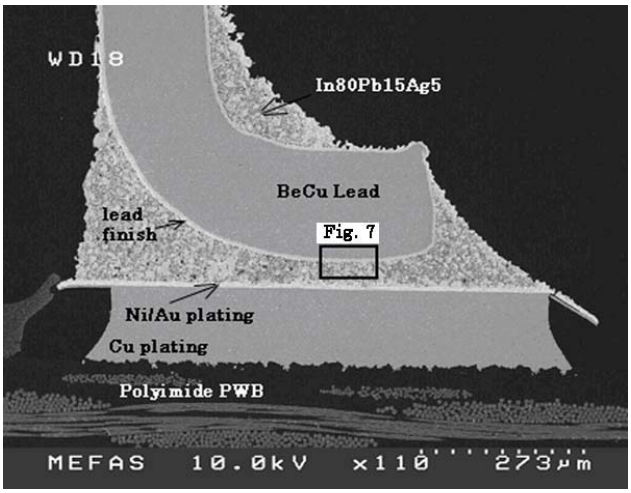

Figure 6: SEM cross- section of a lead that did not fail at 10x and 10kev

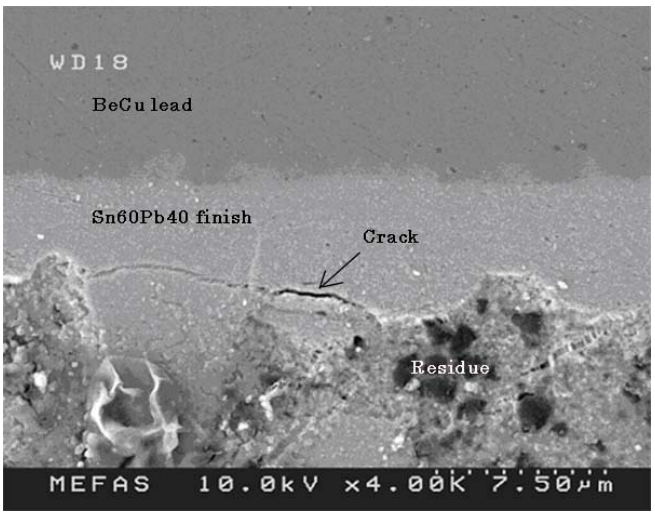

Figure 7: SEM cross- section of probable crack initiation site at 4kx/10keV (inset from Fig. 8)

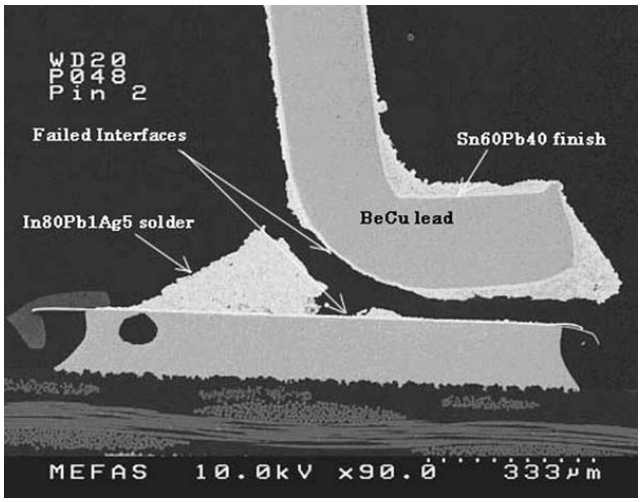

Figure 8: SEM coss- section of failed lead at 90x/ 10keV

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[6]Beryllium Copper, UNS C17200, MatWeb website , http://www.matweb.com/search/SpecificMaterial.asp?bassnum=NBB486

[7] Master Solder Alloy Properties Table, from the Indium Corp. website < http://www.indium.com/products/oldalloychart.php> accessed November 2, 2004

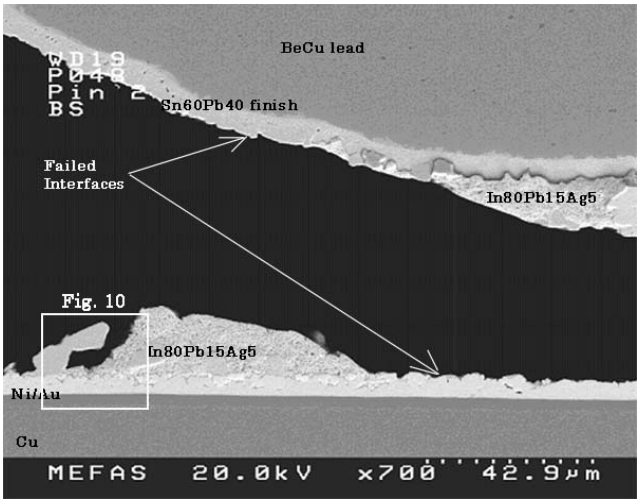


Figure 9: Back-scatter image of failed interfaces at 700x/20keV

Figure 10 shows a magnified view rotated 90 degrees from the inset in Figure 9 of the area of interest where the crack propagated through intermetallic compounds. Due to these extreme temperature excursions, delta CTE between the lead, solder, and PWB, and known brittle nature of intermetallics [1,2,6], cracking could have occurred through one of the identified compounds. Figure 11 shows the area under an increased magnification. Figure 12 shows the inset in Figure 11 under 10.10kx magnification with 7 distinct regions where EDS Spectra were taken.

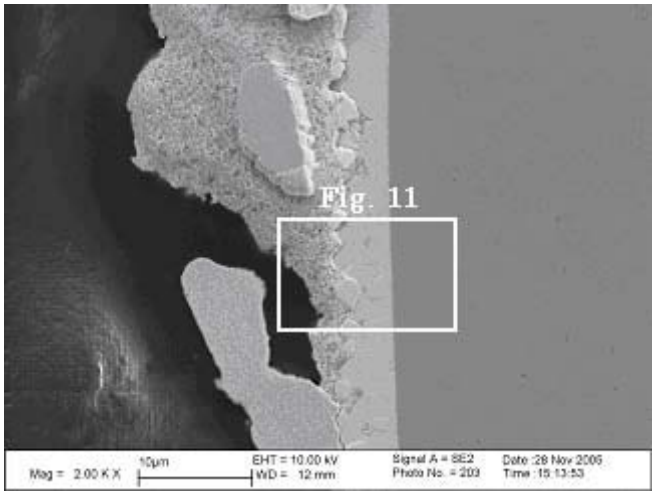


Figure 10: Magnified view of inset in Fig. 9 at 2kx/ 10keV

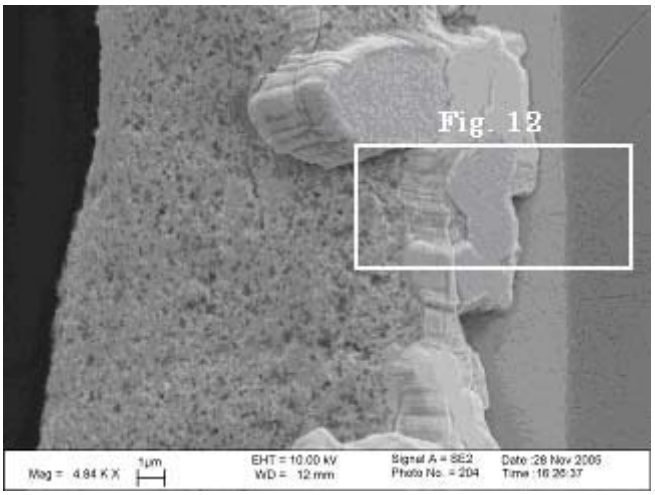


Figure 11: Magnified view of inset in Fig. 10 at 4.84kx/ 10keV

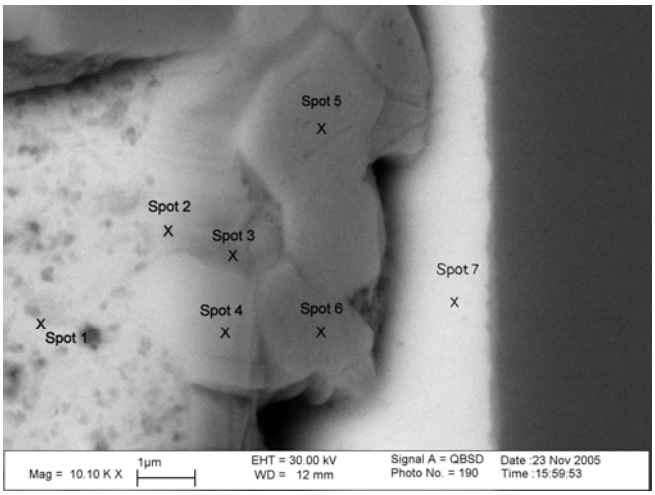


Figure 12: EDS spot scan locations- magnified view of inset in Fig. 11 at 10.10kx/ 30keV

EDS Spectra (all with ZAF correction factor) on the 7 spots defined in Figure 12 were taken at 20 second spot scans since In and Sn were convoluted and a short time interval clearly distinguished the peak intensities. The theoretical interaction volume is approximately 2um, so several spot scans were taken for the best resolution. The X-ray detector azimuth angle was at 45°, tilt at 0° and take-off angle at 25°. Scans were taken at 30keV, 10.10 kx, and a working distance of 12mm. In, Ag, and Sn were at Lalpha. Au and Pb were at Malpha, and Ni, Cu, and Al were at Kalpha. Figure 13 shows one example of the EDS Spectrum with high peak intensities of In-Pb-Sn. at Spot 1. Al was disregarded since it may have been found on the specimen due to sample preparation.

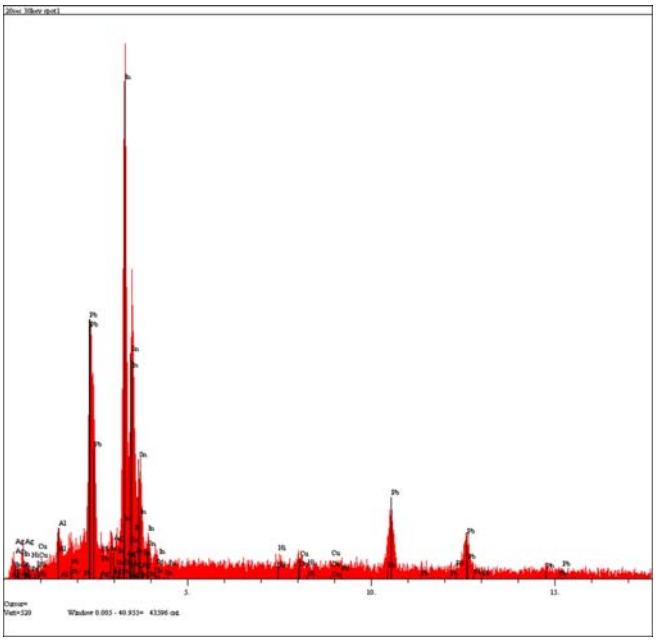


Figure 13: EDS Spectrum at Spot 1 at 30 keV

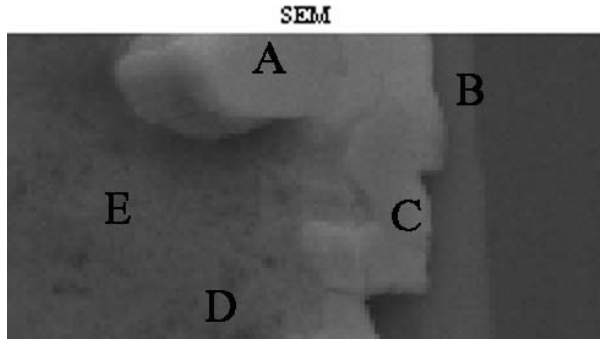


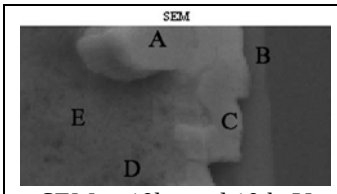
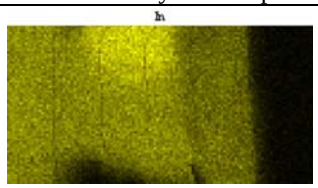
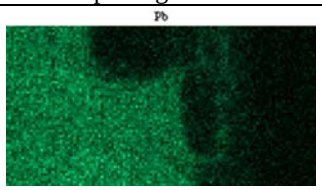
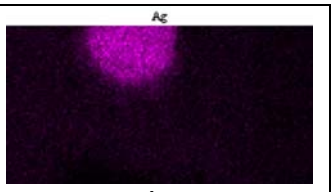
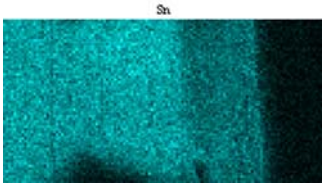
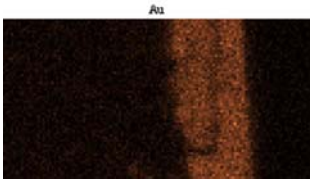
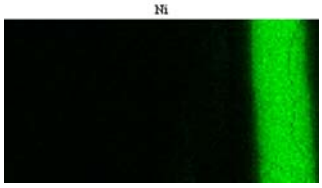
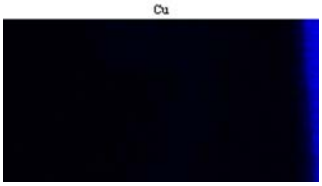
Figure 14: SEM X-Ray map of area of interest at 10kx/10keV

According to the EDS spectra, several intermetallic compounds were found at different spot locations. $In_xPb_ySn_z$ compound was detected at spot locations #1-3 and 6. Locations #4 and #5 revealed a In_xPb_y compound. A compound of $In_xAu_ySn_z$ was found at location #7.

A dot map confirmed additional intermetallic compounds at this interface. This dot map was scanned at an 8 micro-seconds time constant for 14 minutes, as shown in Figure 14 at 10kx and 10keV. Table 1 shows the X-ray dot map elemental data for each element in the region. It appears that Sn has diffused throughout the region and has formed several intermetallic compounds. There is an abundance of Sn because it is convoluted with In, so the Sn and In X-ray dot maps look very similar.

Figure 14 which corresponds with the dot maps in Table 1 is defined into selected regions A- E. Region A, not defined in Figure 12, illustrates a $In_xAg_ySn_z$ compound. Region B which also is defined as location #7 in Figure 12 confirms the same intermetallic, $In_xAu_ySn_z$. Region C and location #6 illustrates an $In_xPb_yAu_z$ compound. Region D suggests a single Pb area. $In_xPb_ySn_z$ compound is illustrated in Region E as in location #1 of Figure 12. The intermetallics found at spot location #2 and 3 are also shown in the same areas of the dot map. The dot map shows that Sn may have formed with In_xPb_y found in the EDS spectra on locations #4 and #5, or it may be unlikely since In and Sn are convoluted.

Table 1: EDS Elemental X-Ray Dot Maps at solder and plating interface at 10kx and 10 keV

 SEM at 10kx and 10 keV	 In	 Pb	 Ag
 Sn	 Au	 Ni	 Cu

It appears that two complexes of the Au-Sn intermetallic formed as well. Figure 15 details the Au –Sn area of the dot map. Within the region defined on the top, two different bands of the Au-Sn complex formed as illustrated on the bottom dot map. Therefore, Regions B and C defined in Figure 14 also contain complexes of this intermetallic.

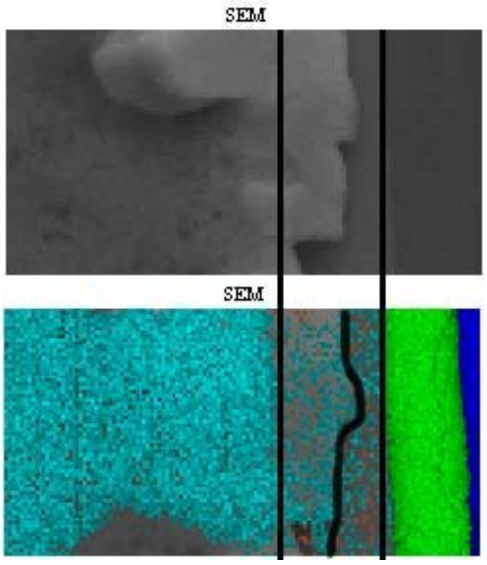


Figure 15: Detailed Dot Map of the Au-Sn Complexes

At a magnification of 5kx, other intermetallics were found as shown in Figure 16. EDS Spectrum (with ZAF correction factor) of Locations 8 and 9 revealed phases of In_xAg_y in Region 8 and $In_xPb_ySn_z$ in Region 9.

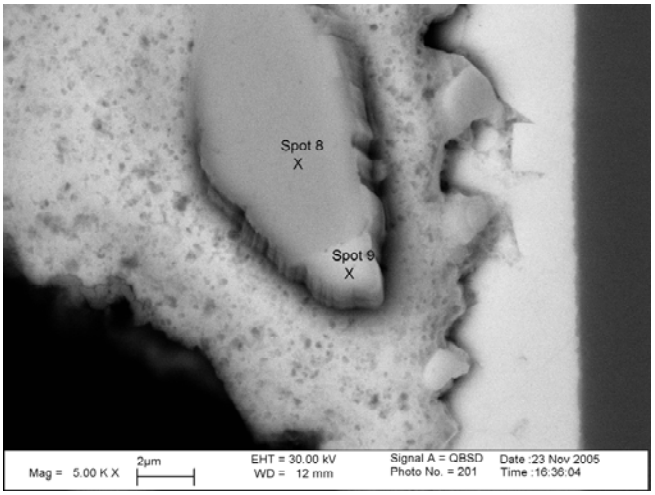


Figure 16: Location of Additional Phases in Region at

Overall, an assortment of intermetallic compounds was found at the solder/plating interface through the EDS spot location and dot map analysis. The data suggest that Sn is integral in intermetallic formation with In80Pb15Ag5 solder and the Au plating. Since it is known that this Sn phase becomes brittle at cold temperatures and intermetallic compounds are typically more brittle than bulk solder [1,6], brittle crack growth and propagation occurred at this interface.

6. CONCLUSIONS

The effect of thermally induced fatigue on the nano-connector lead solder joint has been studied. The analysis proved the nano-connector leads with Sn60Pb40 finish soldered to polyimide PWB with an In80Pb15Ag5 alloy failed due to lead lifting initiating between 638 – 863 cycles. Several conclusions have been made regarding the failure modes at each interface:

- The lead failed due to primary crack propagation at the lead finish near the heel which is the highest stress propagation, and secondary crack propagation at the solder/plating interface.
- Crack initiation most likely occurred in the Sn phase at the primary crack site, Sn60Pb40 lead finish, due to the martensitic phase transformation and brittle nature of Sn at low temperatures.
- The failure mode at the In80Pb15Ag5 bulk solder and PWB occurred due to cracking through the brittle intermetallic compounds.
- Several intermetallics at the solder and plating interface were found with intermetallic embrittlement as the failure mode.

7. FUTURE WORK

A more detailed intermetallic analysis of the Sn60Pb40 lead finish is recommended for future work in order to study and confirm the Sn phase involved in the crack initiation site.

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[10] Internal JPL verbal communication- Results of TMA testing

BIOGRAPHY

Carissa Tudryn began working at JPL in September 2004. She is a Mechanical Engineer in the Advanced Electronic Packaging Group. She has a Bachelor in Mechanical Engineering from The Catholic

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