

Impact of Junction Temperature on Microelectronic Device Reliability and Considerations for Space Applications

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Abstract

The space community and other high reliability users of microelectronic devices have been derating junction temperature and other critical stress parameters for decades to improve device reliability and extend operating life. Semiconductor technology scaling and process improvements, however, compel us to reassess common failure mechanisms and established derating guidelines to provide affirmation that common derating factors remain adequate for current technologies used in high reliability space applications. It is incumbent upon the user to develop an understanding of advanced technology failure mechanisms through modeling, accelerated testing, and failure analysis prior to product insertion in critical applications. This paper provides a summary of an industry survey on junction temperature derating from key microelectronics suppliers, and offers recommendations to users for temperature derating for reliable operation over time. Background information on established derating factors, and recommendations for safe operating junction temperatures for newer technologies are also presented.

Background

Established industry derating guidelines published by RAC (Reliability Analysis Center) [1] and NASA JPL (Jet Propulsion Laboratory) [2] provide users of commercial, as well as mil-spec microelectronics, derating factors for critical device parameters intended to reduce the occurrence of stress related failures in the intended application. Complex microcircuits with improved functionality, higher speed and lower core voltages continue to be sought after for characterization testing and product infusion in high reliability space applications; silicon process feature sizes of 0.18 micron are more common in these newer technologies. As feature sizes diminish, there are a number of intrinsic failure mechanisms, those that are inherent in the design and/or materials, and extrinsic failure mechanisms, or process related defects, that the user must remain cognizant of in their reliability assessment of advanced technologies. The primary intrinsic wearout failure mechanisms of concern continue to include: 1) Electromigration – a mass transport induced wearout mechanism in which metal atoms are diffused along an interconnect; 2) Time-dependent dielectric breakdown (TDDB) – wearout damage to the silicon dioxide dielectric film in a device through constant applied voltage and high, but still within specified operating range, electric field; and 3) Hot carrier aging – the degradation of MOS device characteristics due to charge trapping in the gate dielectric. Limiting stress levels on devices by reducing in the application can help offset some of the device wearout mechanisms.

Survey Results

An industry survey was performed with eight major microcircuit suppliers to the military/aerospace market. Primary questions and supplier responses are provided in Appendix A. The objective of the survey was to solicit feedback on current product regarding targeted product lifetime, product lifetime validation methodologies, activation energies, life limiting failure mechanisms, and the preferred, or most effective, screening regimen to identify weak devices, i.e. burn-in or high voltage stress test. Data is reflective of silicon process feature sizes as small as 0.18 micron. A summary of the supplier feedback follows. [3]

All suppliers in the survey continue to rely on the Arrhenius methodology for current product lines to determine acceleration factors for failure rate calculations and equivalent stress testing protocols. Through accelerated testing, the user is able to reduce the time to failure and obtain data in a shorter time than would otherwise be required. This technique remains widely used throughout the semiconductor industry. The rate at which many diffusion based chemical processes take place is governed by the Arrhenius equation:

$$R = A \exp(-E_a/kT)$$

where

R = rate of the process
A = a proportional multiplier
E_a = activation energy, a constant
k = Boltzmann's constant, 8.6x10⁻⁵ (eV/K)
T = Absolute temperature in Kelvin

Experimental data obtained from accelerated tests at elevated temperatures are based on the Arrhenius equation to obtain a model of device behavior at normal operating temperatures. Rearranging the Arrhenius equation allows the temperature dependence of device failure to be modeled as follows:

$$\ln t_2/t_1 = E_a/k (1/T_2 - 1/T_1)$$

where

t_{1,2} = time to failure
E_a = activation energy in electron volts
T = absolute temperature in Kelvin

Activation energies that are empirically representative of established technologies range from 0.7 to 1.0 eV for Bipolar processes and 0.5 to 0.7 eV for CMOS processes, hence many have adopted 0.7 eV for all diffusion-based failure mechanisms combined. Some of our survey respondents however have

experimentally and empirically demonstrated E_a of 0.4 eV for metal migration with new technology ASP/DSP CMOS 0.18-micron processes and 0.3 eV for DRAM gate oxide integrity. [4] Users should be cautious when applying generic activation energy standards to new technologies, as they may not be representative of current failure mechanism processes.

Other stresses used to accelerate device failure mechanisms include voltage, current, humidity and temperature cycling. Elevated voltage stress testing at wafer level probe is recognized as a more effective technique than temperature acceleration to detect oxide related defects. However, most suppliers in our survey rely on temperature acceleration in conjunction with voltage stress testing to provide a comprehensive assessment of their product. Voltage acceleration is based upon the McPherson model and the corresponding voltage acceleration factor, β , is empirically derived for each device family or technology.

Product life limiting failure mechanisms are highly technology dependent. Electromigration and TDDB are reported to be the most commonly experienced life limiting failure mechanisms in our study; hot carrier effects are becoming more of an issue with smaller feature sizes.

Most suppliers in our survey use product life testing at, or near, maximum junction temperature of the device to validate product lifetime; this is typically performed at 125 to 150°C. Target product lifetimes for mil-product are generally 10 years at maximum rated junction temperature, however, some designs are customer driven and reflect a 15, 20 or 25 year target product lifetime. There are varying product lifetime definitions from the suppliers in our survey therefore the user should request the specific test conditions and confidence level associated with a given FIT rate. Supplier responses for target FIT rates ranged from 50 FIT (0.5% cumulative failure rate) at 10 years and 60% confidence level, to 0.76 FIT (0.01% cumulative failure rate) at 15 years and 60% confidence level. One (1) FIT over 10 years for intrinsic failure mechanisms (0.01% cumulative failure rate) at 10 years and 60% confidence level is the historical benchmark. Therefore, we consider typical microelectronic lifetime for mil-products to be 10 years at maximum rated junction temperature unless otherwise defined. FIT rate calculations and targeted product lifetimes should be considered when using new technologies in high reliability applications. It is assumed that these failure levels are acceptable in electronic systems.

Tj Baseline Calculations and Temperature Stress Derating Curves

Historically, junction temperature (T_j) derating for silicon microcircuits in ceramic hermetic packages has been limited to between 110°C and 115°C. The basis of this calculation can be described as follows:

$$MTTF \propto e^{-E_a/kT}$$

Assume a product lifetime of 10 years. Adding a safety margin of two, the target product lifetime in space is 20 years minimum, or twice the product's designed lifetime. In order to achieve twice the lifetime, the junction temperature must be lowered such that MTTF is twice the nominal value. Using the Arrhenius equation:

$$e^{-E_a/kT_{derated}} / e^{-E_a/kT_{nominal}} = 2$$

$$\text{or}$$

$$-E_a/k \times (1/T_{derated} - 1/T_{nominal}) = \ln 2 = 0.693$$

$$1/T_{derated} - 1/T_{nominal} = -5.96 \times 10^{-5} / E_a$$

If $T_{nominal}$ is 125°C, $T_{nominal}$ is 398°K,

The worst case derating represents the lowest activation energy in the range. In the past, 0.6eV to 0.7eV have been widely used.

Assuming an $E_a = 0.6$ eV,

$$1/T_{derated} - 1/T_{nominal} = -9.93 \times 10^{-5}$$

or

$$1/T_{Derated} = -9.93 \times 10^{-5} + 2.51 \times 10^{-3} = 2.61 \times 10^{-3}$$

$$T_{Derated} = 1/2.61 \times 10^{-3} = 383^\circ\text{K}$$

$$T_{Derated} = 110^\circ\text{C (Current JPL D-8545 Tj Value)}$$

Historical linear and digital microcircuit temperature stress derating curves are described in Figure 1.[5] A corresponding failure rate may be obtained at each temperature for established technologies which is helpful to the user in determining an acceptable failure rate for established technologies in a given application.

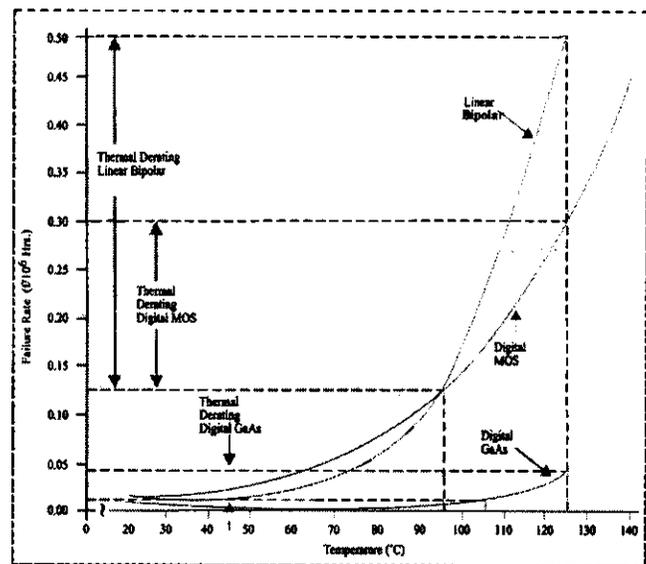


Figure 1. Linear/Digital Microcircuit Temperature Stress Derating Curves.

Summary and Recommendations

Many of JPL's current programs are operating, or will operate, in the 6-month to 15-year mission life range. Microelectronics applications in these missions vary in criticality, operating environment, and operating conditions. Therefore it is appropriate to consider these variables, in addition to current device technology trends, feature size, and failure mechanism activation energies when establishing a safe, adequate, operating junction temperature

for an intended mission application. Additional Tj calculations are presented in Figure 2.

Device Max Rated Tj	Activation Energy	Years of Operation	Derated Tj
125°C	0.3	10	125
	0.3	15	107
	0.3	20	96
	0.5	10	125
	0.5	15	114
	0.5	20	107
	0.6	20	110
	0.7	10	125
	0.7	15	117
0.7	20	112	
150°C			
	0.3	10	150
	0.3	15	130
	0.3	20	117
	0.5	10	150
	0.5	15	138
	0.5	20	130
	0.7	10	150
	0.7	15	141
	0.7	20	135

Figure 2. Junction Temperature Calculations.

While additional safety margin may be realized with lower operating temperatures, voltages and frequencies, the user should take in to consideration the supplier's basis for FIT rate calculations, the product lifetime design, and failure mechanism developments and trends in new technology product lines in the overall reliability assessment. Users of Commercial-Off-The-Shelf (COTS) components in high reliability applications utilizing plastic packaging techniques must also take in to consideration limitations of the Tg of the packaging material itself, as well as the flame retardant precipitation effect in the mold compound. Either one of these factors may override the safe operating junction temperature limit in a given application. Additionally, COTS designed lifetime may vary greatly depending on device type and the intended application. Hence, the user should not necessarily assume a 10 year designed lifetime at maximum rated operating temperatures for COTS products without verification.

Further research, modeling, accelerated testing, and failure analysis is recommended to better understand the correlation relationships of smaller feature sizes and device failure mechanism activation energies to more quantifiably assess the reliability of current device technology trends. In general, however, the results from this supplier survey indicate the following activation energies are more appropriate for determining derated Tj values for a given application:

Technology	Conservative Ea Value
Bipolar	0.7 eV
MOS - General	0.5 eV
ASP/DSP	0.5 eV
DRAM	0.3 eV

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References

- [1] Electronic Derating for Optimum Performance, Reliability Analysis Center under contract to Defense Supply Center Columbus (DSCC), p104 (2000).
- [2] JPL Derating Guidelines JPL-D-8545 Revision D, Jet Propulsion Laboratory under contract to National Aeronautics and Space Administration (NASA), pp 14-15 (2003).
- [3] JPL Internal Document 5141-03-053, Impact of Junction Temperature on Microelectronic Device Reliability, (2003).
- [4] Supplier Survey with eight major microelectronics suppliers, Appendix A (2003).
- [5] Electronic Derating for Optimum Performance, Reliability Analysis Center under contract to Defense Supply Center Columbus (DSCC), p106 (2000).

Appendix A Supplier Survey Results - Anonymous

Questions/Responses	Supplier A	Supplier B	Supplier C	Supplier D	Supplier E	Supplier F	Supplier G	Supplier H
1. Does your product line's life testing at various temperatures follow the Arrhenius Equation?	Yes	Yes	Yes, but we haven't proven the fit at the product level. Instead, we perform reliability tests at various temperatures on device structures for EMG and TOSB.	Yes. We use the Arrhenius equation to estimate the failure rate based on comparing the testing at accelerated temperatures.	Yes	We use in-line screening programs to measure early and long term failure rates, and look for defect related reliability problems. We do not consider the in-line screening program (e.g. typically 125C, 1MDE, clocking, over-voltage) as a measure of how long a device lasts before it reaches wearout. Roughly the in-line screening program or burn-in follows Arrhenius. Specific mechanisms (TOSB and electro-migration) can be more complicated.	Yes we use Arrhenius typically 110 degrees Celsius to 125 degrees Celsius data. However, we do see some non-Arrhenius phenomena.	Life testing performed on military and commercial product lines uses the Arrhenius equation to determine acceleration factors when calculating failure rates and alternate temperatures for stress. This model is only valid for failure modes that are chemically induced (ionic contamination, gas outgassing, etc.). The Arrhenius is not used for failures that are specific events in time (EOS, ESC, etc.).
2. Is life testing used at your company to validate product lifetime? Can you share information as to how this is done? At what temperatures have you performed your burn-in or life testing?	For new technologies we perform life test fit and typically use Weibull analysis and other tools to determine failure rates. Burn-in and life testing is typically performed at 125C to 150C.	Burn-in and life testing is typically performed at 125C to 150C. New Processes and New Packages are qualified using a maximum 3 lot (77 units per lot) testing for Early Failure Testing (EFT samples Operating Life Test Temp and Humidity Based Test Temperature Cycling Auto-Drive ESDM latch-Up Board Level Temp Cycle (for packages) Exponential	Yes. We perform life testing at junction temperatures = 150C for 1000hrs (or >= 150C for 500hrs) with and accept/reject criteria of DFI to validate product lifetime.	We perform operating life, usually at 125C, by using burn-in boards which have a typical application circuit. The circuit is designed to stress the device close to the maximum junction temperature specification.	Life-testing is performed to assess product reliability not only for the anticipated average life, but to assess the long-term performance of the product family. The usual stress conditions vary based on device design and user density. Burn-in and life test is normally conducted at +125C but a few products are run at +150C. Stress conditions for burn-in, life test and long term life test are the same for a given device being stressed. A dynamic stress pattern is used typically that will be a random set looped through a device using various frequencies to exercise the parts for the entire stress period. Parts are stressed at either 125C or 150C. We employ a 100C approved QML accelerated voltage approach for BJT, LVT and Long-life LT. The Arrhenius equation is used to calculate the acceleration factor using and activation energy of 0.32.	We verify product lifetime (e.g. product will have a failure rate before a certain amount at 10 years) by building up specific failure mechanisms, such as electro-migration, and setting design rules and technologies to avoid these mechanisms. These tests are done at very high temperatures (e.g. 200C for electro-migration). Burn-in and auto-latch screening program are done typically between 125C and 150C junction temperatures. The in-line measurement program can not apply the maximum current. Devices on the device to measure lifetime. With the increased operating junction temperatures, it is less able to give much temperature acceleration as well.	Yes, we use Arrhenius, typically 110 degrees Celsius to 125 degrees Celsius data. However, we do see some non-Arrhenius phenomena.	Life testing is not used to validate product lifetime. This would take too long. Life testing is used to validate that the infant mortality of a product have been reduced to an acceptable level as the probability of early life failures is very small. We cannot evaluate by highly accelerated testing on specific structures to look at specific wearout mechanisms. An example of this is the wearout mechanism of electro-migration. Highly accelerated stress consisting of high current densities and high temperatures are used to develop a degradation/failure model. This model is translated into design rules for a specific maximum operating condition. The design rules for this type of mechanism typically are a maximum current per unit width of metal line. When higher current are required in a line, the line is made wider.
3. What is your definition of product lifetime? We have heard that operating time until accumulated failure rate is 0.01%. What is your confidence level for the lifetime prediction?	The goal for electro-migration reliability is less than 0.01% cumulative failures during 10 years at a maximum junction temperature of 100C. Effectively 20 FIT with 90% confidence level. If you want to define it at 0.01% (1 FIT) the answer is 77,000 hours. For product rated above 100C junction, we perform EM calculations on a case by case basis with the above targets.	The qualification target is 100 FITS (Failure in Time). FITS depends on the device hours, acceleration factor, activation energy and if of failures. The MTBF (Mean Time Between Fail) is FITS.	>10yrs Criteria for device level characterization is <0.01% failure for 10yr equivalent at 125C.	The operating life testing is usually performed for 1000 hours at +125C. The confidence level is typically 90%, based on the exponential distribution, and is useful for comparing the reliability of similar products. Some customers request other confidence level such as 90% or even 95% and so we always offer to calculate FIT rates and MTBF for these requests.	QML V requirements for space level applications are generally considered 15 years. We typically demonstrate predicted lifetime at or below the 0.01% failure rate at 15 years using our 100C/2 approved QML accelerated life test approach. Based on our Long-life life-time testing of each product and family family we have data that is significantly better than the 0.01% FIT rate at 15 years. Normally, our FIT rate calculations are performed at the 90% confidence level.	Life-time definition is the average failure rate at the lifetime (e.g. 10 years) is less than 1 FIT. This is for lifetime failure mechanisms such as TOSB and electro-migration. 1 FIT over 10 years is the same as a cumulative failure of 0.01% at 10 years. 1 FIT = 0.01% (1/100,000) failures. Some packages 0.1%.	Depends on type of products.	This question is related to #2 above. Life testing does not validate product lifetime. Most semiconductor today have intrinsic lifetimes that are significantly long. The wearout point for a process/product is set by the wearout mechanisms (electromigration, dielectric breakdown, hot carrier degradation, device instability, etc.). These are set based on the process and design parameters. As said above the EM requirements are set by design rules. Early life failures are typically what is seen in Life Testing. These are defects caused by wafer fabrication or assembly that accelerate the aging process. The purpose of burn-in is to age these defects sufficiently to remove them from the shipping population thereby improving the reliability. The PDA (percent defective allowable) are also placed on burn-in to screen lots that have an abnormally high failure mortality. The failure rate we publish on our WEB site is based on determining the customer failure rate assumed after burn-in. It is typically calculated for a tenry of products built on the same wafer fab process. As with any electron
4. What is the range of Arrhenius activation energies that are empirically representative of various technologies made by your company?				Based on empirically obtained data, we use 1.0 eV for Bipolar processes and 0.7 eV for CMOS processes. Again, these are useful for comparison purposes. A review of industry publications correlates with these assumptions, however, some customers request other energies of activation such as 0.5 eV which we similarly offer to provide in our FIT and MTBF calculations.	For gate oxide integrity, the activation energy used is 0.32. Experiments have demonstrated that this is a valid number for oxides. For metal migration, the activation energy ranges from 0.4 to 0.8.	We do not have good data on the wear-out mechanisms. We have data for TOSB and electro-migration and other known wearout mechanisms (e.g. HBTI). However, since most reliability failures are defect related, these inherent wearout mechanisms are not all that useful. We have measured an activation energy of 0.54 eV for the typical silicon metalizations (back and metal contacts), and a voltage acceleration also. For long term lifetime failure rates, we use 1.1 eV, for all mechanisms lumped together.		Activation energies are tied back to the physical process underlying the failure and how temperature affects the process. In the case of electro-migration, temperature accelerates the damage done to the metal line. In the case of hot carrier reaction, temperature decreases the rate of trapping. HCI has negative activation energy. Its worst case condition is cold temperature. We use activation energies in the range of -1.0 eV to 1.0 eV depending on the dominant mechanism causing the failure.
5. What is your target product lifetime of the technologies made by your company?	See item 3	ML, Auto at 10 years	10yrs - while this is the criteria we have more headroom on our processes and have characterized some mechanisms for > 100yrs.	These are usually customer driven and 20 years seems to be the current consensus. Our product we typically far surpass this target, because of the conservative design rules and mature processes which we employ.	The QML V product life time target is typically 15 years, but can be proven or less depending upon the customer's requirements for mission lifetime.	Target lifetimes are 10 years for typical products, and 20 years for telecommunication.	From 7 years to 25 years.	This question must be referenced back to #2 and #3. The target lifetime is the wearout point. The mean for the process drives the wearout point (lifetime). Products that are going into consumer products (PC, handhelds, etc.) may have a shorter mission lifetime. These may be targeted at 3 to 5 years lifetime. Military products would have a longer lifetime target, typically 10 years. These targets assume worst-case conditions also. In reality the actual product lifetime may be significantly longer than the because it would not operate at the worst-case conditions for its entire lifetime.
6. What is the life limiting failure mechanism, for example, electro-migration, time dependent dielectric breakdown, or hot carriers?	This depends on the technology. Primarily EM and TOSB. Hot carrier effects are becoming more of a concern as geometries shrink such as the current 0.7 micron process.	Technology dependent. I am comparing burner classification	This is very dependent on the specific product design and process technology.	Again, based on actual data, we observe mobile ion contamination failure mechanisms for both Bipolar and CMOS processes and gate oxide related mechanisms for CMOS processes. Electro-migration hot carriers and other potential failure mechanisms are usually addressed during wafer fabrication by parametric analysis of special test structures on every wafer.	Electro-migration is typically the limiting failure mechanism. If a circuit is designed to operate at the maximum current density allowed based on Arrhenius QML and the specific wear failure design rules, EM will limit the product life more than the other failure mechanisms.	It depends on the technology. In the future technologies (i.e. see Culture by the way) electro-migration is the key.	EM and oxide, both	These are all examples of wearout mechanisms. Any one of them could cause the part to fail. The key is to make sure these mechanisms are not active until well after the product's useful life has been expended. New PC typically have a 3 to 5 year life before they are replaced. Designing a process with 30 year life would not allow you to be cost competitive with the competition.
7. What is the most effective screen of burn-in: elevated temperature or higher voltage?	For newer technologies we believe that accelerated voltage gives us the most effective screen. However, for new product technologies it is a combination of DFI at 125C for a short duration, say 4 hours combined with higher voltage. I know you are aware of other techniques such as 100C and V-STRESS testing to weed out potential reliability defects. For example, just burn-in 100C is a much better predictor of some defect mechanisms than going to data base.	We use both depending on the failure mechanism. e.g. For Oxide related failures it is high voltage and for oxide contamination it is high temperature.	This depends on the technology. Generally, voltage provides more acceleration for oxides (if the process permits) while temperature will accelerate other failure mechanisms.	We do not recommend burn-in screening because the designs are conservative and processes are controlled. Lifetime, the 100% electrical screens performed at wafer sort testing always include voltage screening of susceptible structures. Additionally, 100% Class test screening and QA release are performed using properly guard banded test limit ATE programs assures the Quality and Reliability of product.	Higher voltage is a much more effective screen for oxide defects than temperature.	We rarely use burn-in screening as the failure rates are fairly low, and burn-in screening can do some damage (EOS, wear levels, etc. from latch-up). High voltage stressing during test is the best, followed by high voltage at burn-in. Temperature is important for voltage is more so.	We use both and so we have apply not too high temperature or bias on the circuits.	It would not be reasonable to pick only one screen as the only screen to use. It really takes a battery of screens to evaluate a product's reliability. An integrated circuit is a complex mixture of silicon/polysilicon/metal/oxide. The package technology used for package and return the die is as important as the die itself. Special circuits would require different screens compared to CMOS. Bipolar circuits are primarily a current based device where MOS are voltage based devices. A combination of higher voltage and higher temperature provides a good screen for MOS devices provided you can apply the bias across all internal nodes (functional testing). Package related failures are usually caused by the thermal expansion mismatch between the components and may require temperature cycling to accelerate the failure.
Technology A	BIPOLAR 0.7 3.0	TLT Bipolar > 0.4		Bipolar = 1.0				
Technology B	MOS - GENERAL 0.5 3.0	CMOS > 0.7		CMOS = 0.7				
Technology C	ASIPROX 0.5 3.0	Linear & Transistor > 0.8	0.5 to 0.9 eV		Activation energy for gate oxides 0.32			
Technology D	GRAM 0.3 2.5							