

Evolutionary Recovery from Radiation Induced Faults on Reconfigurable Devices.

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ABSTRACT

Radiation Hard technologies for electronics are the conventional approach to for survivability in high radiation environments. This paper presents a novel approach based on Evolvable Hardware. The key idea is to reconfigure a programmable device, in-situ, to compensate, or bypass its degraded or damaged components. The paper demonstrates the approach using a JPL-developed reconfigurable device, a Field Programmable Transistor Array (FPTA) which shows recovery from radiation damage when reconfigured under the control of Evolutionary Algorithms. Experiments with total radiation dose up to 350kRad show that while the functionality of a variety of circuits, including a rectifier and a Digital to Analog Converter implemented on a FPTA-2 chip is degraded/lost at levels before 100kRad, the correct functionality can be recovered through the proposed evolutionary approach and the chips are able to survive higher radiation, for several functions in excess of total radiation dose of 250kRad. The Evolutionary Algorithms controls the state of about 1,500 switches that determine configurations on the FPTA-2 programmable device. Radiation damages the function, which is then recovered by the evolutionary process using a population of about 500 candidates and running for about 200 generations. Evolution is able to use the resources of the reconfigurable cells, even radiation damaged components, to synthesize a new solution.

1. INTRODUCTION

Long-life space missions and extreme environments have characteristics such as high radiation level (Europa Surface and Subsurface mission, 5 MRad), high temperature (Venus Surface Exploration and Sample Return mission, 460°C) and low temperature (Titan in-situ mission, -180°C). Such missions and environments have dictated the need for new electronics technologies.

Electrons and protons in space can cause permanent damage in electronic devices that can lead to operational failure. Particularly, Single Event Effects (SEE) are radiation induced errors in microelectronic circuits caused when charged particles lose energy by ionizing the

medium through which they pass, leaving behind a wake of electron-hole pairs. These events can be either transient and non-destructive (Single Event Upset) or hard and potentially destructive events (Single Event Latchup).

One technique for environments with high levels of radiation is the use of Radiation Hard technologies such as Silicon on insulator (SOI), that allows compensating for the effect of radiation. However, the fabrication cost associated with extreme environment electronics is high. In this paper we will present another technique, based on Evolvable Hardware, for electronic survivability in high radiation environments.

A reconfigurable chip developed at JPL, the FPTA-2 chip, is used in the experiment described in this paper [18]. We submitted this chip to radiation using JPL facilities, applying a total dose ranging up from 10kRads up to 75kRads at a time and a cumulative dose up to 350kRads. When the chip was back from the radiation chamber, the permanent radiation induced faults (single event latch-up) caused a deterioration in the behavior of some circuits (D/As, filters, rectifiers) previously downloaded/programmed onto the chip. We show that the correct functionality of these circuits can be recovered using Evolutionary Algorithms. The Evolutionary Algorithms control the state of about 1,500 switches. Using a population of about 500 candidates and after running the Evolutionary process for about 200 generations, the correct functionality is recovered. Evolution is able to use the resources of the reconfigurable cells, even the radiation damaged components, to synthesize a new solution.

The results indicate that using Evolvable Hardware technology we can design and develop electronic components and systems that are inherently insensitive to radiation induced faults by using on-board evolution in hardware to achieve fault-tolerant and highly reliable systems. The long term results of the proposed research would allow electronics to adapt to an extreme environment and long mission duration.

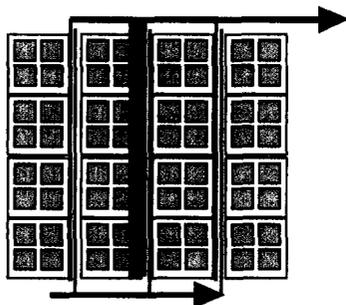
A number of researchers in the literature have examined the effect of radiation on CMOS devices. These could be

classified into those researchers who studied the effect of radiation on various cells and macro-blocks fabricated in silicon [1-7] or those who consider the design of radiation hardened components and cell libraries [8-12]. Work on studying the impact of radiation have considered custom implementation and those targeting conventional digital FPGA platforms such as Xilinx [13-17]. Here work has focused on studying both total dose radiation effects, where the effect is permanent, and Single Event Upsets (SEU)s, where individual bits in memory elements flip when exposed to certain quantity of radiation.

However, most of these researchers seem to have focused on technologies which are above 0.5 micron and hence the effects could not be generalized to devices implemented in the latest Deep sub Micron (DSM) technologies, where leakage currents dominate. In addition, no research has been carried out on the development of custom reconfigurable architectures implemented at transistor level hence enabling the implementation of both analogue and digital circuits.

This paper presents a framework for the development of radiation tolerant mixed analogue and digital circuits on a DSM reconfigurable CMOS device. Experiments are carried out in which the device is subjected to various radiation dosages, using an X-ray based radiation source, and the performance of the device is tested through the mapping a number of functional circuits. When the device fails any of the tests, an evolutionary algorithm is used to recover the functionality of the device where possible.

The rest of this paper is structured as follows: Section 2 describes the Field Programmable Transistor Array (FPTA) device architecture. Section 3 describes the



the data acquisition system. Section 5 provides an analysis of results obtained. Finally, the main conclusions of the work are listed in section 4.

2. FPTA ARCHITECTURE

The FPTA is an evolution-oriented reconfigurable architecture (EORA). Important characteristics needed by evolution-oriented devices are *total accessibility*, needed in order to provide evolutionary algorithms the flexibility of testing in hardware any chromosomal arrangements, some of which may be dangerous for existing commercial devices (may lead to internal bus allocation conflicts and burn the chip) and thus forbidden, *granularity at low level* (here transistor) allowing evolution to choose/construct the most suitable building block for certain system, and *transparency*, which enables users to have access to internal device information, etc.

The FPTA has a configurable granularity at the transistor level. It can map analog, digital and mixed signal circuits. The architecture is cellular, with each cell having a set of transistors, which can be interconnected by other "configuration transistors". For brevity, the "configuration transistors" are called switches. However, unlike conventional switches, these can be controlled for partial opening, with appropriate voltage control on the gates, thus allowing for transistor-resistor type topologies.

The architecture of the FPTA consists of an 8x8 array of re-configurable cells. Each cell has a transistor array as well as a set of programmable resources, including programmable resistors and static capacitors. Figure 1 provides a broad view of the chip architecture together with a detailed view of the reconfigurable transistor array cell. The re-configurable circuitry consists of 14

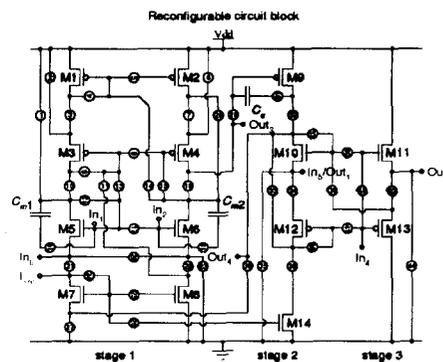


Figure 1: FPTA architecture (left) and schematic of cell transistor array (right). The cell contains additional capacitors and programmable resistors (not shown).

procedure followed during radiation tests. Section 4 describes the overall system architecture which includes

transistors connected through 44 switches. The re-configurable circuitry is able to implement different

building blocks for analog processing, such as two and three stages OpAmps, logarithmic photo detectors, or Gaussian computational circuits. It includes three capacitors, Cm1, Cm2 and Cc, of 100fF, 100fF and 5pF respectively. Control signals come on the 9-bit address bus and 16-bit data bus, and access each individual cell providing the addressing mechanism for downloading the bit-string configuration of each cell. A total of ~5000 bits is used to program the whole chip. The pattern of interconnection between cells is similar to the one used in commercial FPGAs: each cell interconnects with its north, south, east and west neighbors. This is the first mixed-signal programmable array, FPMA, in the sense that its cells can be configured as both analog and digital circuitry; with its 64 cells it can configure more Operational Amplifiers (OpAmps) than the largest commercial Field Programmable Analog Array (FPAA) chip (which contains only 20 OpAmps) [19].

3. EXPERIMENTAL PROCEDURE

The radiation source used was an X-ray based where electrons are accelerated in a vacume chamber. The radiation rate supplied was 300 rad/sec.

The procedure for exposure to radiation, test, and recovery was as follow; 4 different samples of the FPTA chip were exposed to radiation at a time. Two of the samples were under electronic bias (chip B1 and chip B2), whereas, the other two remained un-biased (chip U1 and chip U2). Due to space limitations in the chamber, only two chips could be radiated at a given time, so the biased and un-biased sets were alternated under the same radiation dose.

Both the biased and un-biased sets were exposed to radiation doses ranging from 0 to 300Krad at 50Krad steps. Figure 3 illustrates the incremental radiation profile to which the chips were subjected to over a period of 7 days.

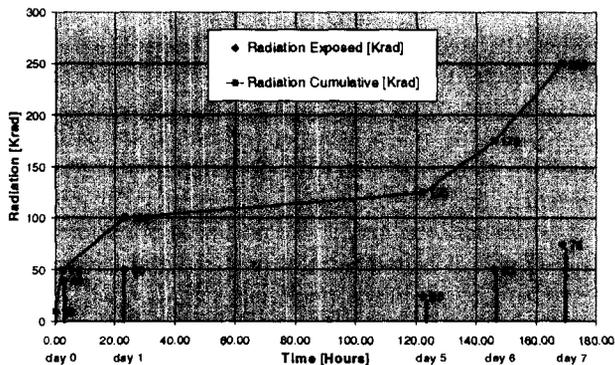


Figure 3: Cumulative radiation and experimental schedule.

After each radiation step both biased and un-biased sets were tested by downloading the configuration for the

following tests/circuits respectively: Identity test, rectifier circuit, Tunable filter, 4-bit A/D converter circuit, Inverter circuit, and a Nand gate circuit.

The identity test is specially designed to test the switching elements, i.e. transmission gates, within the FPTA and operate by propagating a sinusoidal signal to the output through exercising the correct set of transmission gates within the FPTA. The rectifier, tunable filter, and the 4-bit A/D converter are examples of relatively large macro blocks which are utilized within sensor interfacing circuitry.

4. SYSTEM ARCHITECTURE

A complete stand-alone board-level evolvable system (SABLES) is built by integrating the FPTA and a DSP implementing the Evolutionary recovery algorithm, as shown in Figure 2. The system is connected to the PC only for the purpose of receiving specifications and communicating back the result of evolution for analysis. The system fits in a box 8" x 8" x 3". Communication between DSP and FPTA is very fast with a 32-bit bus operating at 7.5MHz. The FPTA can be attached to a Zip socket attached to a metal electronics board to perform extreme temperature and radiation experiments The evaluation time depends on the tests performed on the circuit. Many of the tests attempted here require less than two milliseconds per individual, and runs of populations of 100 to 200 generations require only 20 seconds.

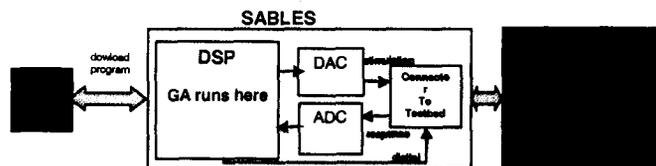


Figure 2: Complete System Architecture.

5. RESULTS

Tables 1-4 illustrate results of radiation tests for dosages of 100Krad, 175Krad, 250Krad, and 350Krad respectively. Each table illustrates the experimental results with the various tests described in section 3 using both biased and un-biased test chip samples. The X symbol indicates the failure of the specific test with the corresponding chip, whereas V indicates its success. The elliptical shapes highlight a successful recovery through evolution. On the other hand a triangular shape indicates that the recovery was unable to obtain an acceptable output for the particular test. For each test any noticeable change in the behavior of input/output signals are reported. For example in table 1, U2 sample initially suffers a 50% drop in amplitude after reaching an accumulative dosage of 100krad. This is later recovered through evolution in 311 generations.

Table 1: Experimental results at 100kRads on chip samples un-bias U1, U2 and bias B1 and B2.

	U1	U2	B1	B2	B3	B4	B5	B6	
test on cell0; cell16; cell17; cell5 switches: S2-S31-S24-S29-S30-S57-S71	X response flat	X response flat for all chromosomes	V	V	V	V	V	X shape output distorted	V recovered - raise fitness threshold to 6K from 4.5k - sine wave slightly clipped on the rising edge
test on cell0; cell16; cell17; cell5 switch: S2	X response flat	X response flat for all chromosomes	V	V	V	V	V	V	
4 cells: cell0, cell1, cell2, cell3	X response flat	X response flat for all chromosomes	X amplitude drop 50%	V recovered generation=311 fitness=4600	X amplitude drops 50%	V recovered generation=300 fitness=4500	X	X low amplitude sine wave	V recovered generation=242 fitness=4890
10 cells: cell0 to cell9 frequency: amplify 1kHz and attenuate 10kHz input:									
20 cells: cell0 to cell19	X 04= signal bit	X fitness=13 generation=200 not achieving bit2, bit3 and bit4	V	V	V	V	V	X bit1 is working bit2 modification of bit1 in output value	V recovered fitness=4.3 generation=288 reference fitness=2.5

Table 2: Experimental results at 175 kRads.

	U1	U2	B1	B2	B3	B4	B5	B6
test on cell0; cell1; cell2; cell3 switches: S2-S31-S24-S29-S30-S57-S71	V	V	V	V	V	V	V	V
4 cells: cell0, cell1, cell2, cell3	X The shape has been changed. No reconstruction.	V 501 generations fitness 4272	V	X The input is observed at the output	V 577 generations fitness 7506	X The input waveform is observed at the output.	V 208 generations fitness 16212	V
10 cells: cell0 to cell9 frequency: amplify 1kHz and attenuate 10kHz input:	V FREQUENCY ANALYSIS: result of sweep etc: no harmonics INPUT: for input 1kHz = -12.64 dB 10kHz = -19.96 dB OUTPUT: 1kHz = -14.51 dB 10kHz = -36.99 dB	V FREQUENCY ANALYSIS: result of sweep etc: no harmonics INPUT: for input 1kHz = -12.63 dB 10kHz = -19.97 dB OUTPUT: 1kHz = -15.61 dB 10kHz = -37.72 dB	V INPUT: for input 1kHz = 10kHz 1kHz = -12.62 dB 10kHz = -20.01 dB OUTPUT: 1kHz = -14.46 dB 10kHz = -35.34 dB Time response distorted slightly harmonics exist around 1K and 10K	V INPUT: for input 1kHz = 10kHz 1kHz = -12.64 dB 10kHz = -20.00 dB OUTPUT: 1kHz = -21.87 dB 10kHz = -45.24 dB low amplitude at output	X INPUT: for input 1kHz = 10kHz 1kHz = -12.78 dB 10kHz = -19.27 dB OUTPUT: 1kHz = -13.74 dB 10kHz = -38.38 dB	V INPUT: for input 1kHz = 10kHz 1kHz = -11.33 dB 10kHz = -19.05 dB OUTPUT: 1kHz = -12.21 dB 10kHz = -38.88 dB	V Reference Chip fitness=4.1	
20 cells: cell0 to cell19	X bit 3 bit four jump and slight bit three jump (discontinuity).	X recovered a 3bits DAC	V	X similar to U1, with more jump on B4	V low voltage range small glitch for bit fitness=6.3	X bit 4 same as bit 1 bit 1 has a slight jump.	V low voltage rate fitness=6.5	V Reference Chip fitness=4.1

After a total dose of 100Krad a number of sample chips suffered from some distortion in the shape of the output waveform. This is mainly observed as a drop in amplitude of the signal. When evolutionary recovery is triggered most of these distortions are overcome and the true functionality is obtained. However, it must be noted in some cases that the fitness threshold in the evolutionary algorithm may require adjustment. This can be clearly seen when performing identity checks on the sample chip B2, where the fitness is adjusted from 4500 to 6000 (Table 1). Although the resulting sine wave has a slight clip on the rising edge, this is small enough not to distort the output waveform which is very similar to that applied on the input. It could be noted from the table 1 that the unbiased chip U1 starts to malfunction at 100Krad with most tests failing drastically such that recovery is not possible.

As the radiation dosage is increased to 175 Krad, the distortion on the output increases. For example, the rectifier for both B1 and B2 passes the input unchanged.

However, in almost all cases the evolutionary recovery system is able to correct the output to the required shape. Figure 4(a) illustrates the response of the rectifier at 50krad on the sample B1 chip. After exposure to radiation of up to 175Krad the rectifier malfunctions as the output response is identical to that of the input shown on Figure 4(b). When the evolutionary mechanism is activated, the correct output response is retained as shown in Figure 4(c).

Table 3: Table 3: Results with 250kRads

Test	Human	Human	Human	Human	Human	Human	Human
Test on c6d0, c6e1, c6e2, c6e3 switches: 52, 931, 524, 529, 530, 567, 571	X output 0 This is true for calls 47, 48, 9, 1, 32 Also true with a2 closed while input on in2 and output on 1	X nearly a flat input. However, there is the shape of input following the output.	V	X slight distortion in output. Sign wave slightly distorted on both sides. Also true for calls 16 Also true with a2 closed while input on in2 and output on 1	X slight decrease in voltage level. also wave clipped on left and right hand sides.	X output 0 This is true for calls 1, 4, 5, 16, 37 also true with a2 closed while input on in2 and output on 1	V perfect waveform obtained
4 calls: c6d0, c6e1, c6e2, c6e3	X output flat	X Function is not even close to the solution.	V	X Output follows the input as a sine wave, with slight distortion on the right hand side	X The bottom 10 and perfectly flat. Stress is 7295. also 1327 measurements	X output follows the input with slight reduction in amplitude.	V perfect recovery. Fitness 4279 after 78 generations. In a number of runs the GA was not able to spot perfect solutions even though these were spotted on the escape. Clearly the fitness function is not perfect for this problem. It may be possible to
10 calls: c6d0 to c6e3 Frequency: simply 1kHz and amplitude 10kHz input	X input flat 1kHz = 10kHz 10kHz = 37.55 dB 10kHz = 31.00 dB OUTPUT: 1kHz = 37.62 dB 10kHz = 44.37 dB	X an response in evolution	V FREQUENCY ANALYSIS: result of sweep: on harmonics INPUT: for input 1kHz + 10kHz 1kHz = -32.30 dB 10kHz = -18.00 dB OUTPUT: 1kHz = -15.54 dB 10kHz = -37.46 dB	X output flat FREQUENCY ANALYSIS: INPUT: for input 1kHz + 10kHz 1kHz = 32.56 dB 10kHz = 19.94 dB OUTPUT: 1kHz = 42.93 dB 10kHz = 47.07 dB	X best response similar to input, with loss of sine shape and lowering of level.	X output has same amplitude. INPUT: for input 1kHz + 10kHz 1kHz = 32.57 dB 10kHz = 19.94 dB OUTPUT: 1kHz = 22.74 dB 10kHz = -45.20 dB	V FREQUENCY ANALYSIS: result of sweep: low harmonics around 10kHz INPUT: for input 1kHz + 10kHz 1kHz = -32.70 dB 10kHz = -18.24 dB OUTPUT: 1kHz = -16.54 dB 10kHz = -37.76 dB a number of runs failed producing best response similar to input, with loss of sine shape. But low and low-amplitude
20 calls: c6d0 to c6e3	X output follows bit	X Sometimes the output is the same as bit number / but a small square wave on high levels and sometimes output flat.	V	X output follows bit 4, with some sort of DAC behaviour at low and high levels	X a monotonic wave was obtained similar to the DAC, however the amplitude is dropped by half and levels are not clear	X The output looks like a dac but the shape is not monotonic, has steps and jumps, and some sudden jumps. Better than ut and bit though.	X

Table 4: Results with 350kRads.

Iteration	Best	Second	Third	Fourth	Fifth	Sixth	Seventh	Eighth	Ninth	Tenth
Iteration 0										
Iteration 1										
Iteration 2										
Iteration 3										
Iteration 4										
Iteration 5										
Iteration 6										
Iteration 7										
Iteration 8										
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Iteration 10										
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Iteration 45										
Iteration 46										
Iteration 47										
Iteration 48										
Iteration 49										
Iteration 50										

As the dosage is increased to 250Krad (Table 3), cases appear where the evolutionary algorithm is unable to recover the correct functionality on the output (discarding U1 due to its inconsistent behavior). However, in most cases recovery is achieved. Again considering the rectifier circuit at 250krad as illustrated in Figure 5(a), the output response is clearly distorted due to radiation. However, the correct output response is recovered once the evolutionary mechanism takes over, even though the final circuit suffers from some non-ideal behavior when the output is low.

As the dosage reaches 350 Krad (Table 4), there is a clear failure pattern with all tests, with the evolutionary algorithm unable to recover any of the required functionality.

Figure 6 demonstrates another example of recovery through evolution using the example of the 4-bit DAC circuit. Figure 6(a) illustrates a correct functioning DAC at 100Krad. When radiation dosage is increased to 175Krad, the circuit malfunctions with clear loss in discrimination between various input values. This is associated with a loss in the monotonic nature of the response, see figure 6(b). When evolution is activated the response is recovered, however, as could be seen from Figure 6(c) there is some deterioration in the signal level.

6. CONCLUSIONS

The paper has presented a mechanism for adapting a mixed analogue reconfigurable platform under total dose radiation faults. Experiments were carried out which exercised the reconfigurable device up to 350Krad radiation dosages demonstrating that the technique is able to recover functionality of blocks such as analogue to digital converters up to 250Krad radiation dosage.

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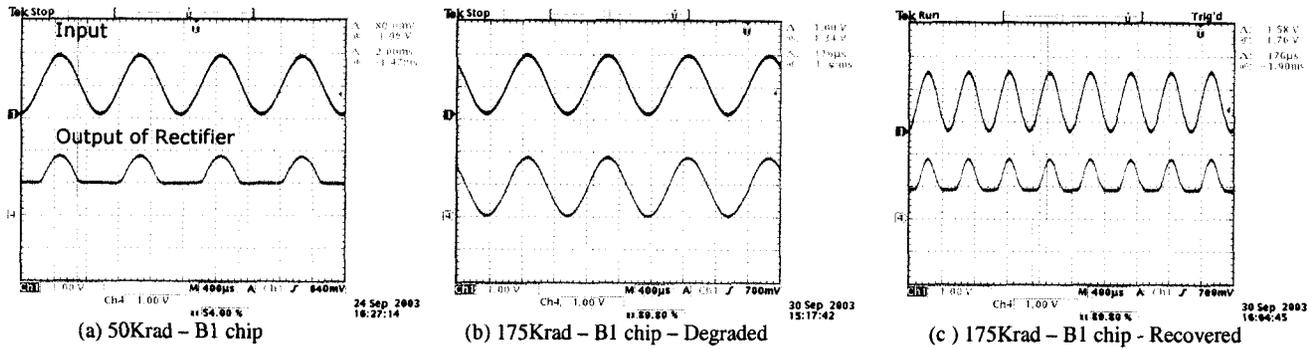


Figure 4: Response of the Rectifier circuit at (a) 50kRads, (b) after being radiated to 175kRads resulting in deterioration through loss of rectification, followed by (c) recovery through Evolution.

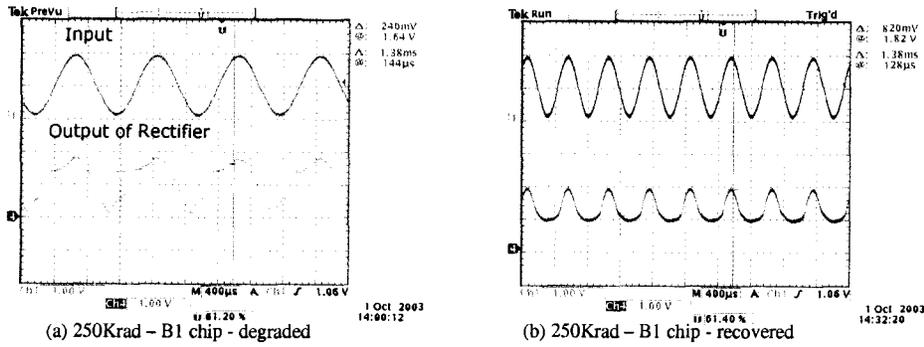


Figure 5: Response of the Rectifier circuit at (a) 250kRads resulting in distortion, followed by (b) recovery through Evolution

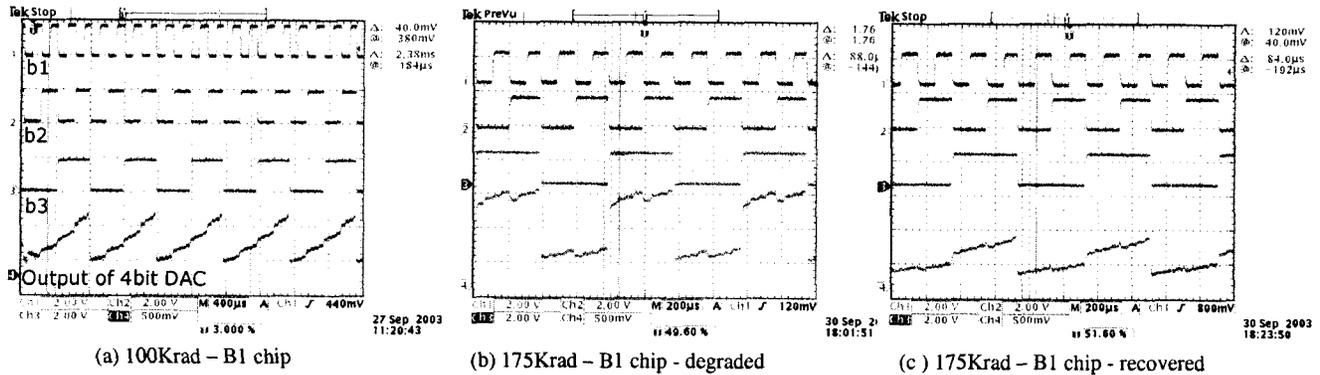


Figure 6: Response of a 4bit DAC circuit (least significant bit b_0 is not shown) at (a) 100kRads, (b) after being radiated to 175kRads resulting in deterioration through loss of "monotonicity", followed by (c) recovery through Evolution at 175kRads.