



**Space Processor Radiation Mitigation
and Validation Techniques for an
1800 MIPS Processor Board**

Heavy Ion Test Results

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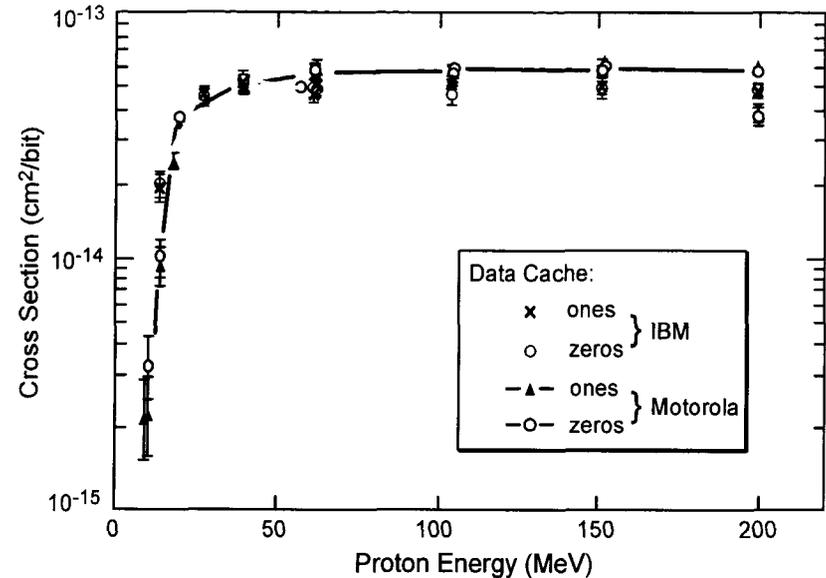
Maxwell Technologies

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In 2001 at NSREC, we concluded:

- From a radiation standpoint, both manufacturers' PowerPC750s are usable for *non-critical* space applications that are like on-board data processing
 - Low upset rate
 - Very low “hang” rate
 - Occasional reset or re-power needed
 - Upset-aware exception handlers needed
- **Proton upset rates tend to dominate heavy ion rates for environments with significant proton components, such as:**
 - Earth Orbit (due to trapped protons)
 - Large Flares



Today, we consider:

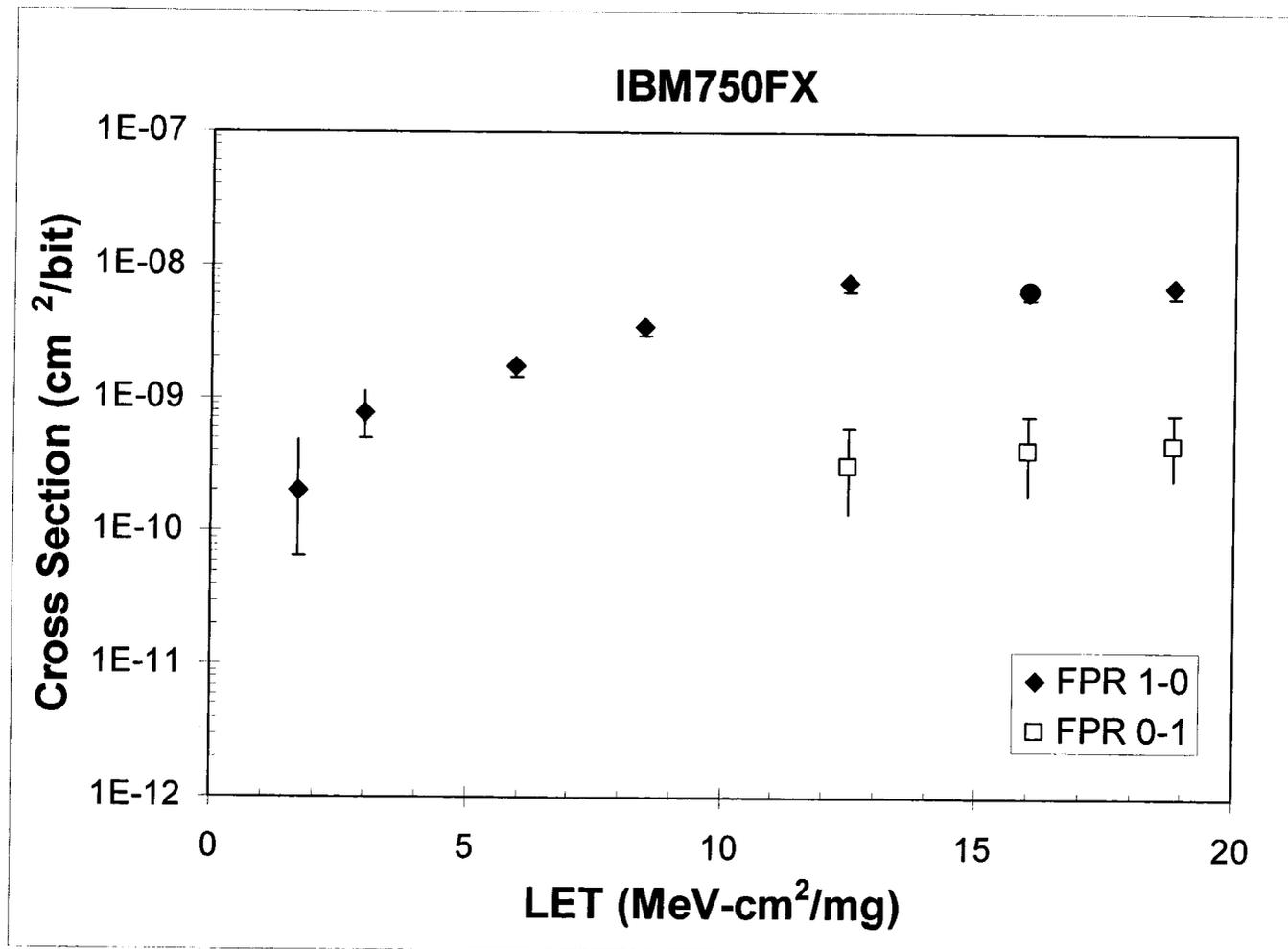
Can system design add sufficient robustness to upset for *critical* applications?

OUTLINE

- Single Processor Results for the IBM PPC750 FX
 - Earlier “static” data
 - “Dynamic” test data
- Three Processor Results
 - System Mitigation Dependences
 - Flux more important than fluence
 - Linear with scrub rate
 - Re-syncs and Reset Results
- In-flight Upset Rate Comparison

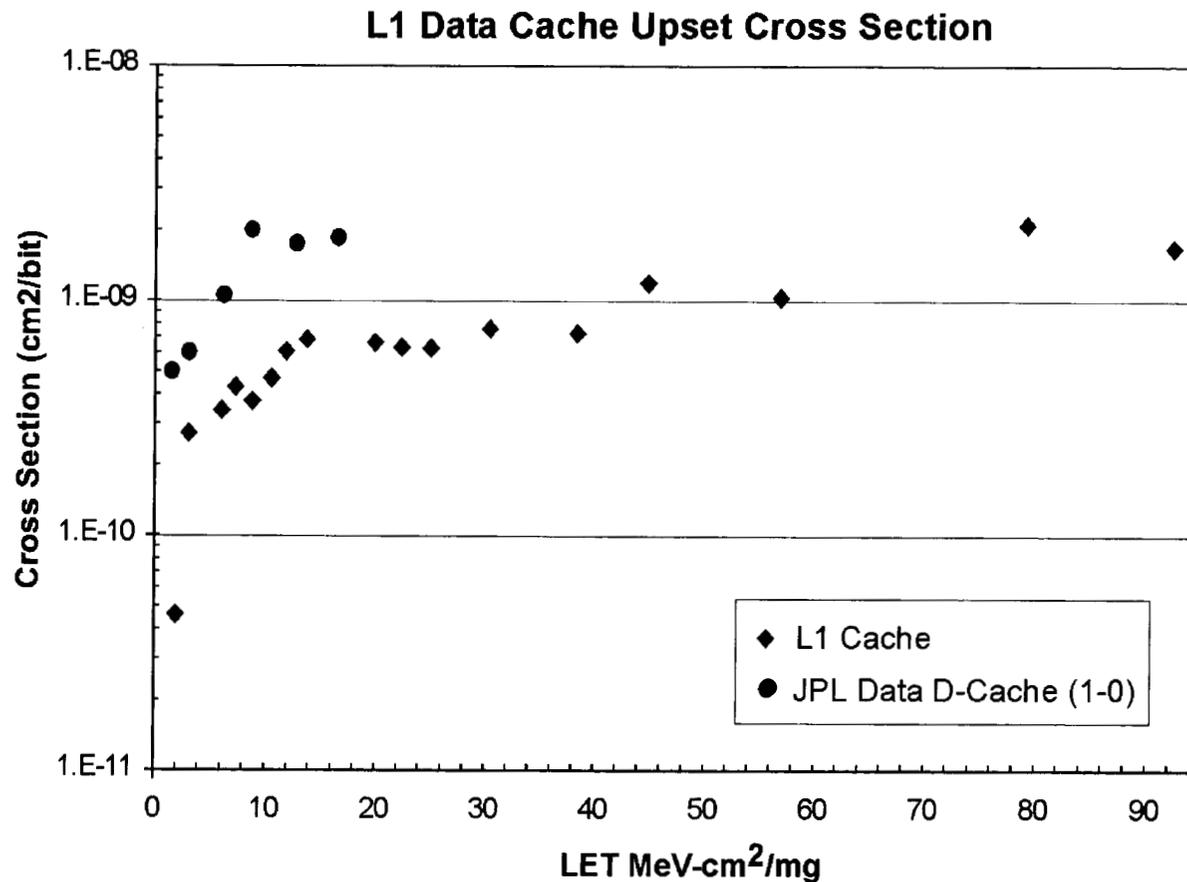
Upset Susceptibility of the IBM PPC 750 FX

From the NSREC 2002 dataset:



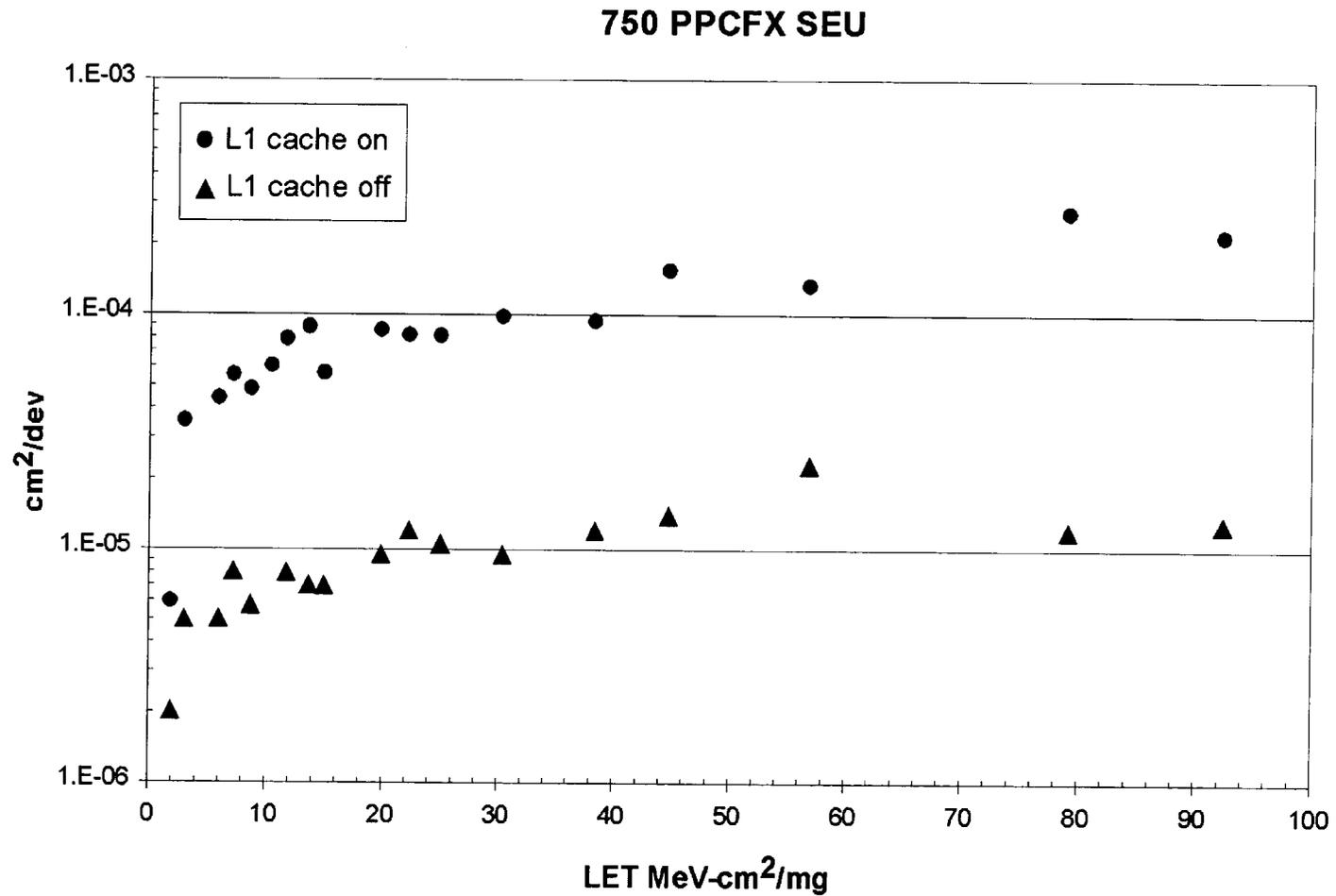
Upset Susceptibility of the IBM PPC 750 FX

New Test Results from Texas A&M Cyclotron:



Upset Susceptibility of the IBM PPC 750 FX

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Test Comparison

Differences in:

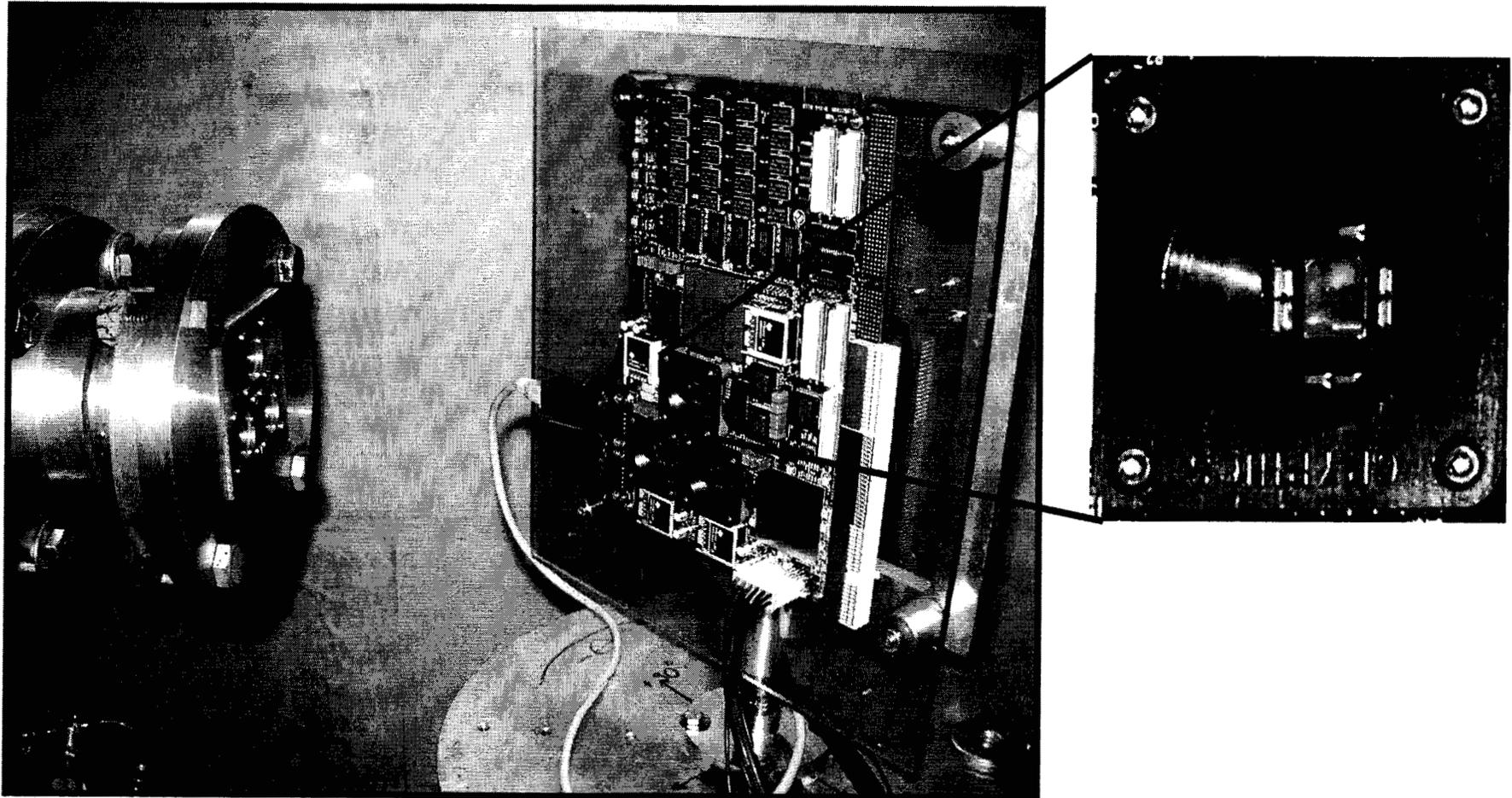
board	-	custom	vs.	Yellowknife
OS	-	VxWorks	vs.	none
program	-	Dhrystone	vs.	do nothing loop
background	-	scrub	vs.	snapshots
speed	-	650 MHz	vs.	500 MHz
die rev	-	DD2	vs.	DD1

Most important difference:

“Register” Test vs. “Application” Test

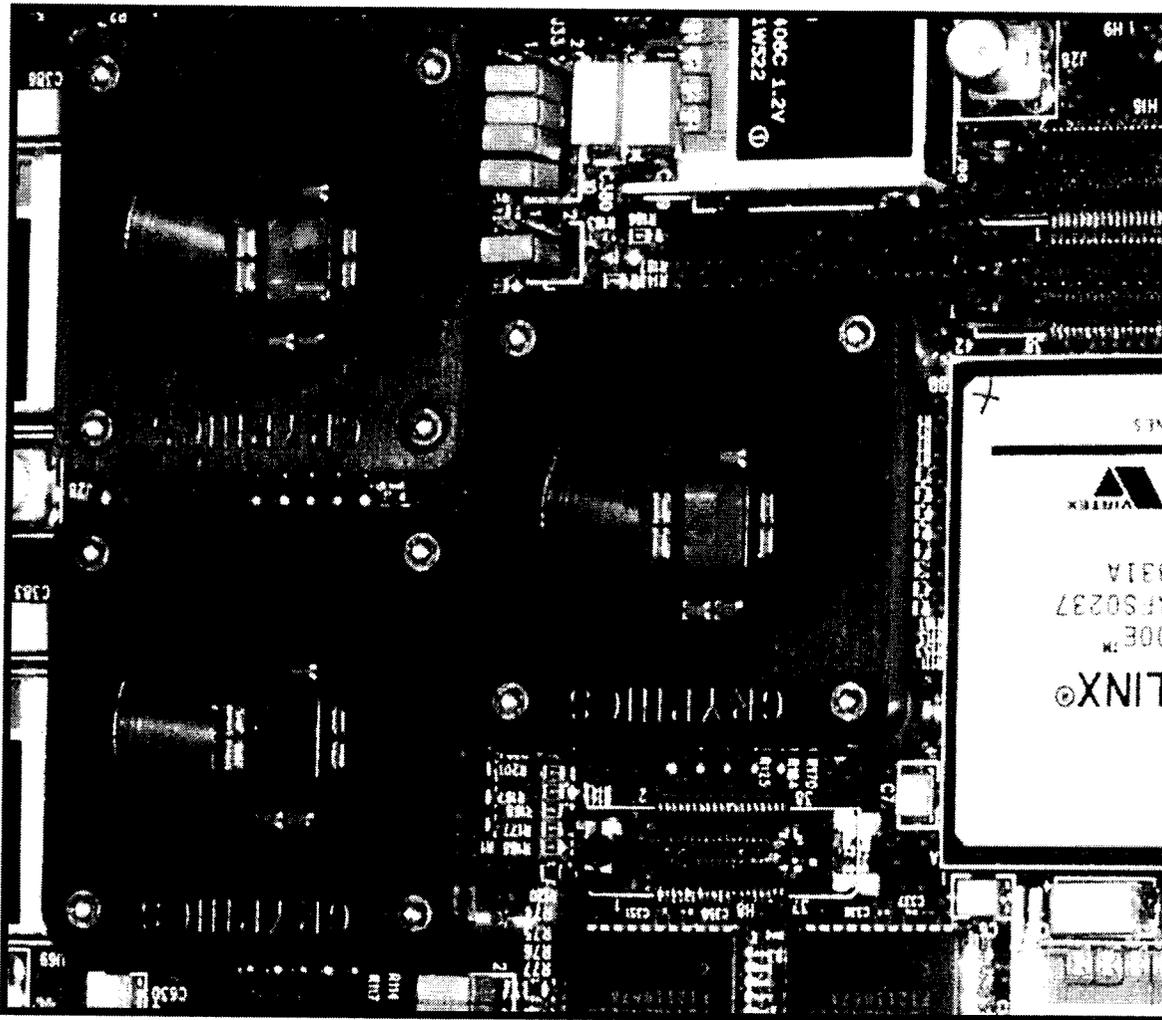
Three Processor Test Setup

At the Texas A&M Cyclotron Facility:



Three Processor Test Setup

At the Texas A&M Cyclotron Facility:



Upsets by Processor

Run	uP-A	uP-B	uP-C
47.1	67	82	82
47.2	20	20	15
47.3	63	66	62
47.4	22	18	19
47.5	113	157	131
47.6	27	32	23
47.7	45	56	37

Quite
Acceptable
Uniformity

Three-Processor System Upset Mitigation

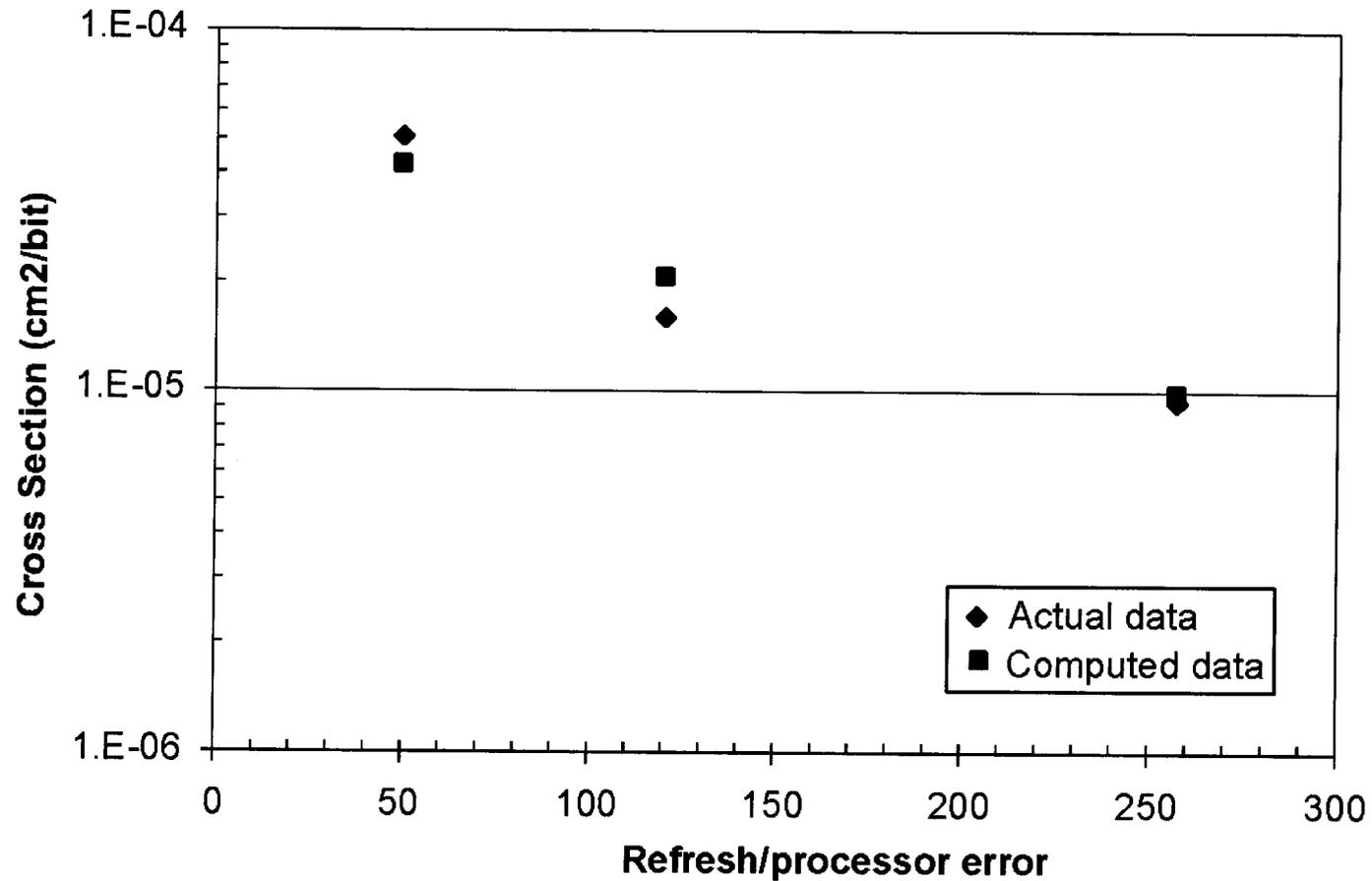
- Regular re-sync “scrubs” single processor upsets
- Upsets in two out of three processors require reset
 - Rate of resets (double errors) goes as:
 - Upset rate (or flux) squared
 - Proportional to scrub time
 - Equation:
 - Reset rate = $3 \times [\text{scrub time}] \times [\text{error rate per processor}]^2$

Three-Processor System Upset Mitigation

- Testing requires steady and low fluxes
 - Made difficult by:
 - Small collimators on beam dosimetry
 - Source fluctuations are a problem, particularly for solid sources
- Example: ion rate triples for 10% of a run
 - Yields 20% more fluence
 - BUT almost doubles likelihood of two errors during a scrub time

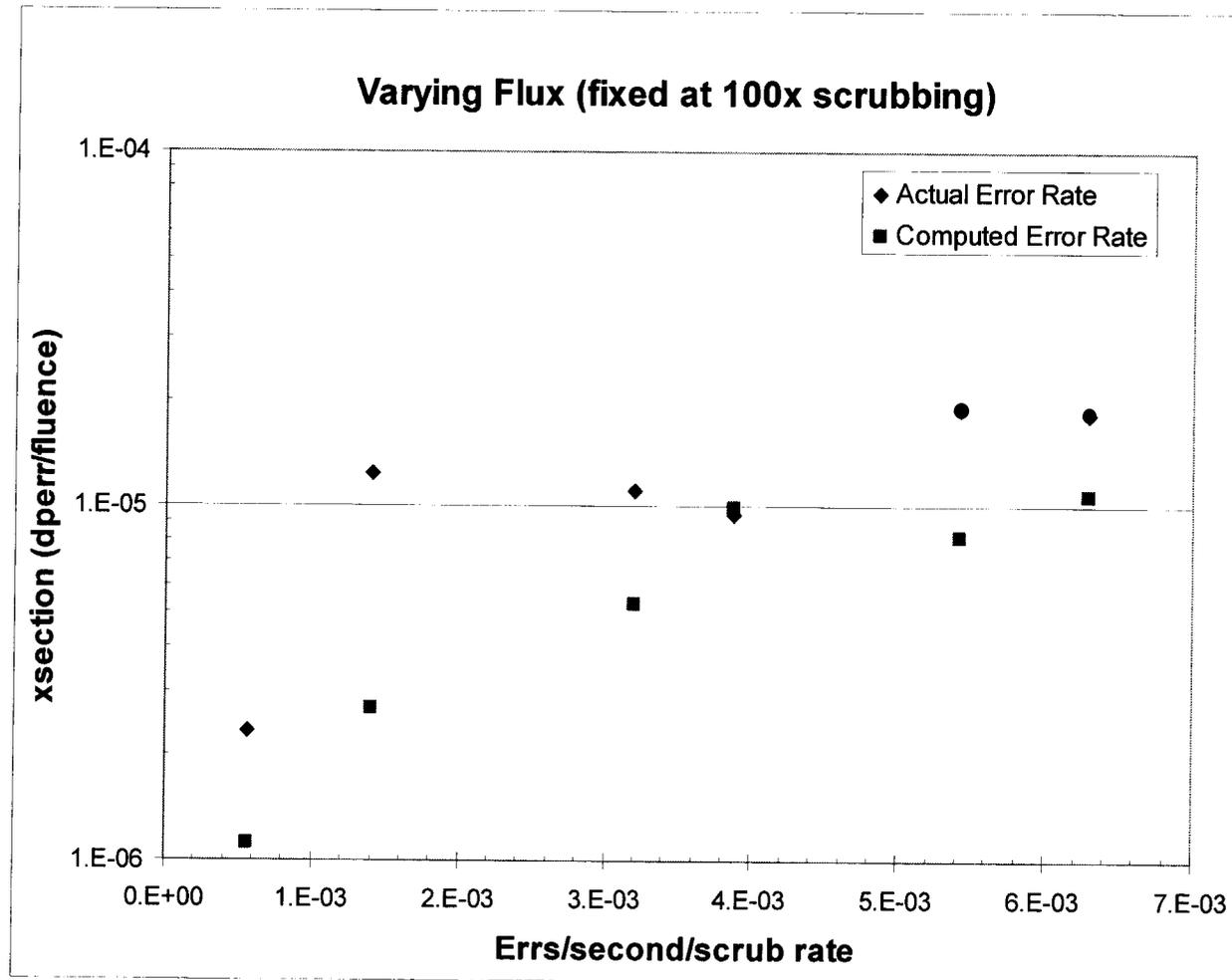
Three-Processor Results

Cross section as a function of scrub rate



Three-Processor Results

Cross section as a function of flux



Rate Comparison

	PPC750FX processor	RAD6000 board	3-P Board*
GCR	34/yr	0.2/yr	1.1E-4/yr
DCF only heavy ions	250/flare	0.6/flare	2.2/flare
DCF including protons	320/flare	3.4/flare	3.6/flare

Note: assuming equivalent shielding of 100 mil Aluminum

GCR = Galactic Cosmic Ray background at solar minimum

DCF = JPL Design Case Flare (at one A.U.)

*1 scrub/second, L2 Cache has ECC, L1 not using parity

CONCLUSION

- Under heavy-ion irradiation, the three-processor upset mitigation scheme was demonstrated to be quite effective, at least for the test programs.
- The performance hit for periodic re-syncing (scrubbing) is small.
- Upon the coincidence of an upset in two processors, the board successfully re-booted itself. Power cycling was never required to recover correct operation.