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DEVELPOMENT OF RELIABLE ELECTRONIC PACKAGING SOLUTIONS FOR SPACECRAFT AVIONICS MINIATURIZATION USING EMBEDDED PASSIVE DEVICES

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ABSTRACT

Miniaturization of electronic packages will play a key role in future space avionics systems. Smaller avionics packages will reduce payloads while providing greater functionality for information processing and mission instrumentation. Current surface mount technology discrete passive devices not only take up significant space but also add weight. To that end, the use of embedded passive devices, such as capacitors, inductors and resistors will be instrumental in allowing electronics to be made smaller and lighter. Embedded passive devices fabricated on silicon or like substrates using thin film technology, promise great savings in circuit volume, as well as potentially improving electrical performance by decreasing parasitic losses. These devices exhibit a low physical profile and allow the circuit footprint to be reduced by stacking passive elements within a substrate. Thin film technologies used to deposit embedded passive devices are improving and costs associated with the process are decreasing.

There are still many challenges with regard to this approach that must be overcome. In order to become a viable approach these devices need to work in conjunction with other active devices such as bumped die (flip chip) that share the same substrate area. This dictates that the embedded passive devices are resistant to the subsequent assembly processes associated with die attach (temperature, pressure). Bare die will need to be mounted directly on top of one or more layers of embedded passive devices. Currently there is not an abundant amount of information available on the reliability of these devices when subjected to the high temperatures of die attach or environmental thermal cycling for space environments. Device performance must be consistent over time and temperature with minimal parasitic loss.

Pretested and assembled silicon substrates with layers of embedded capacitors made with two different dielectric materials, Ta_2O_5 (Tantalum Oxide) and benzocyclobutene (BCB), were subjected to the die attach process and tested for performance in an ambient environment. These assemblies were subjected to environmental thermal cycling from –55°C to 100°C. Preliminary results indicate embedded passive capacitors and resistors can fulfill the performance and reliability requirements of space flight on future missions. Testing results are encouraging for continued development of integrating embedded passive devices to replace conventional electronic packaging methods.

INTRODUCTION

The objective of this experiment was to determine the effect of assembly processing temperatures and subsequent thermal cycling on the performance of embedded capacitors. This is the beginning of a two-phase study. The initial study, which is the topic of this paper is focused on the evaluation of the effects of assembly processing temperatures, namely chip-on-board bonding over embedded passive capacitors. Once evaluated this is followed by environmental testing that consists of thermal cycling the capacitors to further determine their reliability. The second study, which is in work at this time, includes embedded passive devices, (capacitors and resistors) incorporated into a functional power circuit that will be subjected to environmental testing. Die attach reliability will also be evaluated.

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TEST HARDWARE DESIGN

Multiple layers of embedded capacitors will be required for future application in order to make this a viable alternative to current surface mount designs. Due to space and weight constraints the desired packaging solutions for future space flight electronics are primarily active devices in bare die form (flip chip) mounted directly to embedded substrates with resistor, inductor and capacitor networks integrated into the substrate below. Due to its low mass and desirable thermal coefficient of expansion properties silicon was also selected as the substrate material over ceramic or conventional printed circuit board substrate materials such as FR4 and polyimide. The selection of silicon as a substrate for this study ignores industry fabrication costs for this material selection. This is considered an expensive approach over Low Temperature Co-Fired Ceramic substrates and standard printed circuit board materials. Silicon was selected primarily for its advantages in reliability due to optimized TCE matching and low mass. The test hardware consisted of a single 125 mm silicon wafer. The silicon wafer acts as the base substrate material for the embedded capacitors. The wafer is subdivided into 13 sections or groupings each containing 10 embedded capacitors. See Figure 1 for illustration and numbering of groupings. See Figure 2 for picture of wafer; capacitor substrate groupings are visible.

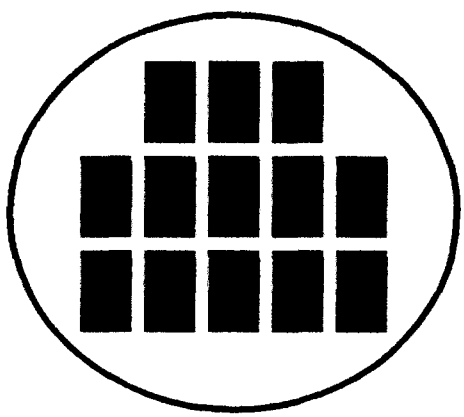

Figure 1 – Illustration of 125 mm wafer with embedded capacitor groupings

Figure 3 depicts a plan view of both capacitor layers and illustrates them side-by-side to help show the layout. In the as fabricated form the top layer is superimposed over the bottom layer. Figure 4 is a simplified illustration of the substrate cross section. The capacitors that were deposited on the substrate were made up of 2 different materials, 6 were tantalum oxide (Ta_2O_5) and 4 were BCB (benzocyclobutene). The first layer or bottom layer consists of 8 capacitors and the second layer or top layer consists of 2 capacitors. The first layer capacitors are labeled T1, T2, T3, T4, and T5 for the tantalum oxide composition and the remaining are labeled B1, B2, and B3 for the benzocyclobutene composition. The second layer or top layer of capacitors are labeled T6 (tantalum oxide) and B4 (BCB). See Figure 3 for illustration of capacitor layout. All of the test capacitors measure 5 mm by 5 mm.

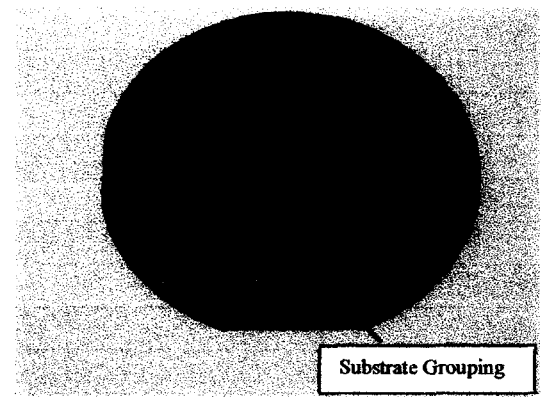

Figure 2 – Picture of 125mm wafer w/13 embedded capacitor groupings

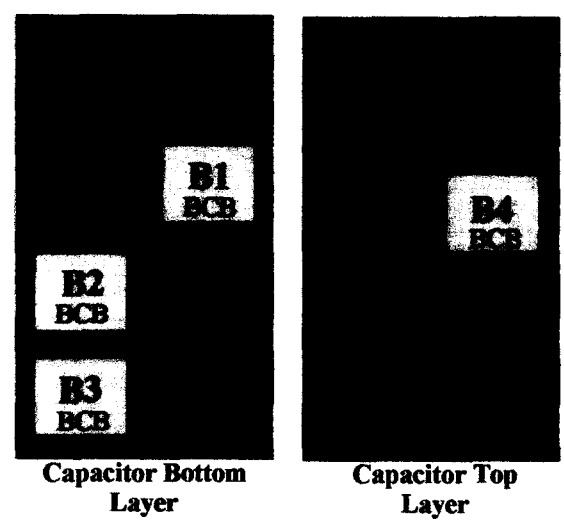

Figure 3 – Substrate showing tantalum oxide and BCB capacitor layout with pad layout for Delco die

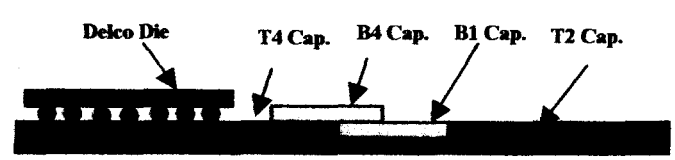

Figure 4 – Cross sectional illustration of substrate

Due to dielectric properties, BCB and tantalum oxide have a significant electrical capacitance difference for the designated 5 x 5 mm space allocated on the substrate. The BCB capacitors require a larger surface area to achieve the same capacitance as a tantalum oxide

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capacitor given the same dielectric thickness. See Figure 5 for the surface area comparison between the two materials. The tantalum capacitors were fabricated to produce approximately 1000 pF/mm^2 with a deposited thickness of 2000 Angstroms. The targeted nominal value for this experiment was 25 nF. The BCB capacitors were fabricated to produce approximately 4.80 pF/mm^2 with a spun thickness of 5 microns. The targeted nominal value for this experiment was 130 pF. The top layer capacitors have some overlap with the capacitors of the bottom layer. The capacitors are not electrically connected to one another. Each capacitor has individual test pads on the edge of the substrate to measure electrical value. Capacitance values were measured at 120 kHz. The test substrate design also includes a mounting location for a flip chip silicon test die. The test wafer substrate was fabricated at Integral Wave Technologies for the Jet Propulsion Laboratory. This mounting pattern was designed to accept a standard perimeter bumped test die, part number PB-8 manufactured by Delphi Automotive Systems was used for this study. The test die is 10.1 mm x 10.1 mm x 650 microns thick and consists of 88 perimeter solder bumps that are on .28 mm centerlines. The solder balls are Sn63 with a diameter of 102 microns and a height of 112 microns. Every other ball is connected with a trace to allow a complete circuit of electrical continuity if mated to a substrate, which is designed for this purpose. The substrate contains traces above the embedded capacitors to allow a daisy chain; which forms a complete continuous conductive circuit once the die is mounted.

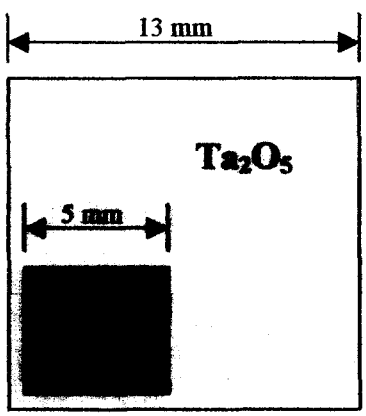

Figure 5 – Relative area scale to achieve equal electrical capacitance

FUTURE CONSIDERATIONS

Extreme cold temperatures in the range of –180°C to 85°C will dictate the future challenges of space flight electronics. There is limited information available for the standard electronic packaging assemblies currently available from industry at these temperatures and even less for chip scale and embedded passive packaging solutions. Future designs will need to include complex layering of embedded capacitors, resistors and inductors to achieve the functionality afforded by today's standard surface mount technology packaging solutions. Active devices in the form of bumped flip chip die will be mounted on top of this complex layer of passives. The effects of thermal mis-match of combined dielectric materials on multiple substrate materials and under chip scale bumped die still needs to be understood.

CONCLUSIONS

The results of this study indicate the Ta_2O_5 and BCB capacitors were not affected by assembly process heating and subsequent short term thermal cycling. The targeted nominal design value for the tantalum capacitors was 25 nF +/-2%. The as processed mean value for all tantalum capacitors measurements taken after fabrication and before thermal cycling was 30.19 nF with a standard deviation of .99 nF. The measured values after 20 cycles from –55°C to 100°C yielded a mean value of 30.01 nF with a standard deviation of .91 nF. The targeted nominal design value for the benzocyclobutene capacitors was 130 pF +/-3%. The processed mean value for all benzocyclobutene capacitors was 130.65 pF with a standard deviation of 1.95 pF. The measured values after 20 thermal cycles yielded a mean value of 129.90 pF with a standard deviation of 1.75 pF. This indicates the data sample values did not change significantly from the as fabricated capacitors to the thermal cycled capacitors. While measured readings did change slightly, the difference was statistically insignificant considering design tolerances and gauge repeatability. Thermal cycling of the test hardware is continuing at the time of this publication. There was not any difference in the measured values of the benzocyclobutene and tantalum oxide capacitors that were located directly under the PB-8 test die vs. the benzocyclobutene and tantalum oxide capacitors located on the remaining substrate area. Die attach processing temperatures did not effect capacitance values.

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