Single-Event Upsets in Highly Scaled Commercial SOI Microprocessor

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Commercial SOI Devices

- Interest in the possible use of commercial SOI processors in space
  - Very high performance (higher speed)
  - Superior electrical performance compared to hardened processors
- Small area and reduced charge collection depth
  - ~110 nm in 0.18 μm feature size
- This work continues earlier work on SOI processors
  - Smaller feature size
  - Processors "Hang"
  - Clock frequency dependence

PD SOI Advantages Over Bulk/epi devices

To first Order

- Reduction of the silicon region for charge collection
- Decrease the *deposited* charge by more than an order of magnitude

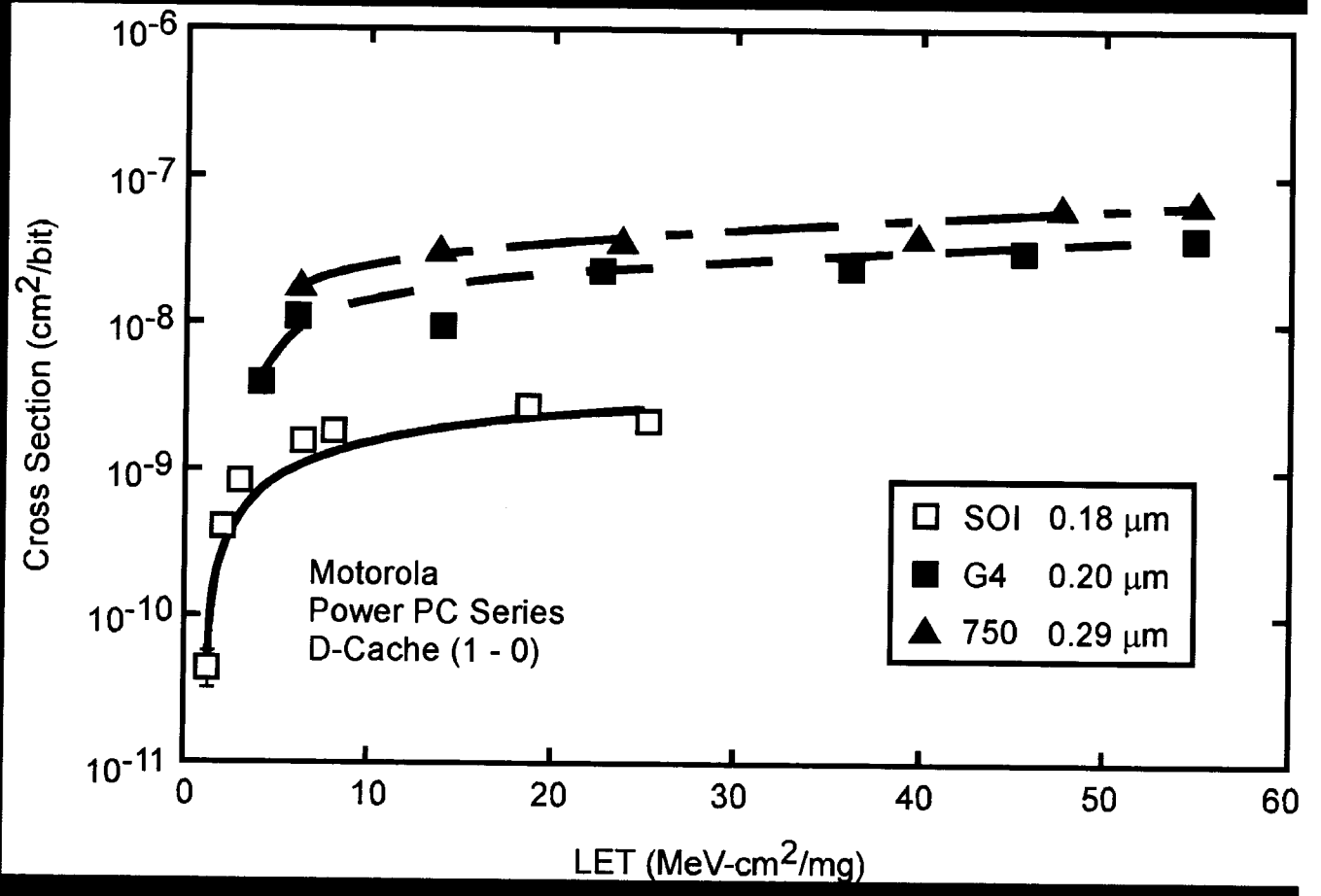
However

- Reduction in junction capacitance
- Lower operating voltages
- Charge amplification by parasitic bipolar Transistor

Limits the degree of improvement in SEU sensitivity that can be obtained with commercial SOI processors

PD SOI Compared with Bulk/epi Devices

- No significant change in the threshold LET
- Cross section is about an order of magnitude lower for 0.18 μm SOI



Motorola and IBM SOI PowerPC Processors

Device	Feature Size (μm)	Film Thickness (nm)	Core Voltage (V)
Mot 7455	0.18	110	1.6
Mot 7455	0.18	110	1.3
Mot 7457	0.13	55	1.3
IBM 750FX	0.13	117	1.4

Static SEU Testing

- Write a test pattern into the storage elements
- Irradiate the part
- Read the storage element states
- Determine the number of SEUs

Obviously, clock frequency has no effect on Static measurement of this kind

Dynamic SEU Testing

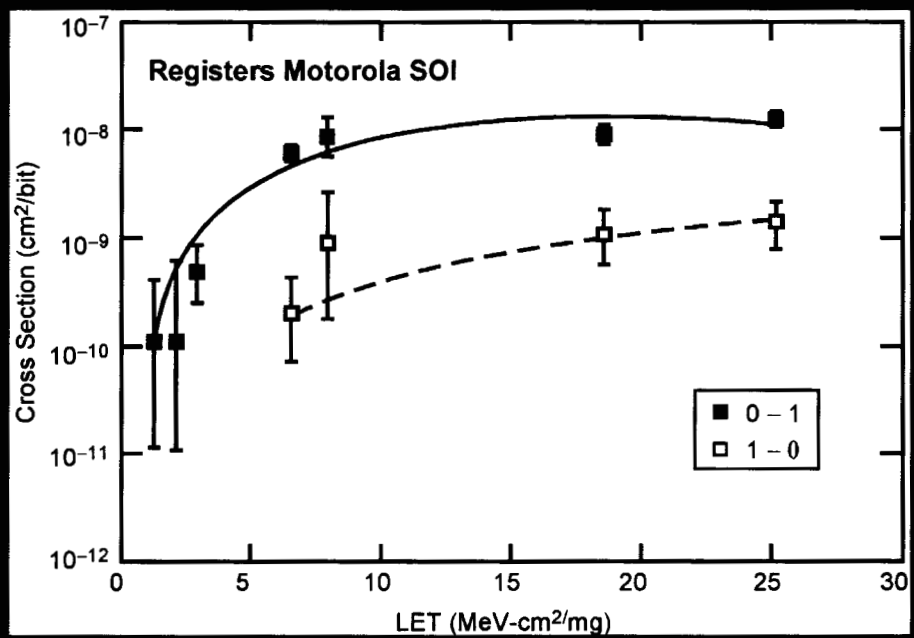
- The storage element is continuously written to and read during irradiation
- Determine number of upsets

Clock frequency is expected to affect the cross section Measurement.
Because there is a larger probability that transient from logic operator will overlap clock edge transitions

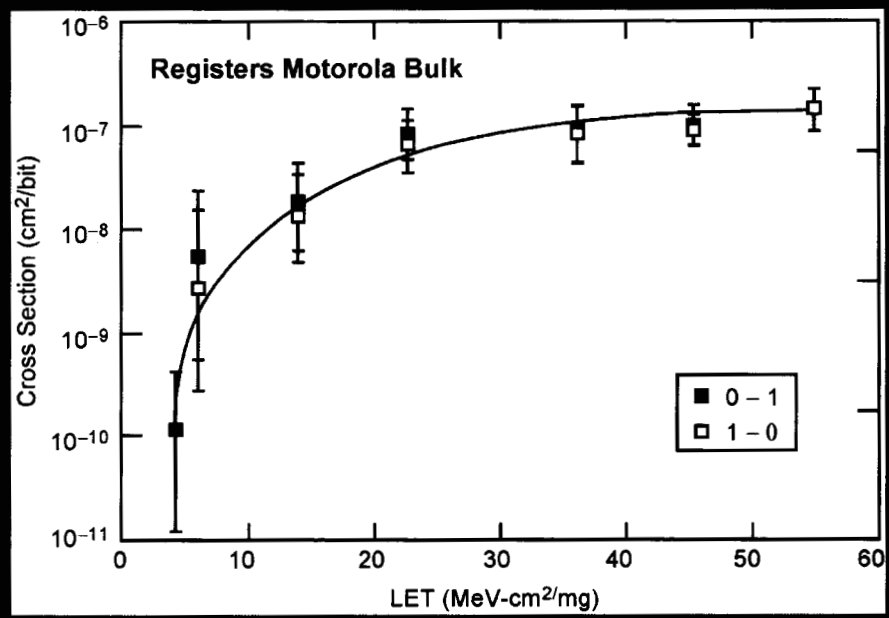
Radiation Test

- Heavy-ion at Texas A&M
  - Back irradiation
  - LET's from 1 to 25 MeV-cm^2/mg
- We measured static cross sections for
  - Registers
  - D-Cache
  - Functional Errors ("Hang")
- We measured dynamic cross section for
  - Registers (350 and 1000 MHz)
  - D-Cache (in near future)

Asymmetric Sensitivity for Registers in SOI Processor

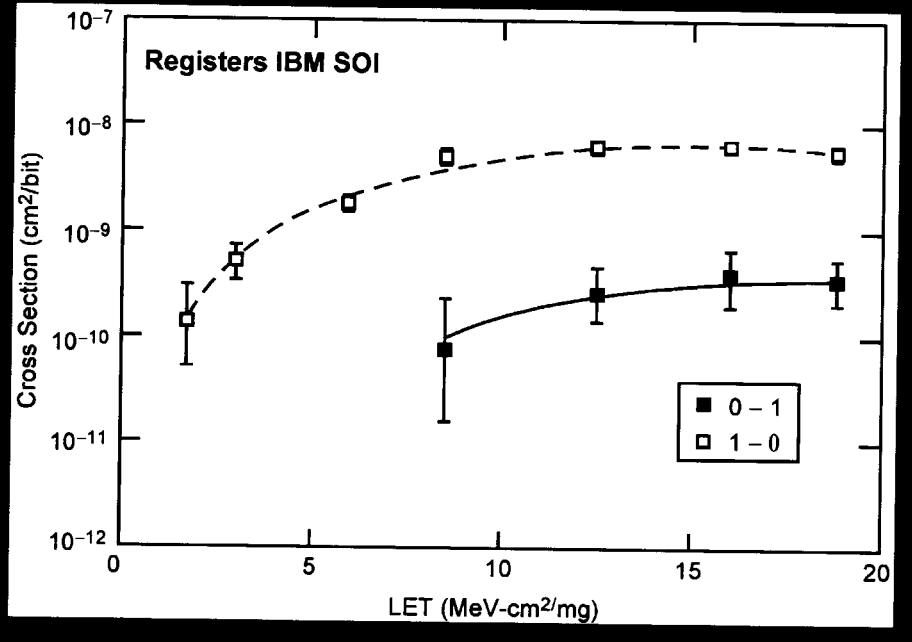


Heavy–ion cross section for the Registers of the SOI PowerPC 7455

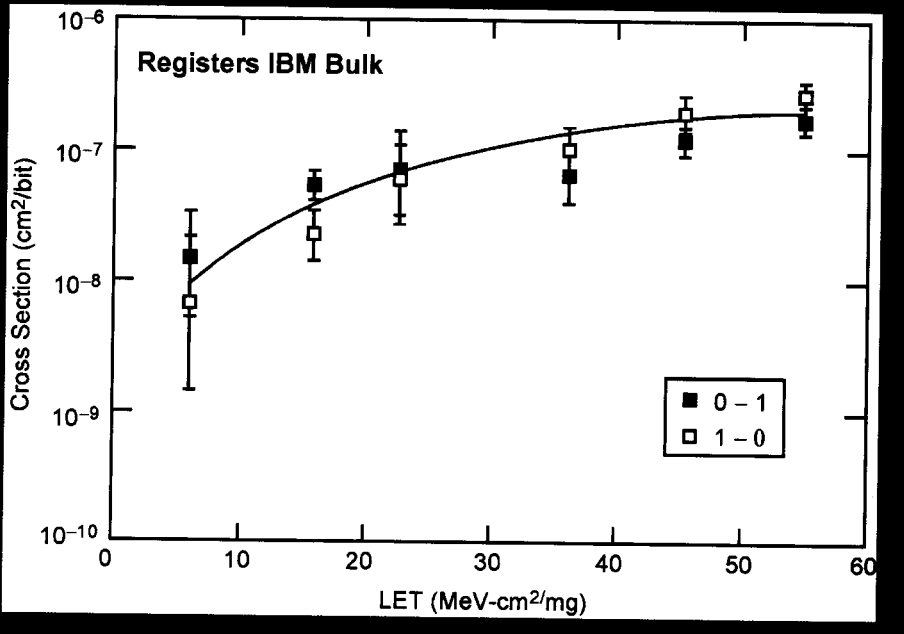


Heavy–ion cross section for the Registers of the bulk/epi PowerPC 7400

Asymmetric Sensitivity for Registers in SOI Processor



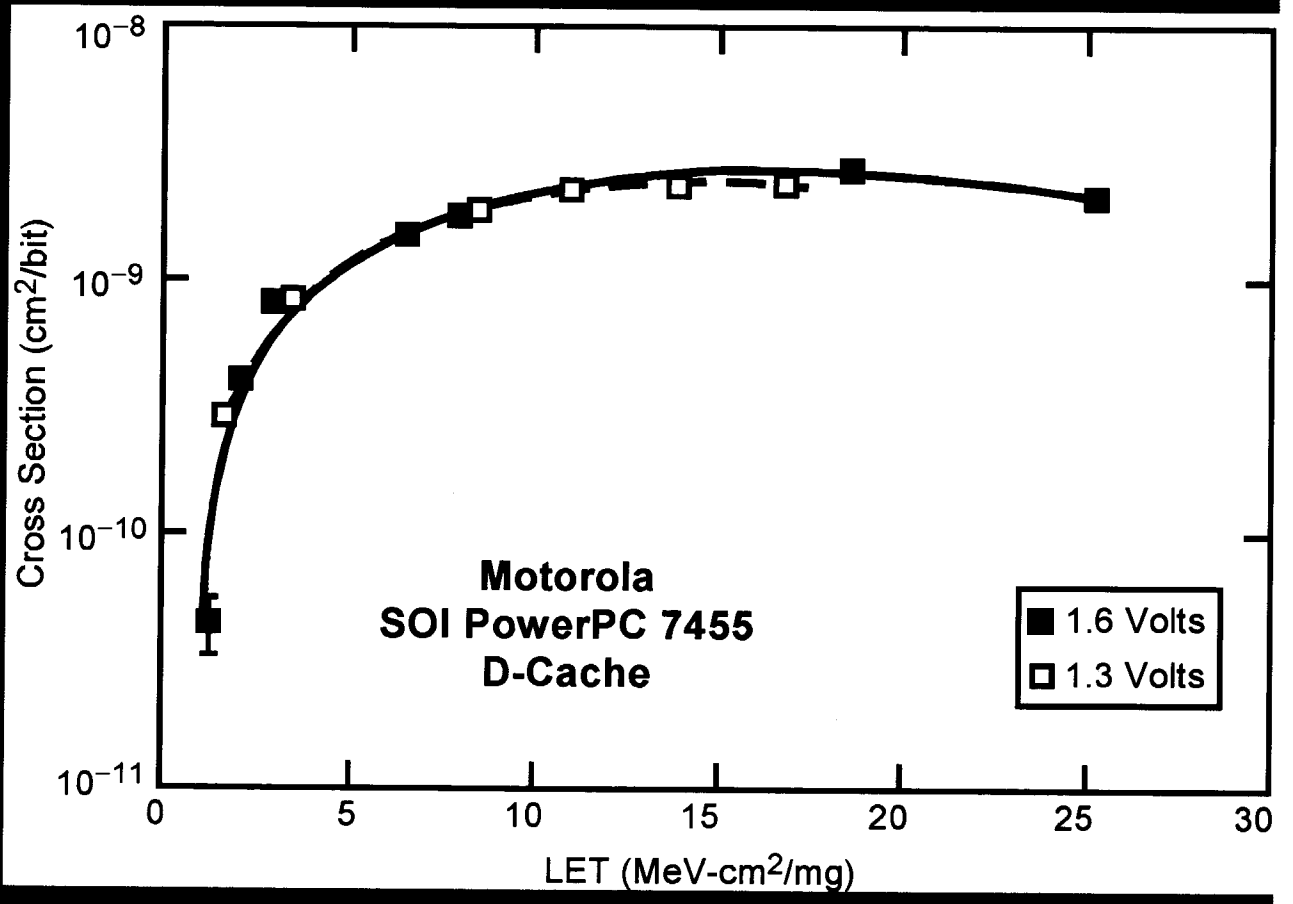
Heavy–ion cross section for the Registers of the SOI PowerPC 750FX



Heavy–ion cross section for the Registers of the bulk/epi PowerPC 750

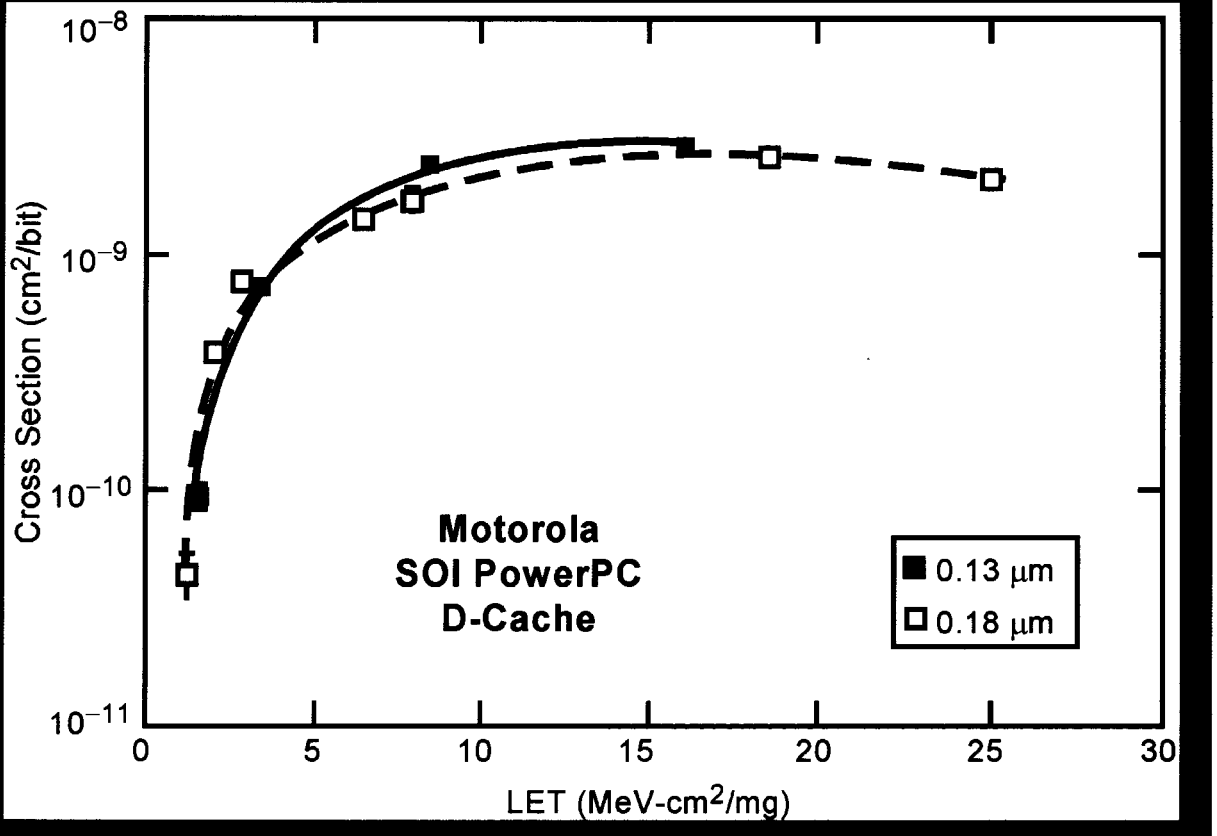
Cache Tests for SOI Processor with Two Different Core Voltage Specification

- Same feature size
- Same film thickness
- Different core voltage in specification
- Nearly the same results, despite the lower core voltage

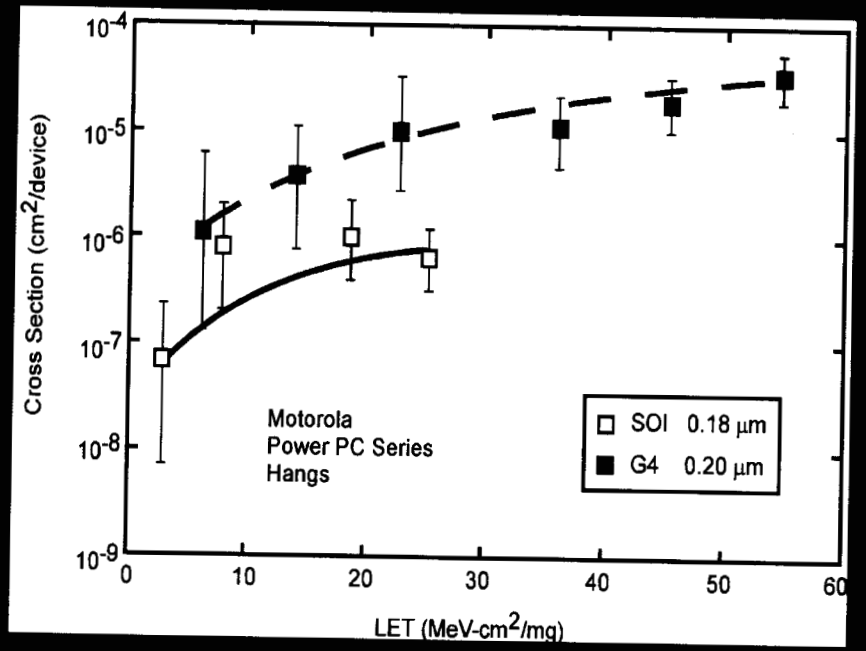


Cache Tests for SOI Processor with Different feature Sizes

- SOI PowerPC 7457
  Feature Size (0.13 μm)
  Core Voltage 1.3 V
- SOI PowerPC 7455
  Feature Size (0.18 μm)
  Core Voltage 1.6 V
- Good agreement between two sets of data

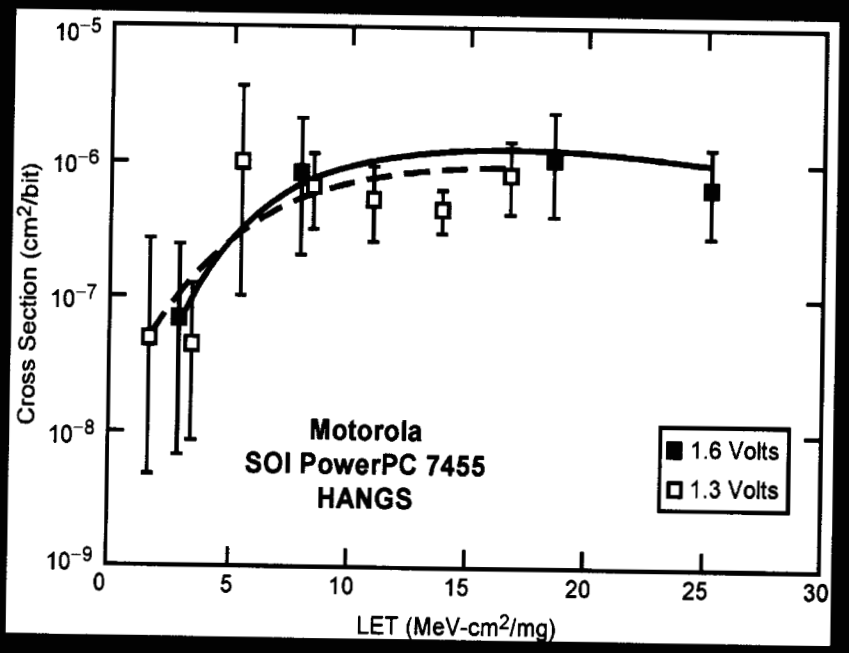


Hangs



Comparison of Bulk/epi with SOI

SOI 7455 device with different core voltage specification



- The cross section is lower by factor of 10 compare to bulk/epi results
- The cross section per device is 10^{-6}
- The threshold LET is low
- Upset rate is ~1 in 25 years for GCR

Register Dynamic Test

- Load a register with the operand 0x55555555
- Load the next register with operand 0x2
- Multiply the registers together and write the result into the first register.
- Increment the register pointer
- Repeat the step 1 to 3, until all the registers hold multiplication results.
- Read the entire registers and check that the result agrees with expected value of 0xaaaaaaaa.
- If not, then log the result to external memory as a strip chart (for later read out after the current irradiation is complete).

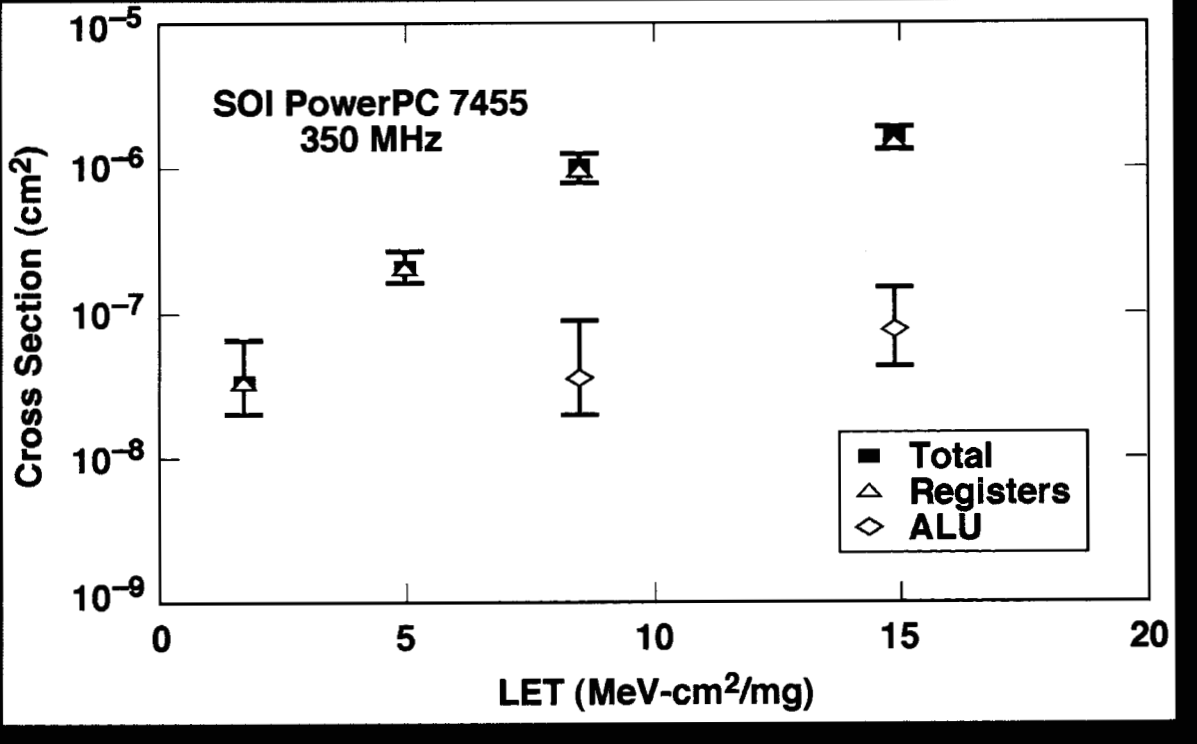
Register Dynamic Test

- The test passes and no upset is recorded
- The result does not match the expected value, but only one or two bits are wrong so this is counted as a *register* upset
- The result does not match the expected value, but many bits are erroneous which is counted as *processing unit upset*

Registers Dynamic Results

Motorola PowerPC 7455 in a dynamic mode 350 MHz clock frequency.

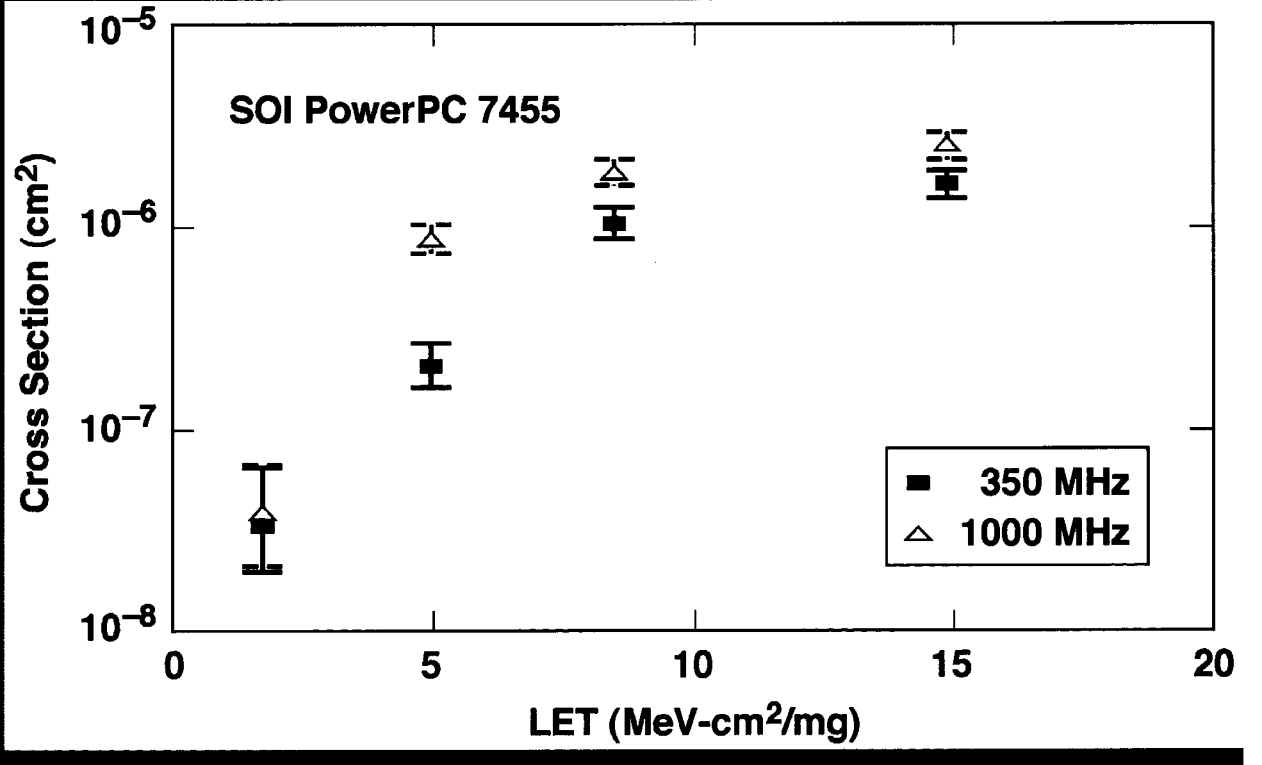
Clearly, the main contribution to the SEU is from the upsets in the registers. However, there is also some contribution from the ALU unit to the SEUs at higher LETs



Register Dynamic Results

Motorola PowerPC 7455
at two clock freq.
350 and 1000 MHz.

At very low LET
counting statistics
prevent conclusive
interpretation.
However, for the
higher LETs the results
with 1000 MHz clock
frequency are
systematically larger
by almost a factor of 2



Conclusion

- SOI processors have error rates that are more than 30 times lower than PowerPC 750 because of reduced feature size and the transition to SOI
- Asymmetric cross sections were observed for registers in the SOI processors, but not for D-Cache
- There is no change in SEU cross section for one type SOI processor with core voltage specification of 1.3 and 1.6 V
- Scaling between 0.18 and 0.13 μm feature size appears to have little effect on SEU sensitivity.
- Clock frequency dependence were observed for registers in dynamic measurement.