

# IBM PowerPC 405 SEU Mitigation Using Processor Voting Techniques in Xilinx Virtex-II Pro FPGA

Mandy M. Wang  
Jet Propulsion Laboratory  
California Institute of Technology  
Pasadena, CA 91109  
mandy.wang@jpl.nasa.gov

Gary S. Bolotin  
Jet Propulsion Laboratory  
California Institute of Technology  
Pasadena, CA 91109  
gary.s.bolotin@jpl.nasa.gov

*does it have*

*Abstract* – Not until recently, Xilinx has developed a new field programmable gate array (FPGA) device family, Virtex-II Pro. In this single device, not only ~~it has~~ high density logic cells (3K to 125K), gigabit connectivity, on-chip memory, digital clock management, but also it can have up to four IBM PowerPC 405 Processor hard cores, running up to 400MHz and 633Mbps. To utilize this cutting-edge device in space applications, a few Single-Event Upset (SEU) mitigation techniques need to be implemented to a design for the device. At Jet Propulsion Laboratory (JPL), we have successfully demonstrated the feasibility of running multiple processors running in a lock step fashion to accomplish SEU mitigation and fault tolerance.

demonstration the feasibility and capability of the proposed system: CPU board and MTR board. CPU board is an implementation of the proposed general purpose platform based on the Xilinx Virtex-II Pro FPGA family. MTR board is a motor driver board that interfaces between the CPU board and the motors. It's used to demonstrate the ease of leveraging the general platform in a specific application. The processor voting techniques discuss in this paper will be implemented on the CPU board.

## TABLE OF CONTENTS

1. TASK BACKGROUND
2. DESCRIPTION OF VIRTEX-II PRO FPGA
3. RADIATION CHARACTERISTICS
4. MITIGATION STRATEGIES
5. DESIGN OF DUAL PROCESSOR VOTING
6. CONCLUSION AND FUTURE WORK
7. REFERENCES

## 2. DESCRIPTION OF VIRTEX-II PRO FPGA

The Virtex-II Pro is the next generation of the Virtex II family with embedded IBM PowerPC 405 Processor hard cores (PPC405), and RocketIO™ Multi-Gigabit Transceivers (MGT) pins. It natively supports the low voltage differential signaling (LVDS) serial interface on hundreds of signal pairs and is capable of running real time operating systems: VxWorks and MontaVista Linux, on its embedded PowerPC processor(s). There could be as many as four embedded processors on a single FPGA, each running at speed up to 400MHz, 600+ DMIPS. In addition, each RocketIO™ MGT is capable of supporting data rates up to 3.125 Gb/s for high-speed serial transmission standards like Gigabit Ethernet, InfiniBand, RapidIO and PCI Express.

## 1. TASK BACKGROUND

This work is part of a mobility avionics task that aims to develop a scalable, configurable, and highly integrated 32-bit embedded platform capable of implementing computationally intensive signal processing in space flight instruments and systems. This platform is designed to service the need of both small and large spacecraft and planetary rovers that will operate within moderate radiation environments. Some of the key characteristics of this platform are its small size, low power, high performance, and flexibility. This estimated 10 fold reduction in both size and power over state-of-the-art processing platforms will enable this new product to act as the core of a low-cost mobility system for a wide range of missions.

Furthermore, the task will deliver the infrastructure to support the development of such avionics packages including testbeds, tools, system software, and IP libraries. In the near future, two prototype boards would be built to

## 3. RADIATION CHARACTERISTICS

Using Xilinx FPGA on flight project is not new. An early generation of Xilinx FPGA, Virtex, has been used on Mars Exploration Rover's DC motor controller.

To design an effective SEU mitigation solution for the Xilinx Virtex-II Pro, we must know the radiation properties of the Virtex-II Pro. The SEU susceptible areas of Virtex-II Pro's can be logically divided into the following categories: Flip-flops, Configuration Memory, Block SelectRAM, PPC L1 cache, and PPC internal registers. Each of these areas of susceptibility has its own fault statistics and requires its own mitigation method. We derived SEU rates for each of the categories based on experimental data that were obtained from a previous SEU susceptibility test done on the Virtex-II family<sup>[1]</sup>, which precedes the current Virtex-II Pro family. The following normalized upset rates are obtained as a

result: Flip-flops (3%), Configuration Memory (22%), Block SelectRAM (11%), and PPC L1 Cache (64%). Since Virtex II family doesn't have PPC processor, the L1 Cache value was calculated using the highest upset rate among the groups. Base on the upset rate and intrinsic characteristics of each category, the appropriate error detection and mitigation methods can be chosen accordingly.

#### 4. MITIGATION STRATEGIES

Technology development for the SEU mitigation effort has proceeded in stages, each stage consisting of research, application, implementation, and demonstration. We propose three major design stages: Simple Strategy, Robust Strategy, and Always Available Strategy, in the order of increasing complexity. The Simple Strategy involves developing a simple yet effective solution for non-critical systems as soon as possible. Robust Strategy is a refinement of the simple strategy aimed at producing correct results under all SEU circumstances but not necessarily in a time-critical fashion. Always Available Strategy satisfies the more stringent requirement of producing correct results under all SEU circumstances in a time-critical fashion. Time-critical implies that the success of the mission depend upon the data results being produced in a timely fashion with a small tolerance for delay of data. Each strategy is discussed in more detail below:

#### 4.1 Simple Strategy

The simple strategy targets the non-mission critical and non-time critical sub systems such as science data processor, image processor, and motor control. This strategy may use less than desirable techniques such as total device reset and reconfiguration as a means of error correction. In addition, the CPU might be relied upon to verify the integrity of the overall system. A single FPGA is used and the part count is minimal. This technique allows us to have a radiation hard solution while also providing us the opportunity to refine the technique for more complex situations. The design goal for this approach is to detect 98% of SEUs and mitigates all detected SEUs.

As discussed in previous sections, a FPGA can be logically divided into separate areas in terms of fault characteristics. Table 4-1 shows the proposed SEU mitigation techniques for each of the area type.

#### 4.2 Robust Strategy

For subsystems such as orbital CBH and micro-mobility controller, the correct system operation and the retention of the data are absolutely essential to the success of the mission but in a non time-critical manner. While Simple

	Effect	Detection	Indicator	Mitigation	SEU Injection
<b>Processor:</b>					
Cache	Incorrect software execution or output data	Processor Comparison at the Coreconnect Bus	External FF or internal FF	Processor Reset	Software injection
Processor Registers	Incorrect software execution or output data	Processor Comparison at the Coreconnect Bus	External FF or internal FF	Processor Reset	Software injection
Coreconnect Bus Interfaces	Incorrect cache read or I/O operations	Processor Comparison at the Coreconnect Bus	External FF or internal FF	Processor Reset	Software fault injection for registers. Hardware injection logic for signal lines
<b>Configurable Logic:</b>					
Function Generator 1) as LUT or ROM 2) as distributed RAM	Transient errors signals Incorrect data or software execution	TMR as appropriate Use TMR as appropriate or software error trap	Voter with mis-match F/F Software error trap	Fault Masking by TMR Reload code from non-volatile memory or use check pointing and rollback	Configuration memory injection Software injection
Flip-Flops	Incorrect software execution or data output	TMR as appropriate	Voter with mis-match F/F	Fault Masking by TMR	Software injection
Block RAM	Incorrect software execution or data output	EDAC as appropriate	Low Level Interrupt	Error Correction	Independently writable EDAC bits
<b>Configuration Memory:</b>					
Configuration Memory Content	Hardware implementation get altered	Configuration memory scrubbing with separately stored checksum	Check by software	Device Reset	Modify configuration memory
Configuration Registers	Incorrect configuration	CRC in configuration process	CRC register	Device Reset	Use configuration command to modify CRC register
Clock	1) registers changed inadvertently by clock glitch 2) Frequency change	Use dual clock signals directly derived from a single external source, and use counter in each clock and compare them	Counter mismatch F/F	Reset the clock multiplier and divider to original value	Change clock multiplier and divider by software. Use hardware fault injection logic on clock lines.
<b>I/O Blocks</b>					
Rocket I/O	Incorrect I/O operation/data	Built-In CRC		Retry the I/O operation	Hardware injection logic at the I/O signals
General I/O	incorrect I/O operation/data	protocol or handshake. Use redundant I/O signals might be used as appropriate.		Retry the I/O operation if error is detected	Hardware injection logic at the I/O signals

Table 4-1 – Simple Strategy

Strategy falls short in meeting this requirement, Robust Strategy offers a satisfying solution. Robust strategy will rely on redundancy for SEU checking in an autonomous fashion and techniques such as total device reset and reconfiguration are still acceptable. The proposed mitigation scheme is a dual FPGA system: one being the COS Xilinx FPGA and the other being radiation hardened SEU immune FPGA such as Actel 54SX72. The SEU immune FPGA is dedicated to the task of verifying the health, status and configuration correctness of the Xilinx FPGA. This approach offers several advantages over that of the Simple Strategy:

- Increase in processing margin
- Potential Power Savings
- Processors can be disabled if necessary.

The design goal is to detect 99.99% of SEUs and mitigate all detected SEUs.

(Attach block diagram show in the Quarterly Review here):  
 (Attach table of detailed SEU mitigation strategy here once it's ready)

#### 4.3 Always Available Strategy

Always Available Strategy is a refinement over the Robust Strategy and can be used to handle the most mission critical and time critical subsystems such as EDL controller. The design goal is to detect 99.99% of SEUs and mitigate all detected SEUs within 10ms or hot swap to a standby system for recovery within 5 seconds. Techniques such as total device reset and reconfiguration are obviously not

acceptable due to the time constraint. One possible solution is to have a system consists of two identical Xilinx FPGA devices where one serves as the standby for the other. The standby FPGA device is configured and available at all time and checks for the health and status of the main device.

(Attach block diagram show in the Quarterly Review here):  
 (Attach table of detailed SEU mitigation strategy here once it's ready)

### 5. DESIGN OF DUAL PROCESSOR VOTING

With the availability of multiple embedded PPC processors on the Xilinx Virtex-II Pro FPGA, processor voting can be an effective method for single fault detection and correction. By comparing results calculated from multiple processors executing the same program, a mismatch signals the presence of a fault. This comparison can be pair-wise, or it may involve three or more processors simultaneously. Figure 5-1 depicts a high-level block diagram of a pair-wise single fault detection scheme. Primary PPC405 is the active CPU of the system, and secondary PPC405 is the checker, whose outputs do not pass to the system. Three sets of bus are compared inside the comparator: output data bus from the data unit, address bus from the data unit, and address bus from the instruction unit. These data will be latched into the comparator first. Once a fault is detected by having a mismatch on any of the buses, both processors will be notified through the interrupt mechanism, and appropriate actions could be taken depending on the application.

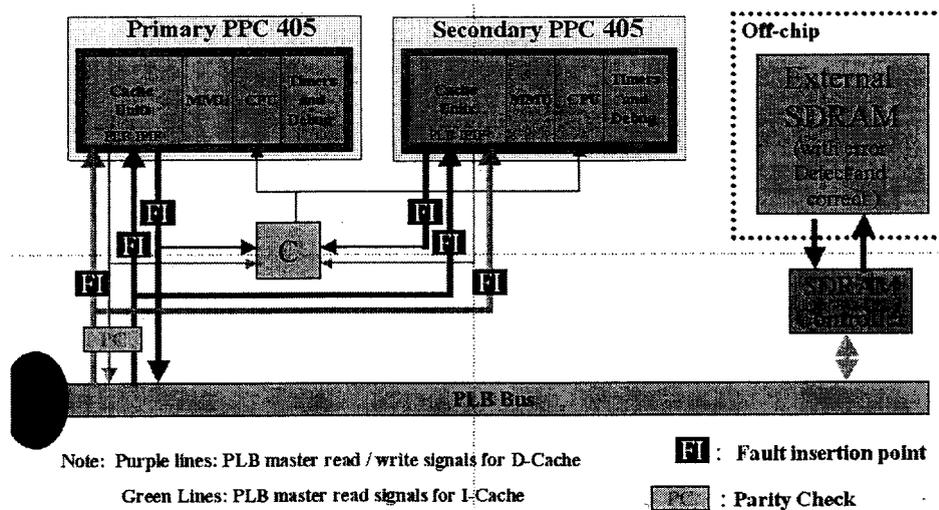


Figure 5-1 – Dual Process Voting Block Diagram

## 5.1 Simulation

Both RTL and timing simulation of the design were performed in ModelSim version 5.7c. Figure 5-2 illustrates the voting mechanism working in timing simulation.

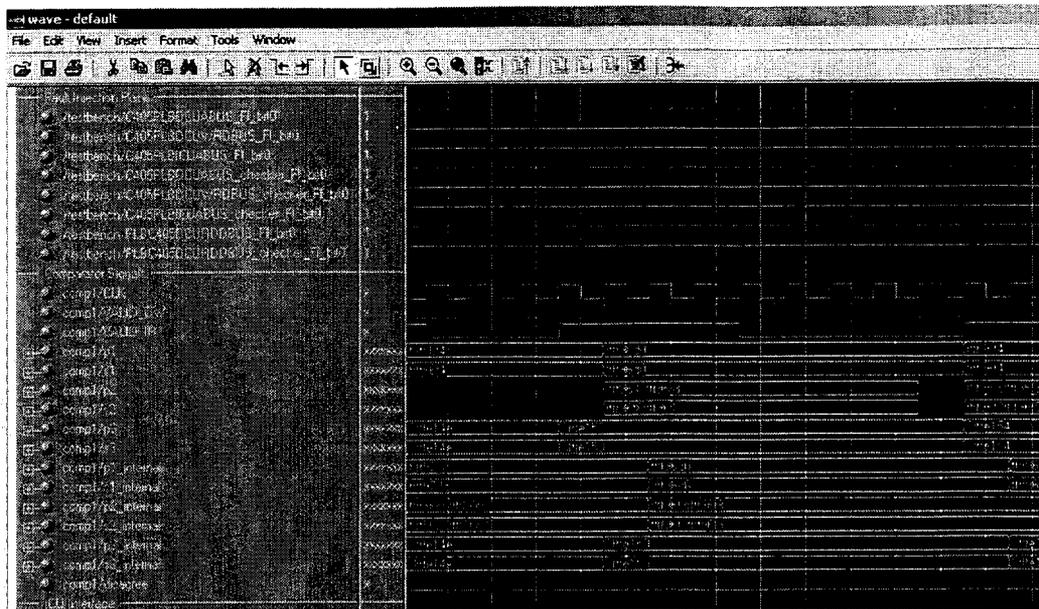


Figure 5-2 – Dual Process Voting Block Diagram

## 5.2 Board-Level Test

Board level test of such a processor voting scheme was conducted on a Xilinx Virtex-II Pro Prototype board using X2VP20-FF1152 device. A simple firmware version of the famous “Hello World” application together with an incrementing counter was loaded on to the Block RAM of the system to monitor CPU’s running status. The counter’s value would set back to zero once the comparator detects a fault. Furthermore, a serial port decoder was implemented to inject single fault (see Figure 1) to the system. Figure 5-3 shows a LabView front panel designed to communicate with the test board. The top left block of the panel includes eight preprogrammed push buttons used for injecting fault to instruction line’s data busses and data line’s address and data busses, and a type-in command window for newly programmed injecting point. The top right block of the panel is an output terminal used to monitor CPU’s output statement coded in the firmware. Once a fault is injected into the system, the output terminal will respond with a counter reset, and the mismatch LED will be turned on.

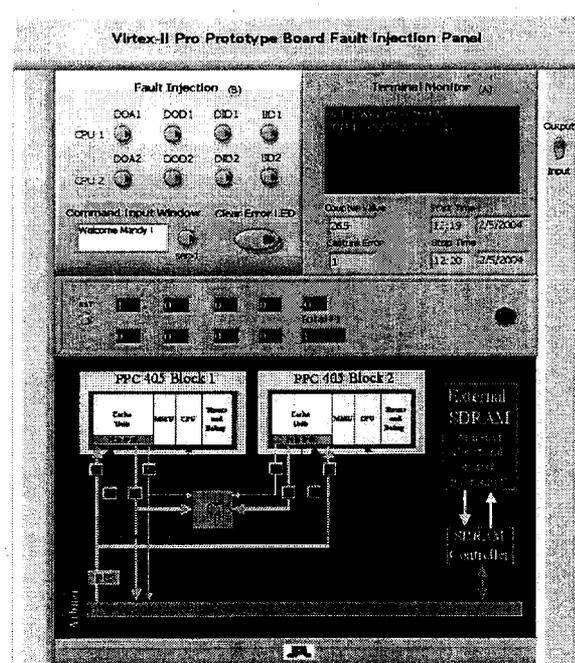


Figure 5-3 – Dual Process Voting Block Diagram

## 6. CONCLUSION AND FUTURE WORK

Recent advances in semiconductor technology have enabled commercially available FPGA to have multiple embedded micro-processor cores. In this study, we have demonstrated the effectiveness of processor voting as a SEU mitigation technique for the embedded PowerPC

processors on the Xilinx Virtex-II Pro FPGA family devices. RTL simulation in ModelSim and prototype testing using LabView shows that functional errors due to SEU can be detected by utilizing processor voting using two processors running in lockstep. Appropriate to address the errors. These initial results are encouraging and demonstrate that FPGA with embedded processor cores are suitable for space applications.

More thorough testing is needed to further confirm the current results. Planned work includes proton and heavy iron based radiation test of the prototype system as well as building more complex test cases to stress test all aspects of the PowerPC processor core.

## 7. REFERENCES

- [1] C. Yui, G. Swift, C. Carmichael, R. Koga, J. George, "SEU Mitigation Testing of Xilinx Virtex II FPGAs," data workshop paper, Nuclear and Space Radiation Conference (NSREC), 2003.