TID, SEE and Radiation Induced Failures in Advanced Flash Memories

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Abstract – **We report on TID and SEE tests of multi-level and higher density flash memories. Stand-by currents and functionality tests were used to characterize the response of radiation-induced failures. The radiation-induced failures can be categorized as followings: SEU read errors during irradiation, stuck-bit read errors verified post-irradiation, write errors, erase failures, multiple upsets, and single-event latch up.**

I. INTRODUCTION

Non-volatile memories have been used widely in commercial as well as space applications. One of the many members of the non-volatile class of memory devices is the flash memory. Flash memories have been found in solid-state recorders of space mission systems. Previous solid-state recorders were designed around reliable, robust and radiation-hardened dynamic random access memories (DRAM) but current recorders for space missions are being built with component-off-the-shelf flash memory devices. Flash memories can retain stored data for many years in the absence of applied power and do not require to be refreshed within certain short period of time.

There are two basic structures of the flash memory devices, NOR and NAND architecture. The NOR structure provides direct access to individual cells at the expense of the cell areas because of the need for contacts at each drain and source connections as shown in figure 1. The NAND structure is more compact since it does not provide contacts to individual source and drain regions. Memory cells in the NAND structure require reading and writing through the other cells in the stack, an architecture that results in inherently slower cell access as shown in figure 2. Both architectures have the same basic storage element (consisting of a control gate stacked over an isolated polysilicon gate in the gate oxide known as a floating gate, a source, and a drain), it is the interconnection of these memory cells that distinguishes the structure. Data can be interpreted as "0" when charges (electrons) are placed in the floating gate. When electrons are removed from the floating gate, data become "1". The configuration is known as single level or one-bit-per-cell storage since the read-out data can be identified either as "1" or "0". In terms of cell threshold voltage, a sense-amp circuitry recognizes "1" optimally at the level of 2.7 volts and "0" at 5.7 volts as shown in figure 3a. In order to obtain higher density, flash memory structures have been scaled down in size. But the scaling process reached its limitation at cell size of 0.13μm. Another limitation is the operating voltage range, channel hot electron injection devices (NOR structure) require 10 to 12V while the Fowler-Nordheim tunnel devices (NAND structure) need 18 to 20V for program and erase [1].

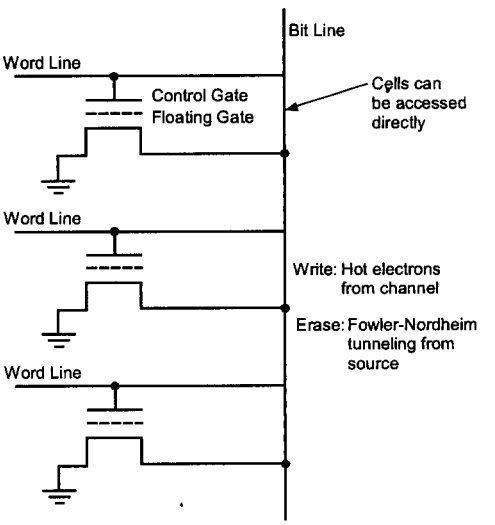

Figure 1: NOR structure with drain and source connections per cell.

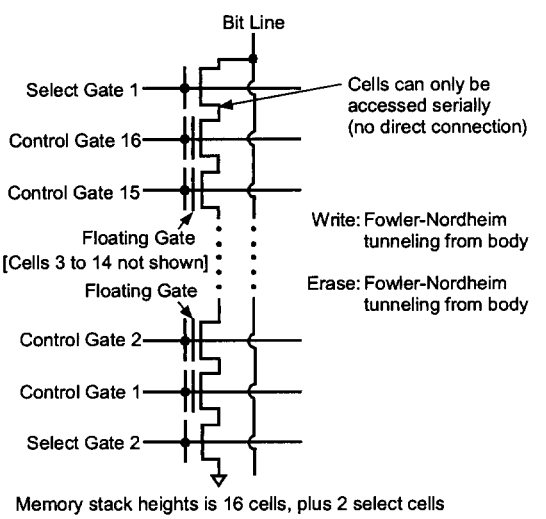

Figure 2: NAND structure

Instead of scaling, an alternate method of storing more than one bit per cell (or multi-level charge storage)

provides a new solution. Figure 3b shows threshold voltage distributions for single and multi-level storage methods [2]. To recognize the four states "11", "10", "01", and "00" within the 6 volt-range, the control and verify circuitry to inject charge must have the finer resolution than the sensing circuitry of single level storage. The programming circuits must deliver precise amounts of electrons to the floating gate and the sense amps must distinguish between the four small threshold voltage regimes.

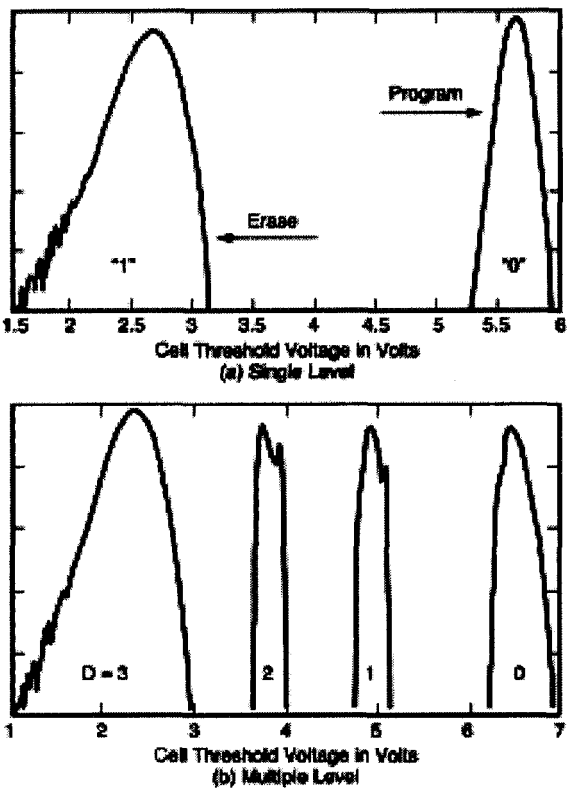

Figure 3: Cell threshold distribution

II. DEVICE DESCRIPTIONS

The NAND-based Toshiba 1 Gigabit flash parts organized as 528 bytes x 32 pages by 8192 blocks. Programming and read data are performed between the 528-byte static register and the memory cell array in 528-byte increments. During program and read mode, the page can be separated into three sections by the use of an internal pointer. The erase operation is implemented in block increments. The serial read cycle is 50ns and the access time of cell array to register is 25 microsecond. Toshiba devices were built on the 0.16-micron process technology.

The Intel 3 Volt-Synchronous StrataFlash 256Mbit devices provide the highest density NOR-based flash memory available commercially with two-bit per cell capability. The Intel device supports three different programming choices: word programming, write buffer programming, and buffered enhanced factory programming. The Intel parts were built on the 0.18-micron process technology. The sensing circuitry designed for the data read operation is also used for the program operation to ensure memory cell has charged with the desired levels.

Both NAND and NOR flash memory technology have internal charge pump generators to provide higher voltages than their external operating supplies, for the programming and erase operations. The Toshiba flash devices typically require 10 seconds to erase the whole part, but the Intel devices needs at least 180 seconds to perform the similar operation. The Toshiba devices operate with lower currents in all modes, up to 30mA compared to 78mA (single-word read) and 70mA (erase/program) for the Intel parts.

Six de-lidded parts were used for SEE testing (3 Intel, and 3 Toshiba). Seven parts were used for TID tests (3 Toshiba, 4 Intel). The date code is as follows: Toshiba TC58100FT with D/C 0240, Intel 28F256K3 with D/C 0238.

III. TEST SET-UP

SEE testing was done at Texas A&M and the Lawrence Berkeley National Lab (LBNL) cyclotrons. All tests were performed at 25 degree C. The test equipment is comprised of two PCs, a power supply, and an FPGA-based test board. One PC controls a HP6629A power supply. This allows precision voltage control and latch-up detection and protection since the PC has millisecond control over the operation of the power supply. A second, dedicated PC controls the test circuit board designed specifically to read errors and write commands/test patterns to the (device under test) DUTs. Parts are programmed with either with a pseudo-random pattern to mimic real data or with all zero. All zero pattern forces all floating gates in the device to be filled with electrons, consequently creates a worst-case leakage test. A depiction of the setup used is shown in Figure 4.

Total dose tests were done using the JPL cobalt-60 facility at the dose rate of 25 rad(Si) per second with a series of 1 or 2 krad(Si) steps and at 25 degrees C. The devices under test (DUT) were static biased during irradiation. Electrical parametric measurements, I_{IN} and I_{SB}, were made after each irradiation step with an Advantest test system. Functional tests consisted of the following sequences:

1. Erase, write, and read to validate stored data
2. Irradiate
3. Read pattern to ensure data retention
4. Erase, write complement data, read to validate
5. Repeat step 2.

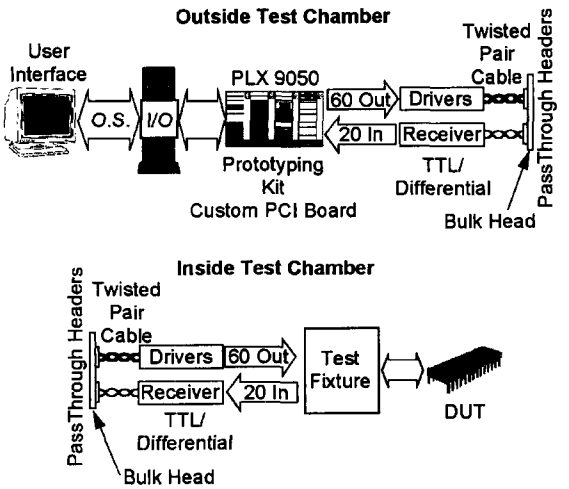

Figure 4: Test Set-Up

IV. Radiation Induced Failures

The overall operation of flash memories requires many clock cycles and commands just like the operation of most microprocessors because of the complex architectures, such as internal state machine, write buffer, and registers. The radiation-induced failures in flash memories can be categorized as followings: upset read errors during irradiation, stuck-bit read errors verified post-irradiation, write errors, erase failures, multiple bit upsets, and single event latch up (SEL). Single bit upset error can be caused by single ion hit the cell area, or in the readout buffer and register. The number of stuck-bit read errors remained for subsequent post-irradiation verifications. Write errors are confirmed when memory cell contents are compared to expected data during post-irradiation. Failure to erase can be defined as an unsuccessful removal of electrons from floating gates after a number of passes, or a failure of device's ready signal to inform the status register after a specified elapsed time. Single event upsets occurred in the state machine and registers (address, data, command, identifier) are very difficult to categorize and interpret because of the many entangled black-boxes inside the functional block. These upsets will mostly interrupt the intended operation and locked it into an unexpected event. The events can be classified as single event functional interrupt (SEFI). The selected operation can be suspended if encounters SEFI resulting with a current surge at a low LET. Devices can enter indefinite loop during erase or programming mode. Studies of SEFI had been done on microprocessors, digital signal processors (DSPs), electrically erasable programmable read only memories (EEPROMs), dynamic random access memory (DRAM), and synchronous DRAMs [3][4].

V. SEE Test Results

Three Intel parts are tested with negligible variation among them. Three operational modes are used during irradiation: read, write and erase. Figure 5 shows the erase SEFI upset cross-sections vs. LET during the dynamic erase operation. The threshold LET is at 12.5 MeV-cm^2/mg with the cross-section of 1.81E-6 cm^2.

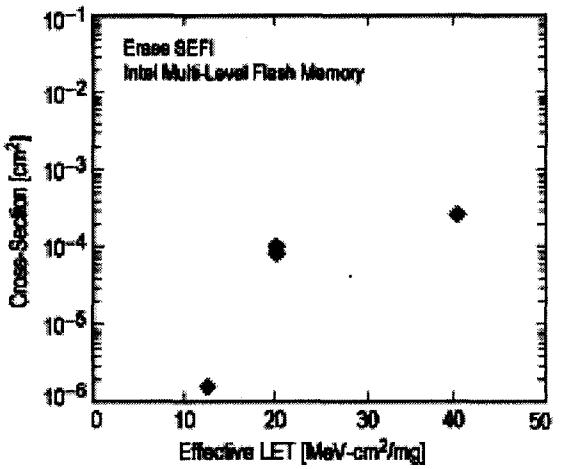

Figure 5: cross-section of SEFI erase upsets (Intel)

The threshold LET of write-upset errors is 6.51 MeV-cm^2/mg. Figure 6 illustrates the measured cross-sections of the Intel multi-level flash memory parts during the word-write operation.

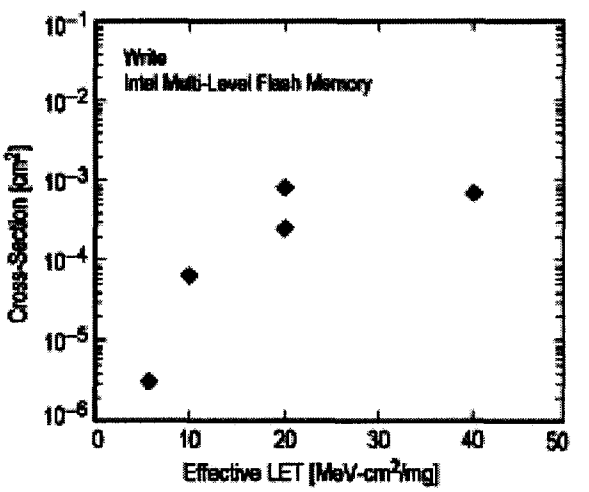

Figure 6: Cross-section of write-upsets (Intel)

The number of read-bit errors is precisely twice as the number of read-address errors at the following LET: 5, 8.65 and 13 MeV-cm^2/mg. Since the Intel devices store two bits per address indicating that the single ion strikes the cells. Figure 7 shows the cross-sections vs. LET during the read

mode. The threshold LET of read-upset errors is 5.64 MeV-cm^2/mg.

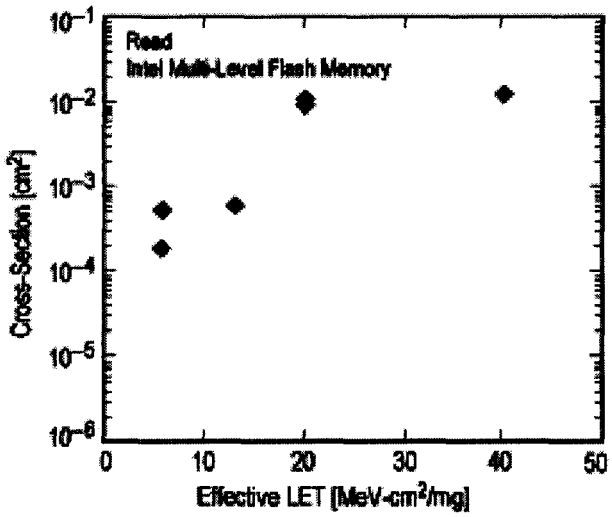

Figure 7: Cross-section of read-upsets (Intel)

Soft upset errors in read mode during irradiation are usually recovered in subsequent post-irradiation runs. But there are some read errors that cannot be re-written immediately. Figure 8 shows the stuck-read errors versus effective LET. The Intel device is susceptible to latch up at LET of 5.64 MeV-cm^2/mg.

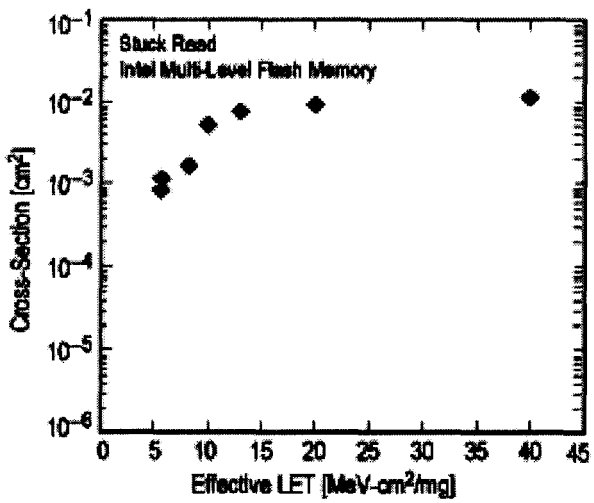

Figure 8: Cross-section of stuck-read upsets (Intel)

Three Toshiba flash devices are programmed with all zeros (the charge states in all memory cells) and are tested in vacuum during read operations, using ions with LET values from 3.3 to 30 MeV-cm^2 /mg, Neon, Argon, Copper, and Krypton. Some tests are performed at 30°, 45°, and 60° angles to increase the effective LET. The threshold LET of read-upsets is 6.88 MeV-cm^2/mg as shown in figure 9. SEFI-type events occur frequently during SEE runs.

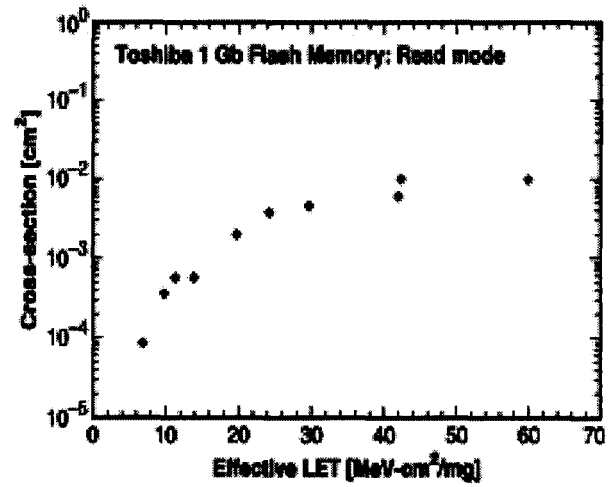

Figure 9: Cross-section of read upsets (Toshiba)

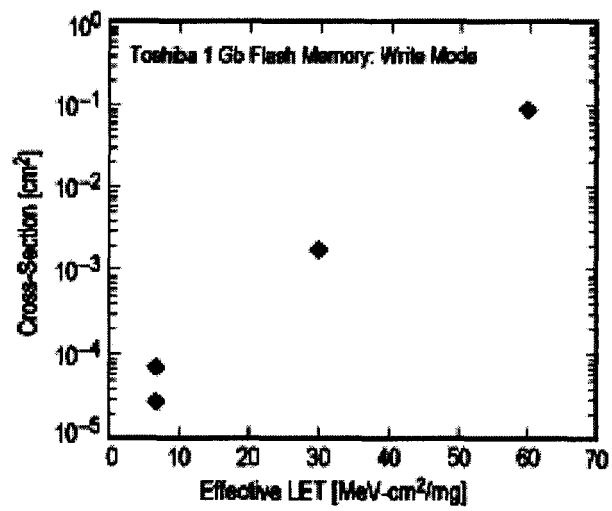

Figure 10: Cross-section of write upsets (Toshiba)

VI. TID TEST RESULTS

Measurements of the stand-by supply current are made after each irradiation step with the Advantest test system. The Toshiba flash memories are erased, then

written with zeros, and then read to validate stored data prior to the next exposure. After each irradiation, the devices are read to screen out errors. The erase/write/read loop restarts. The Toshiba 1Gb flash memories have read errors after the total dose of 14 krad(Si) as shown in figure 11. Data in one part flip both ways (0 to 1, and 1 to 0), while others change in one direction (0 to 1). All three parts fail to erase at this post-level. But after 12 hours of annealing at 3.3volts and 25 degree C, both parts can be erased again. But all fail to write after 48 hours anneal. The charge pump circuits of lower density NAND flash memory devices have been cited as the main cause of the erase and write failures at around 8 to 14 krad(Si) in previous publications [5][6]. Once again, the internal charge pump circuitry fails to provide the sufficient power for the write voltage.

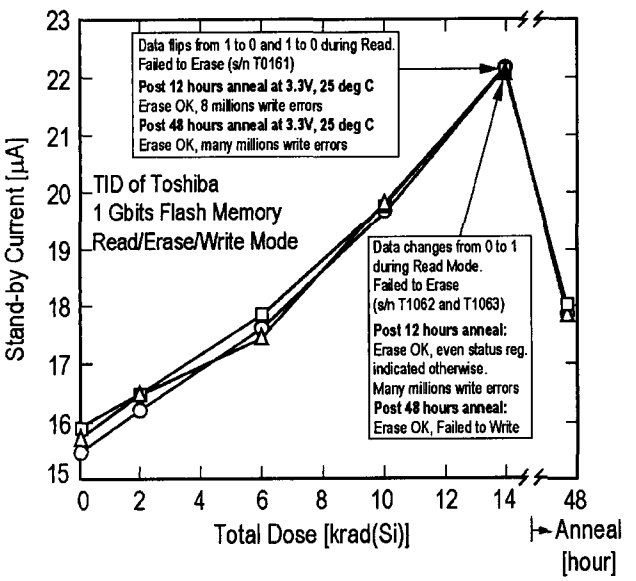

Figure 11: TID of Toshiba devices

Four Intel devices are selected into two groups of two for the TID tests. Two parts of the first group are tested with the read/erase/write mode. After 12 krad(Si), the stand-by current of both devices go over the specification limit of 80μA. As shown in figure 12, one device starts having three read and write errors. Finally, both parts fail to erase after 16 krad(Si). Post 48 hour anneal at 3.3volts and 25 degree C helps to recover the erase function of both devices. One part then is irradiated to 17 krad(Si) where it quits to erase.

Two parts of the second group are programmed with random pattern and irradiated with read mode only. After 8 krad(Si), a SEFI-type event occurs and suddenly there are millions of bit errors and address errors during the post-irradiation read. Recycling power eliminates the problem. Figure 13 shows the chronological order of an increasing number of read failures as the total dose accumulates. Stand-by currents of both parts go over the specification limits of 80μA after 11 krad(Si).

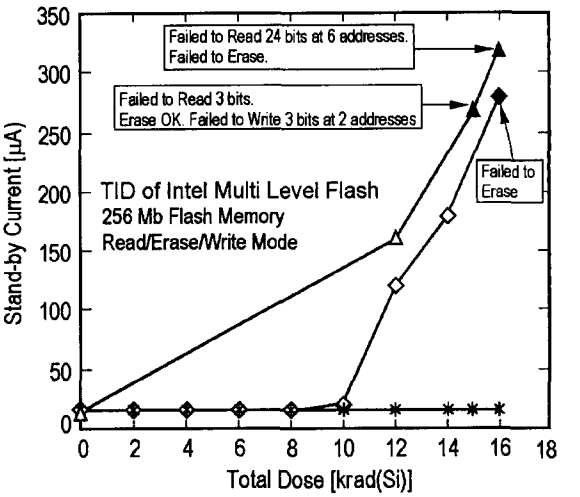

Figure 12: TID of Intel in Read/Erase/Write mode

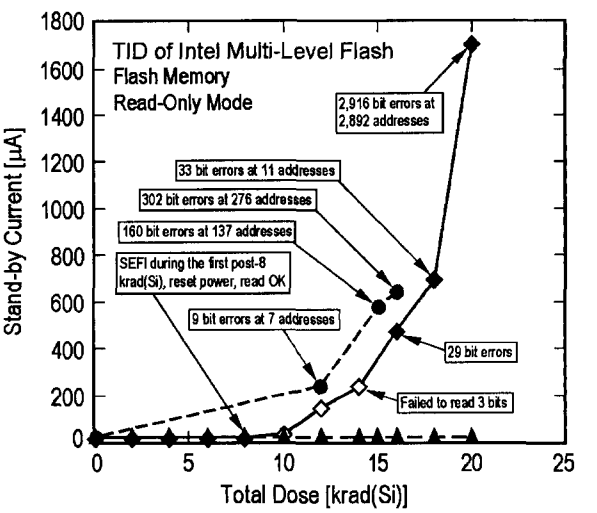

Figure 13: TID of Intel parts in Read-Only mode

VII. CONCLUSIONS

The Intel multi-level flash memory devices are susceptible to latch up at a very low LET. This would preclude its use in space unless the risk of mission failure is least concerned or the functional failures do not cause catastrophic chain reaction effects to the major system. The Toshiba NAND flash memory parts respond better with latch-up, but they fail to either erase or write at 14 krad(Si). The NAND flash memories inherited larger cross-sections in both read and write operations.

ACKNOWLEDGMENT

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I. REFERENCES

[1] S. Lai, "Tunnel oxide and ETOX flash scaling limitation",*Int'l Non-Volatile Memory Technology Conference,* p6.

[2] G. Atwood, et al," Intel StrataFlash memory technology overview," 1998 application note from Intel Corporation

[3] R. Koga, S.H. Penzin, K.B. Crawford, and W.R. Crain," Single event functional interrupt (SEFI) sensitivity in microcircuits," *Proceedings of RADECS97,* 311-318, 1997.

[4] R. Koga, P. Yu, K.B. Crawford, S.H. Crain, and V.T. Tran," Permanent single event functional interrupt (SEFI) in 128- and 256-megabit synchronous dynamic random access memories (SDRAMs)," *2001 IEEE Radiation Effects Data Workshop Record,* p6.

[5] D.N. Nguyen, S.M. Guertin, G.M. Swift, and A.H. Johnston," Radiation Effects on advanced flash memories," *IEEE Trans. Nucl. Sci.,* vol. 46, no. 6, pp. 1744-1750, Dec 1999.

[6] D.N. Nguyen, C.I. Lee, and A.H. Johnston," Total ionizing dose effects on flash memories", *1998 IEEE Radiation Effects Workshop Record,* p100.