TID, SEE and Radiation Induced Failures in Advanced Flash Memories

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Outline

- Non-Volatile Memory (NVM) types
- Test Set-Up
- Radiation Induced Failures
- SEE Test Data
- TID Test Results
- Conclusions
Flash Memory Types

- NOR (Intel)
- NAND (Toshiba)
Cell Threshold Voltage

(a) Single Level

(b) Multiple Level

D = 3

Cell Threshold Voltage in Volts

Program

Erase

"0"

"1"
Test Set-up

Outside Test Chamber

User Interface

Prototyping Kit
Custom PCI Board

PLX 9050

60 Out
Drivers

20 In
Receiver

TTL/Differential
Bulk Head

Pass Through Headers

Inside Test Chamber

Twisted Pair Cable

Drivers 60 Out

Receiver 20 In

TTL/Differential

Bulk Head

FPGA based Test Board

DUT
Test Conditions

- Single Event Upset (SEU): Erase, Write, Read
- Single Event Latch-up (SEL): Read
- Ions used: Ne, Ar, Cu, and Kr
- Total Ionization Dose (TID): biased condition
- Source used (in TID): Cobalt-60
- Dose rate (in TID): 25 rad(Si) per second

Intel StrataFlash (D/C 0238) 28F256K3
Toshiba (D/C 0240) TC58100FT
## Radiation Induced Failures

<table>
<thead>
<tr>
<th>Errors</th>
<th>Description</th>
<th>Signature</th>
</tr>
</thead>
<tbody>
<tr>
<td>Single Event Functional</td>
<td>Interrupt intended operations and/or locked into unexpected endless loops</td>
<td>Operations lock up. Reset mostly with power cycling.</td>
</tr>
<tr>
<td>Interrupt (SEFI)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Read</td>
<td>Read errors during irradiation.</td>
<td>Two errors per address in case of multi-level cells</td>
</tr>
<tr>
<td>Erase</td>
<td>Unsuccessful removal of electrons or long elapsed erase time.</td>
<td>Many passes prior to erase successfully</td>
</tr>
<tr>
<td>Write</td>
<td>Wrong data written to devices, or no access to the entire block.</td>
<td>Elapsed write time varies grossly from blocks to blocks</td>
</tr>
<tr>
<td>Stuck read</td>
<td>Errors remained in subsequent post-irradiation verifications. Initial data came back after several weeks.</td>
<td>No prediction</td>
</tr>
</tbody>
</table>
SEFI (Erase mode - Intel)

Erase SEFI
Intel Multi-Level Flash Memory

Cross-Section [cm²]

Effective LET [MeV-cm²/mg]
Read-upsets (Intel)

![Graph showing cross-section vs. effective LET for Intel Multi-Level Flash Memory.](image-url)
Write upsets (Intel)

Cross-Section [cm²]

Effective LET [MeV·cm²/mg]

Write
Intel Multi-Level Flash Memory
Stuck-read upsets (Intel)

Graph showing the relationship between Cross-Section [cm²] and Effective LET [MeV-cm²/mg].

Stuck Read
InteL Multi-Level Flash Memory

Cross-Section [cm²]

Effective LET [MeV-cm²/mg]

DNN-11, 10-Oct-03
Write upsets (Toshiba)

Toshiba 1 Gb Flash Memory: Write Mode

Cross-Section [cm²]

Effective LET [MeV-cm²/mg]
Read upsets (Toshiba)

Toshiba 1 Gb Flash Memory: Read mode

Cross-section [cm$^2$]

Effective LET [MeV-cm$^2$/mg]

DNN-13.10-Oct-03
TID results (Intel read mode)

TID of Intel Multi-Level Flash
Flash Memory
Read-Only Mode

- 33 bit errors at 11 addresses
- 302 bit errors at 276 addresses
- 160 bit errors at 137 addresses
- 9 bit errors at 7 addresses
- SEFI during the first post-8 krad(Si), reset power, read OK
- 29 bit errors
- Failed to read 3 bits

Stand-by Current [μA] vs. Total Dose [krad(Si)]
TID results (read/erase/write)

Failed to Read 24 bits at 6 addresses. Failed to Erase.

Failed to Read 3 bits. Erase OK. Failed to Write 3 bits at 2 addresses

TID of Intel Multi Level Flash
256 Mb Flash Memory
Read/Erase/Write Mode

Stand-by Current [μA]

Total Dose [krad(Si)]
Data flips from 1 to 0 and 1 to 0 during Read. Failed to Erase (s/n T0161)
Post 12 hours anneal at 3.3V, 25 deg C
Erase OK, 8 millions write errors
Post 48 hours anneal at 3.3V, 25 deg C
Erase OK, many millions write errors

Data changes from 0 to 1 during Read Mode. Failed to Erase
(s/n T1062 and T1063)
Post 12 hours anneal:
Erase OK, even status reg. indicated otherwise.
Many millions write errors
Post 48 hours anneal:
Erase OK, Failed to Write
Conclusions

- Intel StrataFlash:
  - TID ~ 15 krad(Si)
  - SEL ~ 10 MeV-cm² / mg

- Toshiba:
  - TID ~ 15 krad(Si)
  - No observed SEL at 25° C (60 MeV-cm² / mg)

- Both are prone to SEFI