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**Highly Parallel and Systolic Computation by  
Arrays of Quantum Dots Cellular Automata:  
Application to Wavelet Transforms**

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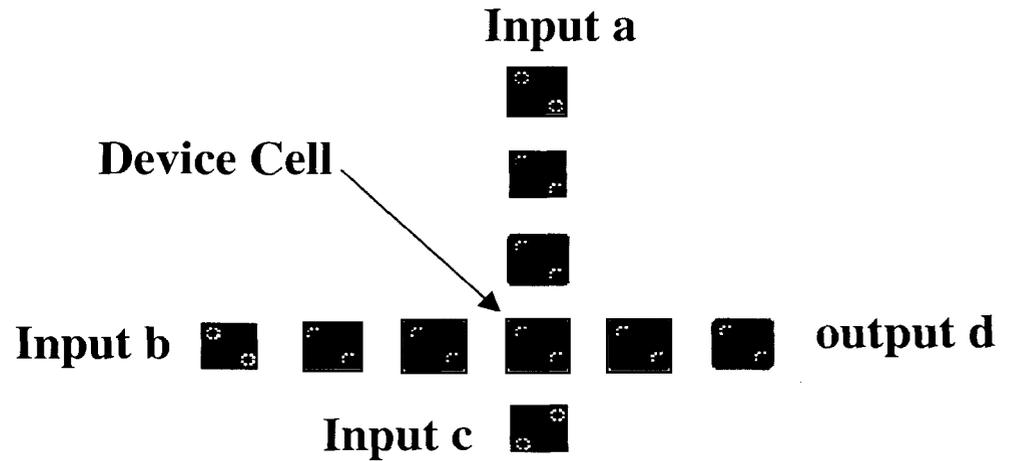
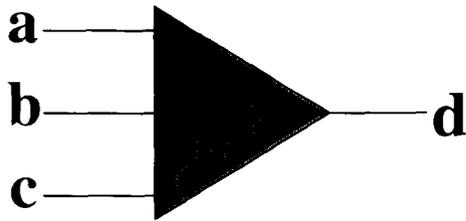
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California Institute of Technology**

# Computation with QCA Array

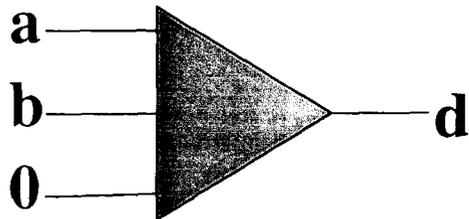
## Basic Logic Gate: Majority Gate

*Majority* gate, an intrinsically simple gate to implement by QCA

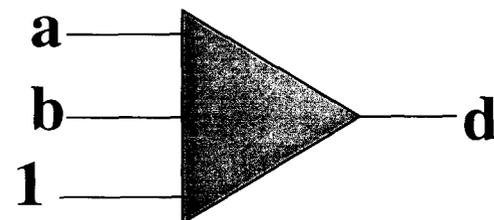


Majority Gate: Schematic

Majority Gate: QCA Implementation



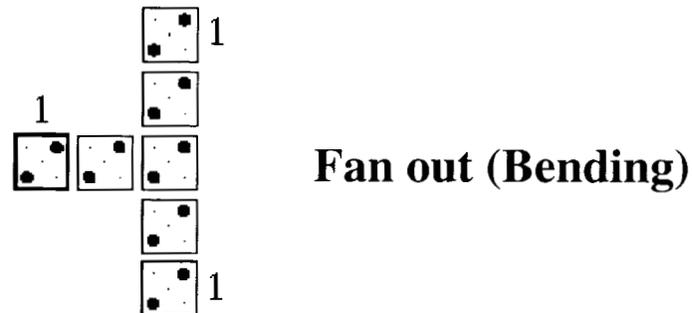
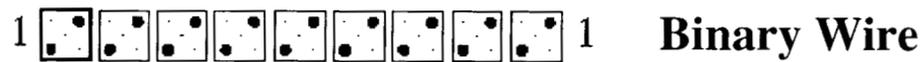
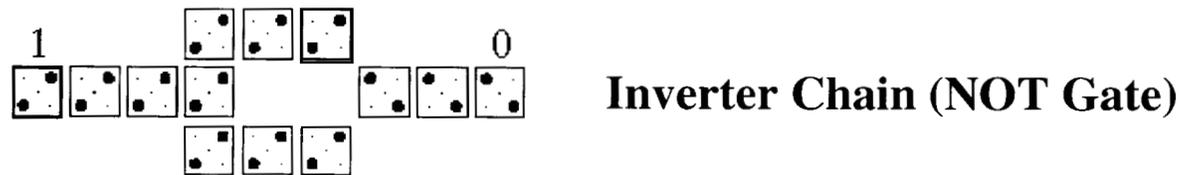
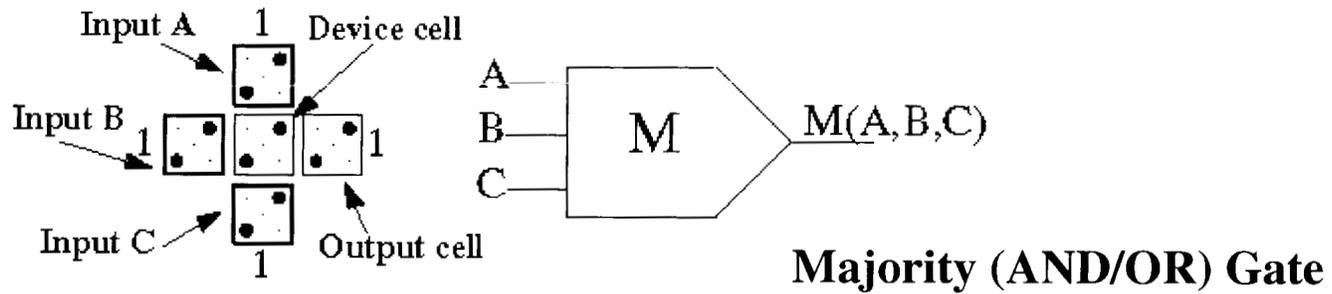
And Gate



Or Gate

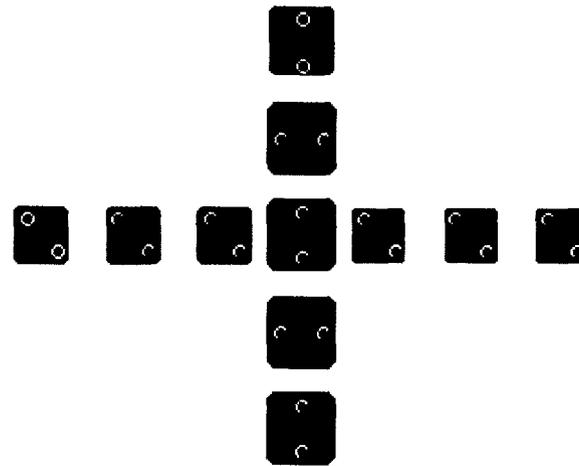
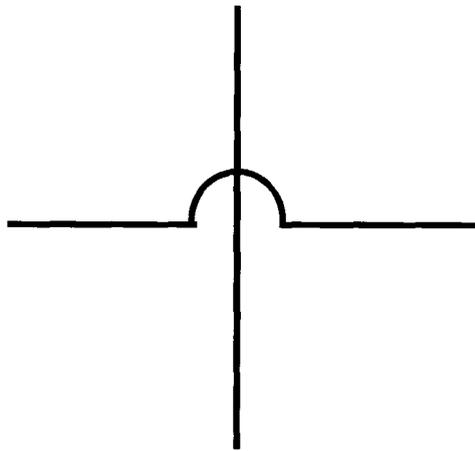
# Background on Quantum Dots Based Computation

## Wires and Gates (Universal Gates)



# Background on Quantum Dots Based Computation: More than Wires and Gates

QCA can overcome a *major limitation* of VLSI by *enabling coplanar* line crossing

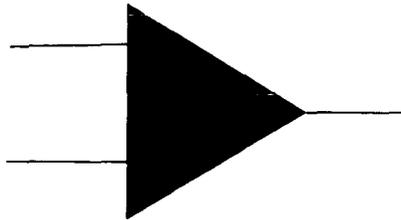


- Allowing the design of brand new architectures.
  - Enable some applications that would have been either *impossible* or *extremely costly* using conventional VLSI

# Computation with QCA Array

## Possibilities and Advantages: Computing on Wire

VLSI

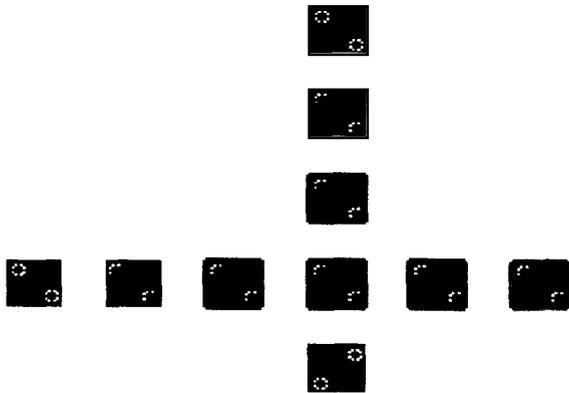


Gate (Si)

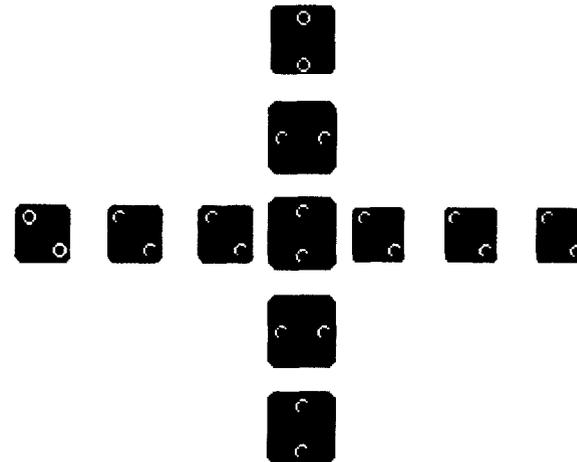


Wire (Metal)

QCA



Majority Gate (QD Cell)



Wire (QD Cell): Co-Planar Line Crossing

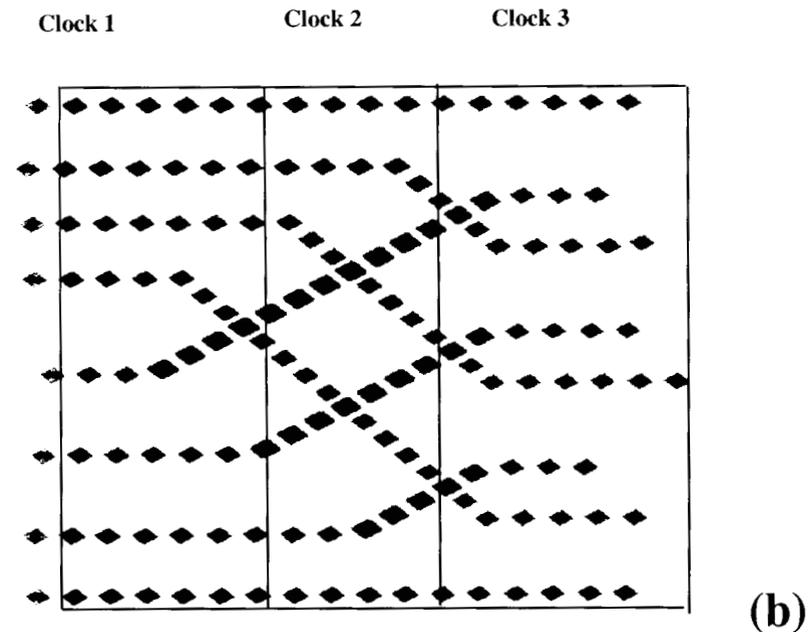
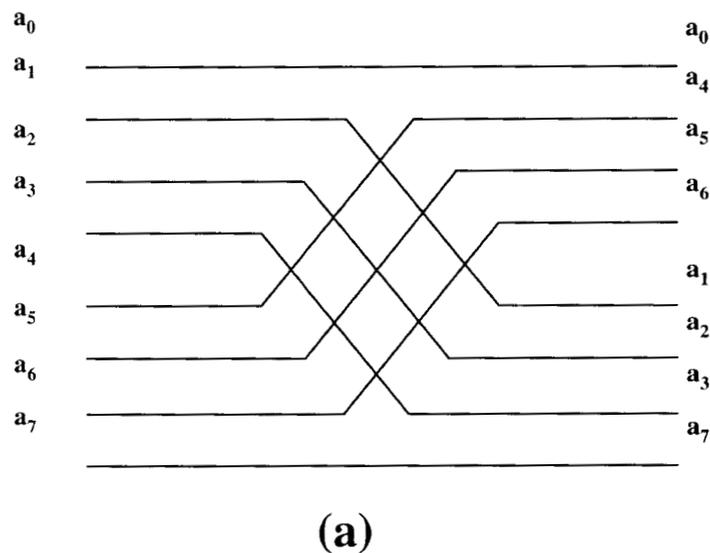
**Other Potential Advantages over VLSI:**

**Higher density, lower power consumption, harder radiation**

# Novel QCA Circuits

## Direct Implementation of Data Permutation Matrices

**QCA circuits for Co-planar and Direct Implementation of Permutation Matrices:  
Perfect Shuffle Permutation Matrix**



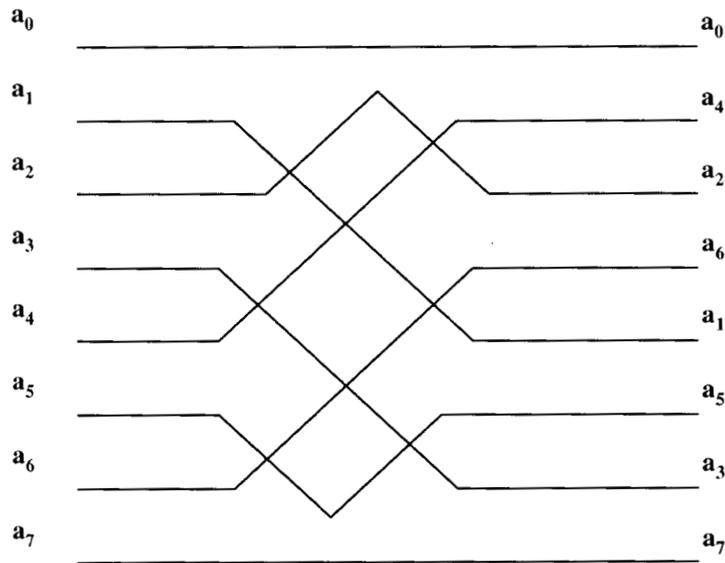
**Implementation of Permutation Matrix  $\Pi_8$**   
 a) Schematic                      b) QCA Circuit

**QCA circuit for implementation of Perfect Shuffle Permutation Matrix plays a major and enabling role in systolic computation of FFT, Wavelet and Walsh-Hadamard**

# Novel QCA Circuits

## Direct Implementation of Data Permutation Matrices

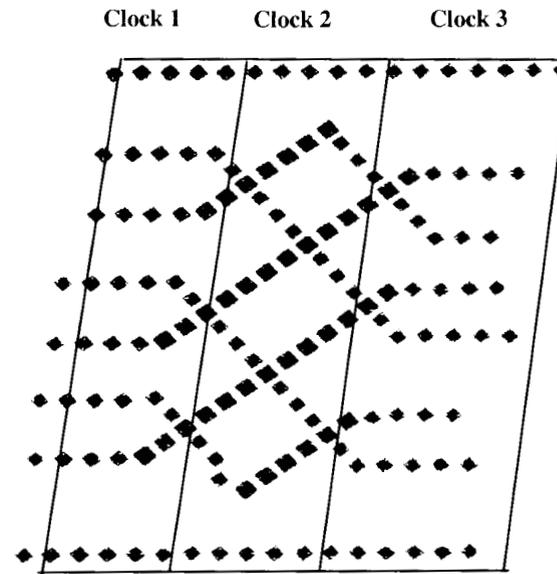
### QCA circuits for Co-planar and Direct Implementation of Permutation Matrices: Bit-Reversal Permutation Matrix



(a)

Implementation of Permutation Matrix  $P_8$

a) Schematic



(b)

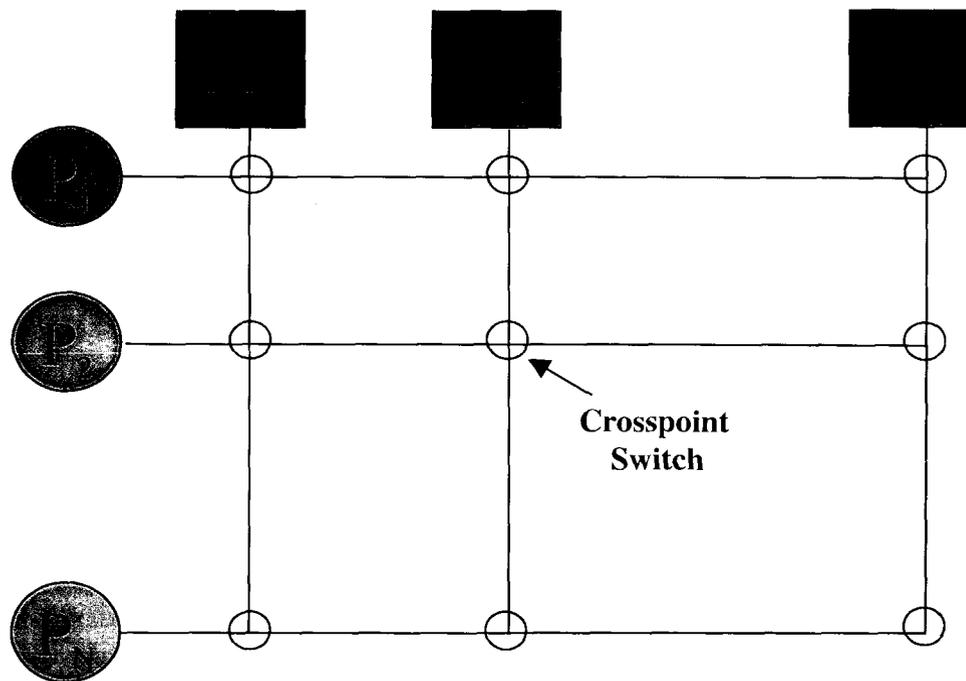
b) QCA Circuit

QCA circuit for implementation of Bit-Reversal Permutation Matrix plays a major and enabling role in systolic computation of FFT

# Novel QCA Circuits

## Co-Planar Implementation of Interconnection Networks

QCA circuits for Co-planar and Compact Implementation of Crossbar Network as the most general mechanism for connecting  $N$  processors to  $N$  memory modules



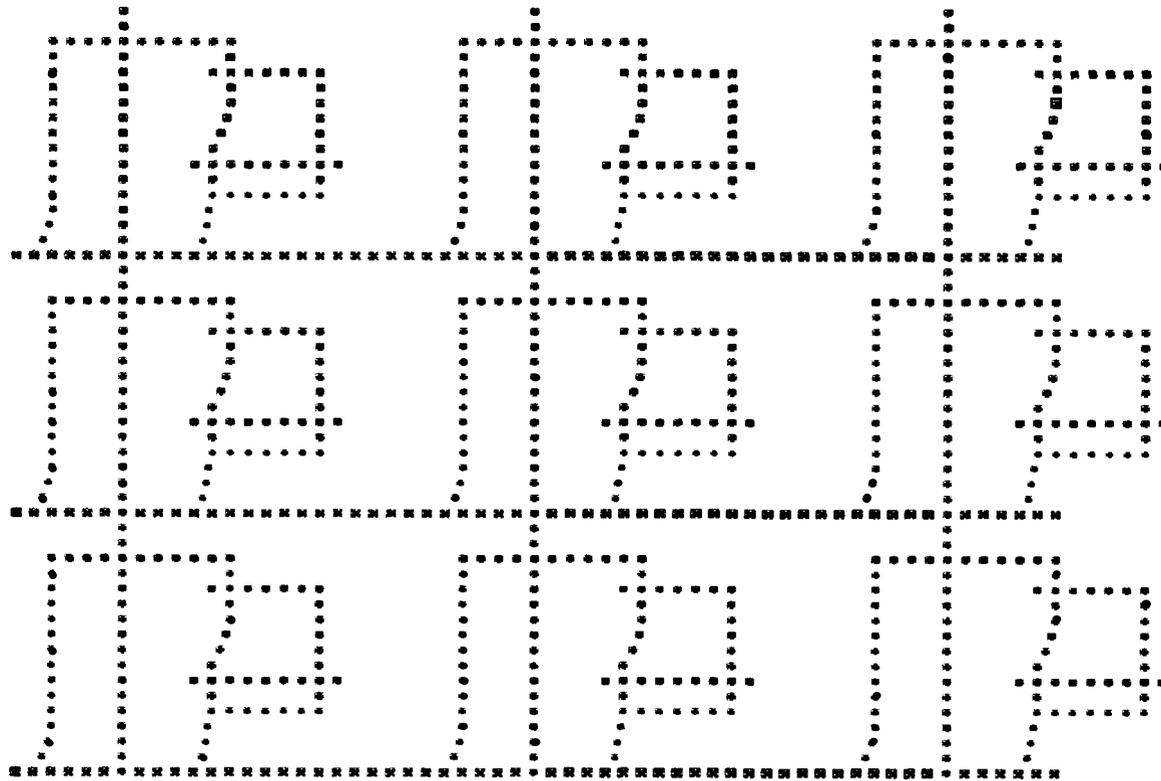
Two key Design Issues:

- Providing the capability of *high impedance* state
- Design of QCA circuit for implementation Crosspoint Switch

# Novel QCA Circuits

## Co-Planar Implementation of Interconnection Networks

### QCA circuit for Co-planar and Compact Implementation of Crossbar Network

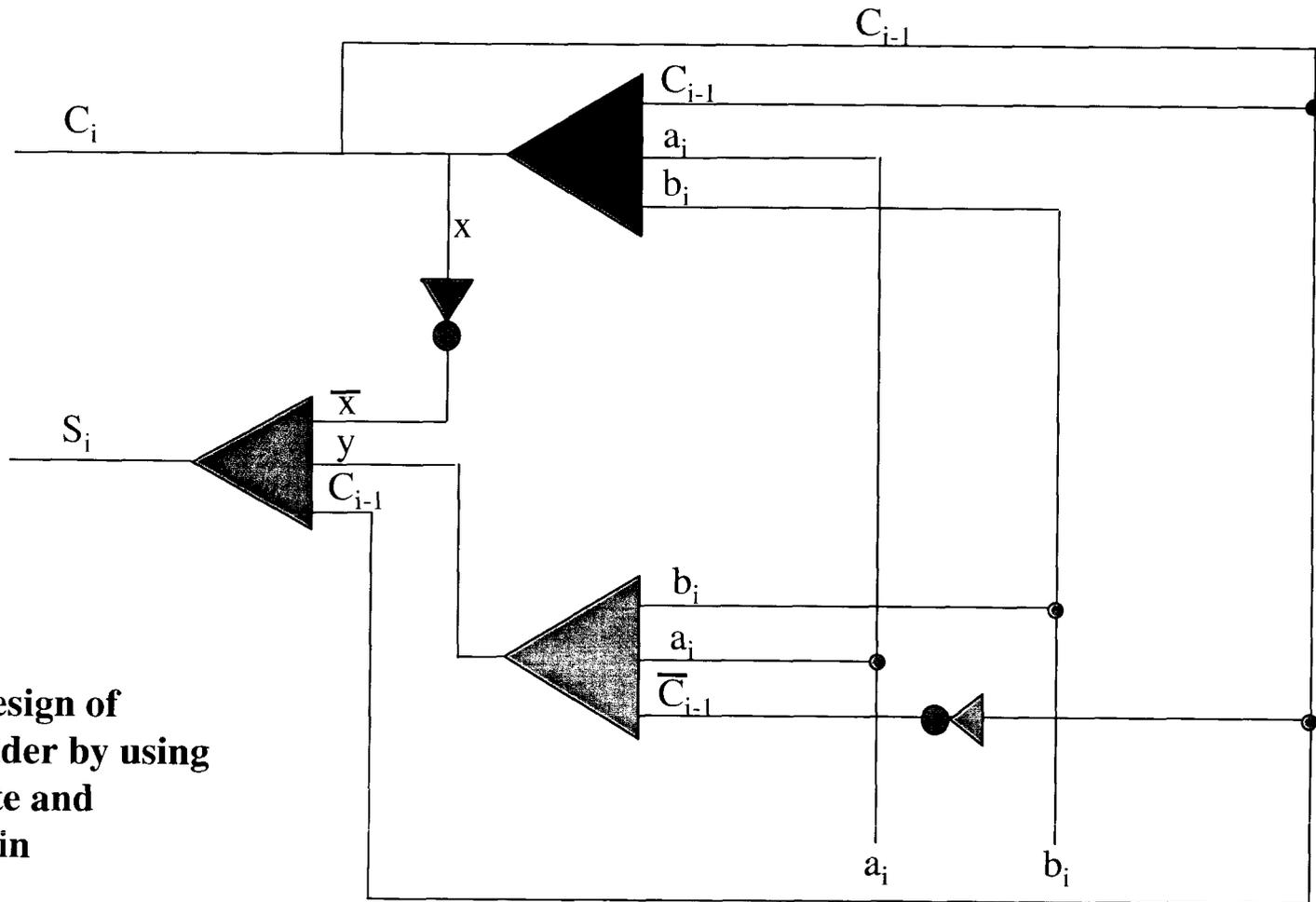


**QCA-based circuit for implementation of a 3X3 Crossbar Network:**  
It provides the high-impedance capability and uses a new scheme for implementation of cross-point switches

# Novel QCA Circuits

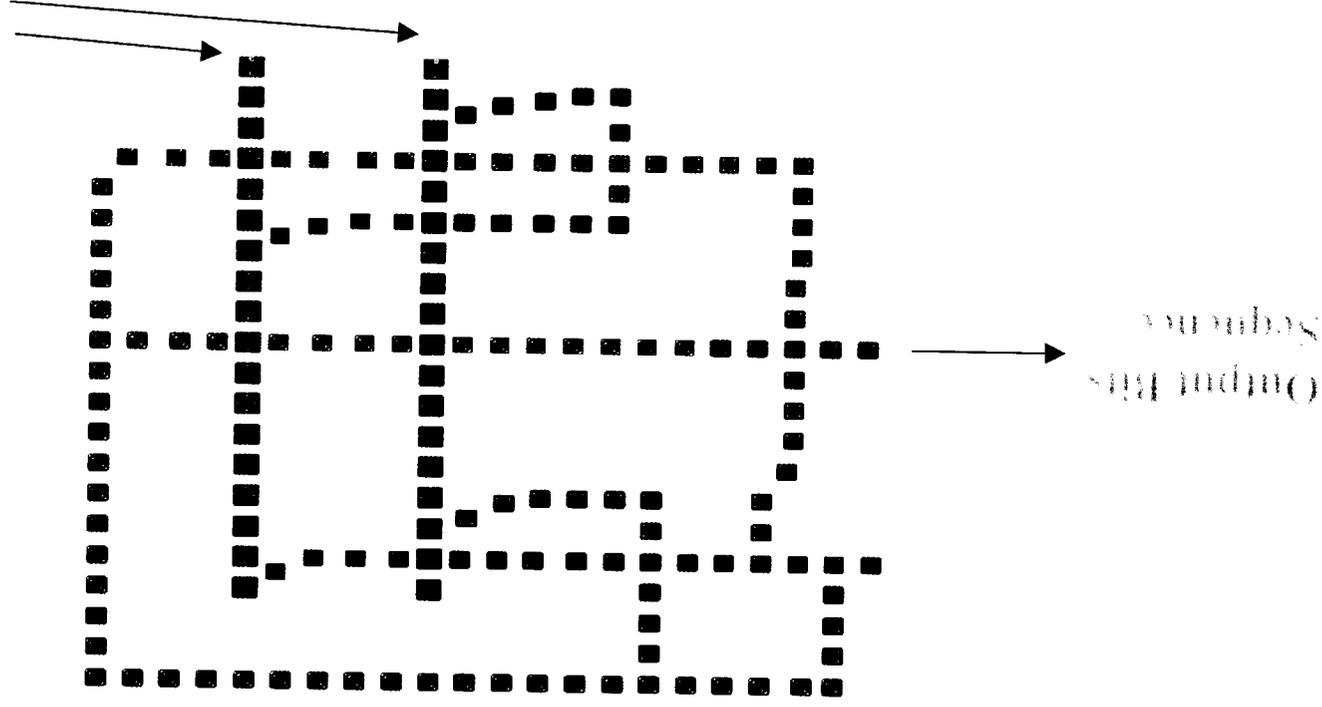
## A Bit-Serial Adder

QCA Circuits for Implementation of a Bit-Serial Adder as the first step toward the design of a bit-serial processor



Schematic Design of Bit-Serial Adder by using Majority Gate and Inverter Chain

# Novel QCA Circuits A Bit-Serial Adder QCA Circuits for Implementation of a Bit-Serial Adder



- The circuit for implementation of Bit-Serial adder incorporates, for the first time, a feedback loop by using QCA-based hardware
- This Bit-Serial Adder represents the first step toward the design of a fully QCA-based processor

# **A Hybrid VLSI/QCA Systolic Architecture for FFT**

- **FFT has previously been considered impractical for highly parallel systolic computation due to its global Communication requirement**
  - **Canonical reformulation of FFT for systolic computation**
  - **A hybrid VLSI/QCA architecture for systolic computation**
    - **The VLSI modules contain a set of simple bit-serial processing elements capable of performing multiply and add operation.**
    - **The QCA modules implement the required complex data permutations.**

# A Canonical Reformulation for Systolic Computation of FFT

$$F_{2^n} = A_n A_{n-1} \cdots A_{i+1} A_i \cdots A_2 A_1 P_{2^n} = \underline{F}_{2^n} P_{2^n}$$

$$A_i = I_{2^{n-i}} \otimes B_{2^i}$$

$$B_{2^i} = \frac{1}{\sqrt{2}} \begin{pmatrix} I_{2^{i-1}} \Omega_{2^{i-1}} \\ I_{2^{i-1}} - \Omega_{2^{i-1}} \end{pmatrix} \quad \Omega_{2^{i-1}} = \text{Diag}\{\omega_{2^i}^j\}$$

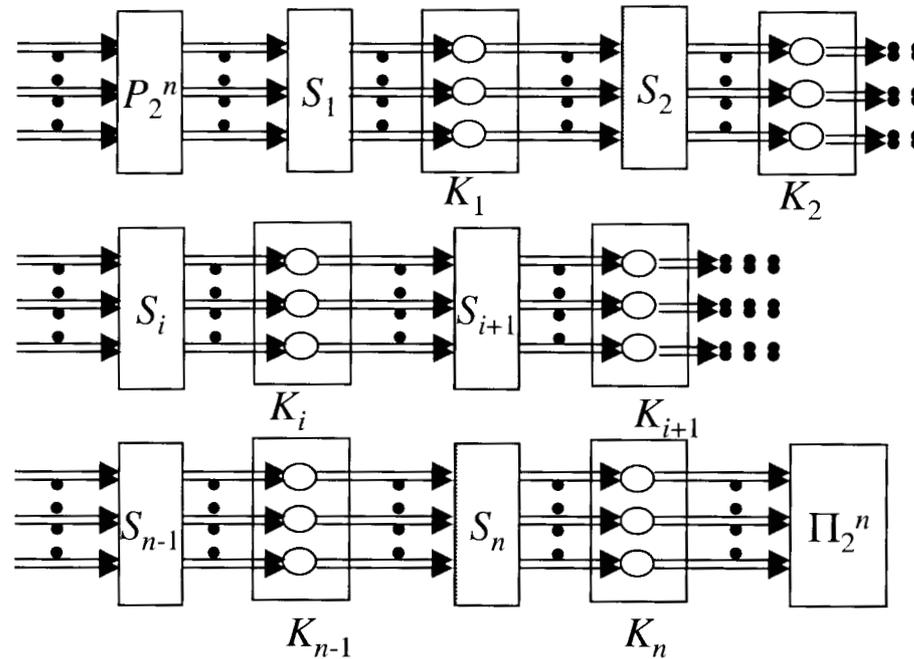
$$S_i = (I_{2^{n-i}} \otimes \Pi_{2^i}) (I_{2^{n-i+1}} \otimes \Pi_{2^{i-1}}^t) \quad K_i = I_{2^{n-i}} \otimes R_{2^i}$$

$$F_{2^n} = \Pi_{2^n} S_n K_n S_{n-1} K_{n-1} \cdots S_{i+1} K_{i+1} S_i K_i \cdots S_2 K_2 S_1 K_1 P_{2^n}$$

# Novel Applications

## Highly Parallel and Systolic Computation of FFT

### A Hybrid QCA/VLSI Architecture for Systolic Computation of FFT

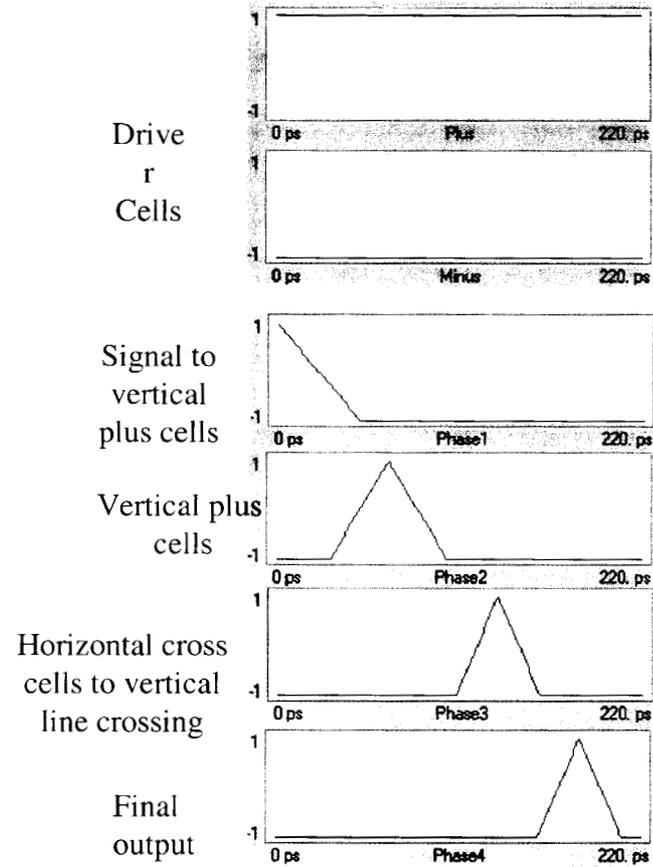
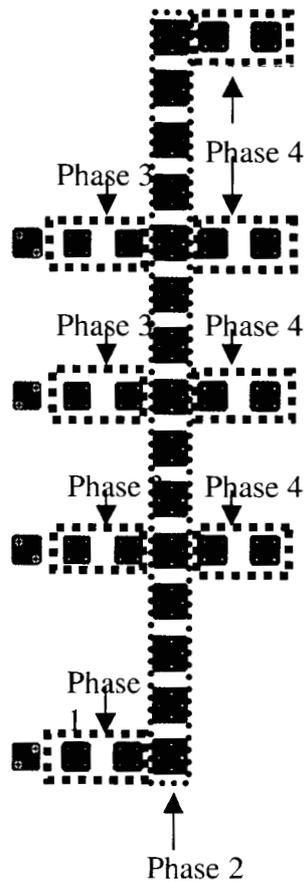


### A Hybrid QCA/VLSI Architecture for Systolic Computation of FFT

- The modules  $S_i$  and other permutation functions are implemented by using QCA circuits.
- The modules  $K_i$  are implemented by using VLSI and contain a set of simple bit-serial processors. They can be replaced by fully QCA-based Bit-Serial Processors.

# Implementation of Permutation Matrix $Q_4$

## Downshift Permutation



$$Q_4 = \begin{pmatrix} 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \\ 1 & 0 & 0 & 0 \end{pmatrix}$$

Clocking Mechanism for Implementation of Permutation Matrix  $Q_4$



# Novel Applications

## Highly Parallel and Systolic Computation of Wavelet Transforms

### *Daubechies 4<sup>th</sup> order $D_n^{(4)}$ Wavelet Transform*

A new factorization of  $D_n^{(4)}$  in a canonical form, which is highly efficient for Systolic computation, is derived as

$$D_n^{(4)} = (I_{n/2} \otimes C_1) Q_n (I_{n/2} \otimes C_0)$$

⊗ Indicates Kronecker (tensor) product

$I_{n/2}$  is identity matrix of dimension  $n/2$

$Q_n$  is the Down Shift Permutation Matrix of dimension  $n$

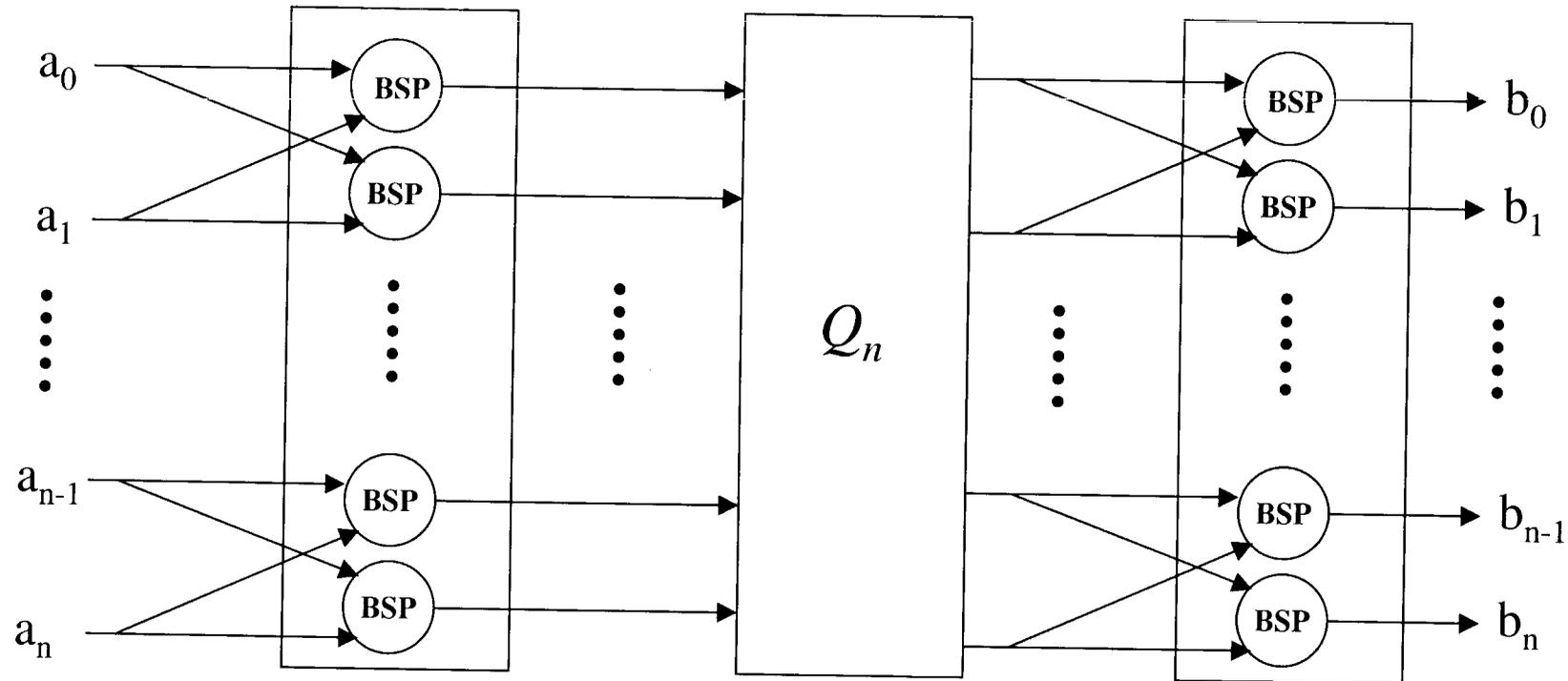
$$C_0 = 2 \begin{bmatrix} -c_2 & c_3 \\ c_3 & -c_2 \end{bmatrix} \quad C_1 = 1/2 \begin{bmatrix} -c_0/c_3 & 1 \\ 1 & c_1/c_2 \end{bmatrix}$$

The matrices  $(I_{n/2} \otimes C_1)$  and  $(I_{n/2} \otimes C_0)$  are block-diagonal matrices with  $2 \times 2$  submatrices on their diagonal.

This new factorization of  $D_n^{(4)}$  Wavelet kernel is highly efficient for a Systolic Computation.

# Novel Applications

## Highly Parallel and Systolic Computation of Wavelet Transform



**A Hybrid QCA/VLSI Architecture for Systolic Computation of Wavelet Transform**

- The permutation functions represented by module  $Q_n$  is implemented by using QCA circuit
- The modules BSP are simple VLSI bit-serial processor capable of performing primitive multiply-and-add operation.

## **Toward fully QCA-based Systolic Architectures for signal/image processing applications**

- The QCA enables efficient and co-planar implementation of various permutation functions arising in signal/image processing applications and thus allowing efficient systolic computation of these applications with hybrid VLSI/QCA architectures .**
- The only VLSI-based component needed for systolic computation of these applications is a simple bit-serial processor capable of performing primitive multiply-and-add operations.**
- The design and implementation of a QCA-based bit-serial processor will then enable systolic computation on signal/image processing applications on fully QCA-based architectures.**
- The developed bit-serial adder represents the first step toward development of a bit-serial processor.**