# Future Capabilities for the Deep Space Network

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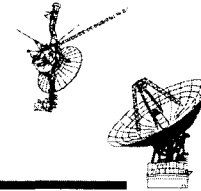
NEW DOWNLINK CHANNEL

- As part of the Network Simplification Project, the Receiver, Ranging, and Telemetry processing were integrated into a single subsystem
  - A Downlink Channel provides all downlink data types (Doppler, Range, and Telemetry)
- Ranging was re-implemented as a single VME DSP processor board in the receiver
  - Instead of a chassis of custom hardware, ranging is now software running on a commercial board
- The telemetry function was implemented in a VME chassis
  - Standard (7, ½) Convolutional decoding, frame synchronization, de-randomization, and output formatting were reduced to a set of just three VME boards, leaving the majority of the chassis open for new capability
  - Two sets of interfaces for symbol data were provided, one for external decoders (such as the current Block III MCDs, which decode (15, 1/6) Convolutional codes), and the other for internal decoders
    - Internal interface is an industry standard FPDP interface, with both the symbols and the symbol's time tag
- The new Downlink Channels easily support the addition of new functions, three of which are discussed in the following slides
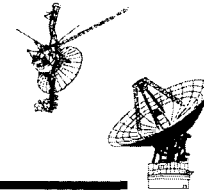
TURBO CODES

- **What are they?**
  - Turbo codes are a new class of error correcting codes that have been approved by the CCSDS
  - They are block codes that are generated by two constraint length 4 convolutional codes
    - One of the convolutional codes operates on a permutated set of source bits
  - There are four frame sizes currently defined: 1784, 3568, 7136, and 8920 bits
  - There are four coding rates defined: 1/2, 1/3, 1/4, and 1/6
- **Why use them?**
  - Performance gain
    - Rate 1/6 turbo code is 0.8 dB better than (15, 1/6) convolutional code concatenated with Reed-Solomon code
    - Rate 1/3 turbo code is 0.4 dB better
  - Decoder complexity
    - Decoding algorithm for (15, 1/6) code is approximately 10 times more complex
    - Turbo decoding can be implemented in software running on commercial DSPs
    - (15, 1/6) decoder required custom ASIC implementation
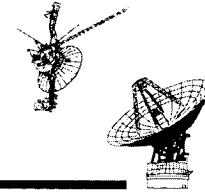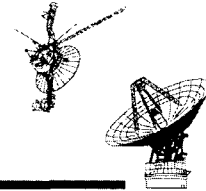
# TURBO CODE BIT ERROR RATE

8920 Bit Frame
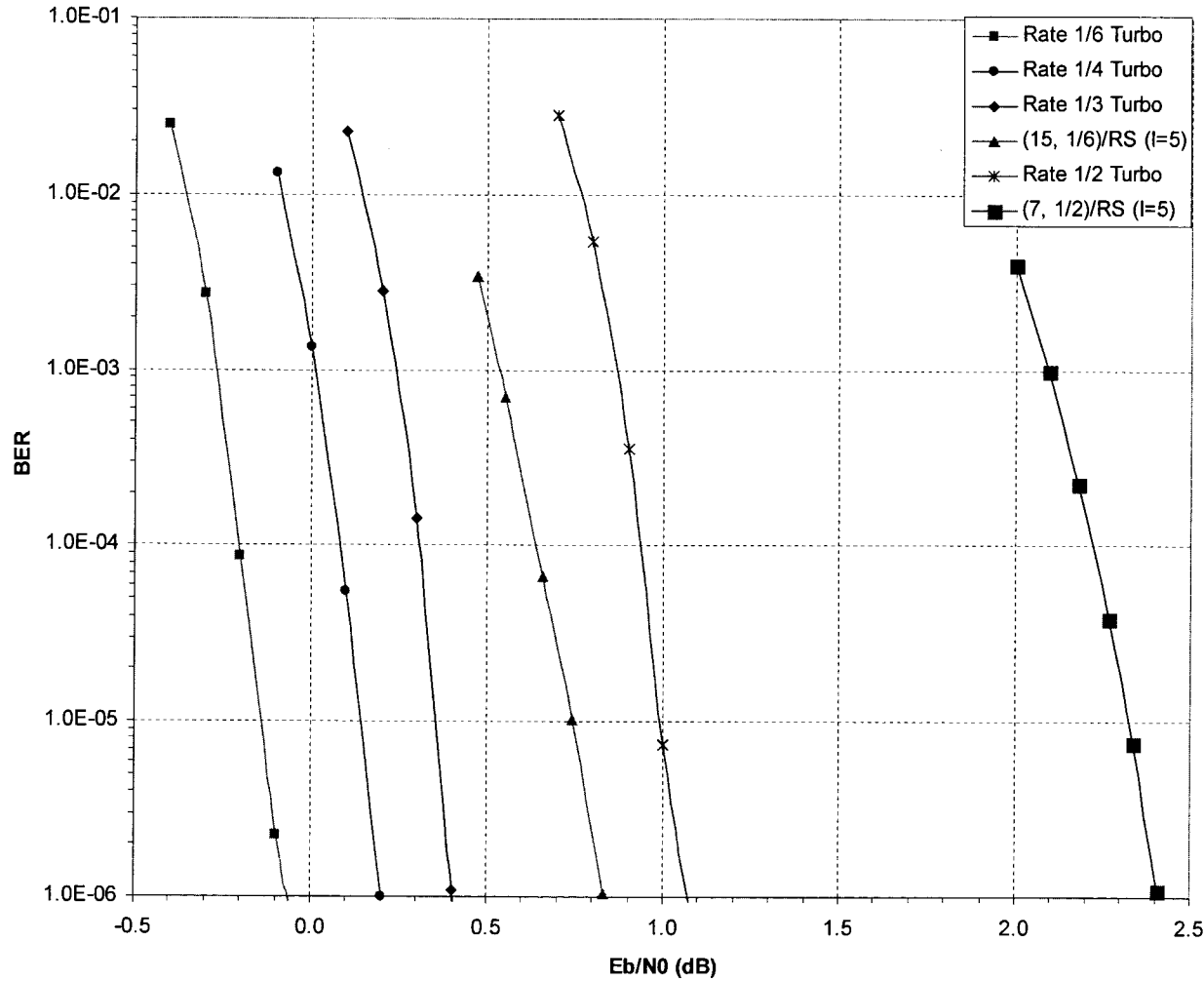
TURBO DECODER IMPLEMENTATION

- The Turbo Decoder is implemented as software running on Texas Instruments Digital Signal Processors (DSPs)
  - Pentek Octal DSP boards are installed in the TLP
  - Additional decoder speed is obtained by adding a second Octal board
- Quantized 8-bit symbols, along with a 24-bit time tag, are sent to the Octal board via an industry standard FPDP (Front Panel Data Port) interface
  - Allows for microsecond time tagging of decoded data
- Control software is integrated into the standard TLP software
  - Decoded data sent across the VME backplane to the output data formatting card

TURBO DECODER STATUS
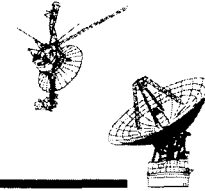
- First delivery of Turbo Decoder has been accomplished
  - Provides support for Messenger bit rates (104 kbps)
  - Subset of code rates and frame sizes
- Next delivery will be in 2004
  - Will support STEREO data rates (up to 720 kbps)
  - All code rates and frame sizes
- Final delivery will be in 2005
  - Second Octal board will be added
  - Supports MRO data rate of 1.6 Mbps
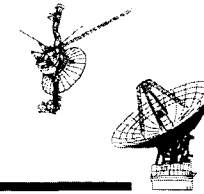
PN RANGING

- **What is PN ranging?**
  - Pseudo Noise (PN) ranging involves creating a ranging signal from a set of short PN sequences, logically combined to provide a longer, unambiguous signal
  - Current ranging (Sequential Ranging) sends tones of different frequencies to set the precision and to resolve the range ambiguity (the highest frequency sets the precision, the lowest sets the ambiguity)
  - PN ranging sets the precision by the chip rate of the modulation and the ambiguity resolution by the length of the combined sequence
- **Why use PN ranging?**
  - Operationally, PN ranging is more robust in the presence of link changes
    - Integration time on the downlink can be changed in real time, without changing the uplink (and waiting an RTLT); Sequential ranging requires changing the uplink
    - Short code periods (one second or less) remove the need to know the RTLT for sequencing
  - PN ranging allows for straight forward regenerative ranging on the spacecraft
   - Can improve the downlink ranging SNR by up to 30 dB
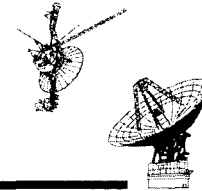
PN RANGING IMPLEMENTATION

- Unlike the previous ranging implementation, the new implementation generates the ranging modulation in software (running on Digital Signal Processors or DSPs
  - No new hardware is needed; only the software needs to be modified
- Implementing PN ranging involves accepting the subsequence definitions and the logical combinations for each one
  - Correlation is done after the received signal is accumulated for the necessary integration time
  - Since the final sequence is a combination of smaller sequences, the accumulation is done on each of the component PN sequences; thus the position in a million chip sequence can be resolved with only 77 correlations
- Control of the ranging type selection and configuration needs to be integrated into the higher level ranging software
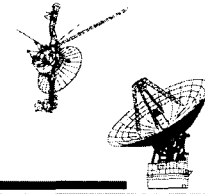
PN RANGING STATUS
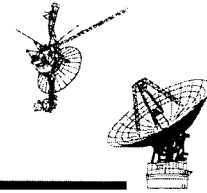
- A set of PN sequences has been selected that provide equivalent or better performance than the sequential tones
- Implementation is planned for 2005
- Ranging regeneration is included on the New Horizons transceiver (launch in 2006)

LOW DENSITY PARITY CHECK CODING

- **What are they?**
  - Low Density Parity Check (LDPC) codes are the second generation of "modern" codes, following turbo codes.
  - They were first defined by Gallager in 1962, but were not practical at that time
    - Rediscovered after the turbo code revolution in 1994
    - Many improvements have been made in the last few years through extensive research
  - LDPC codes are block codes defined implicitly by a sparse parity check matrix:
    - The goal is to design the parity check matrix to optimize performance and complexity
  - Performance is similar to turbo codes
    - Threshold is typically about 0.5 dB from channel capacity
    - An error floor constrains the minimum achievable bit and frame error rates
- **Why use them?**
  - Decoding is iterative, like turbo codes
    - Uses soft input symbols
    - Decoder structure is regular and highly parallel, allowing fast decoders
    - Stops when a codeword is found, or after a maximum number of iterations
  - LDPC codes meet or exceed turbo code SNR performance, with decoders that are 3 (software implementation) to 30 (hardware implementation) times faster
   - This allows decoding of higher data rates than turbo codes
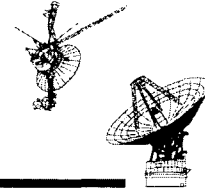
LDPC IMPLEMENTATION

- LDPC codes would only be used in a high data rate scenario
  - 2 Mbps and greater
- High speed implies that the implementation would need to be in hardware, instead of software
  - Frame synchronization must be done at the symbol rate, not the codeword rate
- Integration into the TLP would be very similar to the Turbo Decoder
  - The decoder board would be a VME card
  - The symbols and time tag would be delivered via the FPDP interface
  - Decoded frames would be passed to the formatter processor
 - High level control software would be integrated into the TLP software

LDPC STATUS
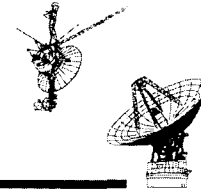
- At this time, LDPC codes are not yet funded for implementation in the DSN; however:
  - They are an extremely active research area
    - Over 100 papers/year are published on LDPC codes
    - Many of these investigate tradeoffs between desirable characteristics
      - Threshold: required E_b/N_0 before code begins to work
      - Error floor: minimum bit and frame error rates at practical SNR values
      - Decoding and encoding complexity
    - Hardware LDPC decoders on FPGAs and ASICs have been built for research purposes, including at JPL
  - Standardization is underway
    - Several LDPC codes have been proposed at CCSDS panel meetings
      - Proof-of-concept deep space experiments are being considered at JPL
    - Draft standard has been written for Digital Video Broadcast (DVB) use
      - Encoded block lengths 16200 and 64800
      - Code rates from 1/2 to 9/10
  - No commercial applications yet, but expect them soon

CONCLUSION

JPL
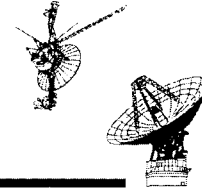
- The new downlink architecture allows for the addition of new capabilities into the DSN
  - Turbo decoding has already been implemented
  - PN ranging is planned to be implemented
  - Low Density Parity Check codes are being considered for implementation