

Technology Infusion for Space-Flight Programs

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Abstract

A tremendous amount of difficulty is encountered in moving technologies from laboratory demonstration (NASA Technology Readiness Level (TRL) 3) to prototype demonstration in a relevant environment (TRL 6). This ability to infuse technologies into space flight programs is limited by a number of factors. Most research funding is for R&D activities that fund tasks from TRL1 to TRL3 (concept to laboratory demonstration). Most flight projects are only interested in technologies that are at TRL6 or higher with no incentive for projects to use any space-unproven technology unless it is essential to completion of the specific mission.

Semiconductors have been following Moore's law for at least four decades, meaning that electronics and packaging technologies that are more than two years old are essentially obsolete. Since it takes about two years to space-qualify a technology if a particular mission regards it critical and there are few or no mechanisms to qualify technologies that are not considered critical to a particular mission, nearly all electronics being used in spacecraft, with the exception of specialty components such as sensors, are many generations obsolete. The same can be said for packaging.

A new approach is required. One approach is to: coordinate all TRL1-3 R&D funding (reduce overlap); require clear and precise statements of work, require progress milestones (i.e. run an experiment, complete literature survey) and to perform independent risk assessments on all TRL1-3 projects using a variety of tools. The tools could be used to rate the technologies in 3 categories: looks promising – continue work; ready for TRL4 and move it into an implementation phase; or, is unlikely to be useable in the next n years – discontinue funding. The residual funding from the R&D <TRL3 phase should be used for TRL4-6 activities, which could be managed the same way: key progress milestones; independent risk assessment; rating for continuation.

Additionally, flight projects need to be given incentive to have a “big-picture” view. Currently, TRL 5 and 6 technologies are taken up by projects and tested to project specific criteria, where with a small amount of incremental funding, technologies could be tested to survive a much broader set of requirements that would be applicable to many different missions. The funding could easily be recovered from the programs because each would not have to redundantly fund complete testing of a particular technology. A program technology tax would be

one way to cover this incremental funding. A number of examples of risk assessments will be covered, emphasizing each of the above.

Introduction

Technology Infusion

In context of this paper, technology infusion means the pathway by which technologies, previously unused by space flight programs, move from their current status onto space flight missions. The technology can be several generations old, the state-of-the-art or anything that is deemed useful to the accomplishment of space missions. In this paper, one approach for addressing technology infusion is proposed. For this approach to make sense, first it should be acknowledged that there is a development “gap” between laboratory bench research and development (R&D) and flight-ready systems. Further, it should be acknowledged that there is proportionally little funding to assist technologies in bridging the “gap.”

TRL at NASA

The National Aeronautics and Space Administration (NASA) has a system for rating where in the development cycle any particular technology resides. This system is called the Technology Readiness Level (TRL). The levels, given in Table I range from inception of a concept to flight-proven.

Table I. Definitions of Technology Readiness Levels for NASA [1]

TRL Level	Description
9	Actual system “flight proven” through successful mission operations
8	Actual system completed and “flight qualified” through test and demonstrated on the ground or in space
7	System prototype demonstrated in a space environment
6	System/subsystem model or prototype demonstration in a relevant environment on the ground or in space
5	Component and/or breadboard validated in a relevant environment
4	Component and/or breadboard validated in a laboratory environment
3	Analytical and experimental critical function and/or characteristic proof-of-concept achieved in a laboratory environment
2	Technology concept and/or application formulated

1	Basic principles observed and reported
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Microelectronics as an example

Microelectronics will be used extensively as an example in this paper because there are well-defined visible metrics for the microelectronics industry. The need for a new strategy for technology infusion will become evident through this example and the proposed new strategy will be viewed in light of this example.

Although references to the microelectronics industry will be used extensively, the approach is applicable to any new technology. The same strategy will work as well for materials development as well as systems or software design.

Background

Microelectronics History

Microelectronics can be viewed in terms of four levels of assemblies. Starting with level-zero is the integrated circuit (IC or chip) itself. Generally, this chip is a semiconductor made of Si, GaAs, InP, SiGe or some variant of intrinsic semiconductors, III-V or II-VI compounds. Level-one, commonly called the package, includes the interconnects that go from the chip itself to either a small circuit board or to a metal lead frame. This package, generally, has standardized dimensions and input/output (I/O) pitch, and is robust enough for transportation to assembly houses anywhere. The package is usually mounted on the next level of assembly (level-two), which is the printed wiring board (PWB) whose function is to connect the packages and any passive components (inductors, resistors, capacitors, transformers and some high-frequency devices) to each other and to the outside world. The level-three assembly is a system level consisting of multiple level-two assemblies. There can be many intermediate sub-system level assemblies in an overall system.

Current technology turnover

A primary driver for change in technology infusion strategies is because of the furious rate of change in the level-zero and level-one technologies. Moore's law (every 18 months, the number of transistors on a chip will double), shown in Figure 1, predicted the current situation accurately in 1965 for level-zero technologies [2]. Because of the tremendous strides in level-zero, the level-one technology has been forced to also rapidly advance.

Unlike previous generations, the technology drive is primarily from commercial electronics. For example, in 1998 military and space technology applications were using complimentary metal oxide semiconductor (CMOS) chips at 2 GHz. Commercial state-of-the-art technologies were running at 300MHz. Currently, typical space-qualified processors run below 500MHz and commercial processors run in excess of 5GHz.

Some concrete examples of Moore's law and packaging advances follow. Features at 0.13 μ m were introduced at the end of 2001 in commercial devices and 90nm were introduced in 2003 [3]. The highest operating frequency of commercial Si microprocessors was 1.68GHz in 2001 and is 5.2GHz in 2003 [3]. The number of gates on a processor has gone from less than 50 million in 1998 to about 200 million in 2002[3].

Unlike previous generations, the packaging technology has also had to advance with similar progress in the state-of-the-art in the last several years. Commonly available wirebond pitch has gone from 200 μ m center to center, on the same row, occasionally using two tiers in 1998 to 70 μ m center to center using up to four tiers in 2002[4].

Another innovation that has swept the packaging industry in the last two years is the significant implementation of flip-chip technologies. Flip –chip technology is one where the traditional Au wirebonds are replaced by small spheres of solder and the chip is mounted to the package face-down. Although used for internal applications from the mid-sixties by IBM and selectively in the automotive industry since 1988, widespread commercial availability did not occur until 2002. Most Si designs do not yet take advantage of the significant improvements made available by flip-chip packaging strategies.

Many other advances have been made in overmold polymers, die attachment techniques and other packaging technologies that had not changed significantly until the last five or so years. These advances have been driven primarily to reduce cost while adapting to the higher and higher chip complexities and speeds.

The infusion process

A particular technology should have several baseline requirements fulfilled to be seriously considered for infusion into flight programs. Among these are:

- A clearly identified advantage the technology offers
- Significant reliability data
- Some production history (commercial or military)
- More than one qualified vendor
- Any additional testing for the particular space environment
- Multiple targeted NASA programs that will clearly benefit