Electronic Packaging for Extended Mars Surface Missions

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Abstract

Extended Mars missions will require vehicles to survive a large number of extended temperature cycles. To address this issue for electronics, previous strategies have been to locate critical electronics in a "warm electronics box" where thermal management is more easily maintained. However, that strategy limits number and location of electronics. An alternative strategy allows electronics to be remotely located on actuator and wheel arms with no heating which has the advantage of distributed control. This strategy requires the electronics to survive the Martian extremes of –120 to +20°C for the duration of the mission. In addition, wheel motor controllers may be mounted directly on the motor casing extending the temperature range on the warm side to +85°C (including some margin). Since missions may last 18 months or more and with day-night cycles on Mars at about 26 hours this will mean survival of approximately 500 cycles. Typical testing is performed to 3x the number of cycles giving the electronics a testing requirement of –120 to +85°C for 1,500 cycles.

Technically, several problems arise in both the large (205°C) temperature swing as well as the large number of cycles. A substantial survey and technical workshop have been conducted leading to an initial choice of a chip-on-board strategy. Materials properties at -120°C are not well known. Additionally, the true materials properties are a function of their process history.

A parallel approach of materials characterization and physics of failure with engineering experimentation is being used to address these issues. An interferometry strain/displacement gauge (ISDG) technique, for in-situ, temperature dependent material stress/strain measurement as a function of temperature as well as a standard dynamic mechanical analyzer (DMA)is being used for materials characterization. A full factorial experiment, designed to highlight expected failure modes from the physics of failure analysis is being conducted. The experiment is designed to evaluate different substrate materials, different die attach materials and different encapsulants or coatings. Combinations of these materials are being tested on a test vehicle with die representing a range of die sizes in an effort to determine lifetime and to verify failure modes. Initial results will be presented.

Introduction

The task objective is to develop and demonstrate low cost, commercially available, and space qualifiable electronic packaging technology that will enable electronics assemblies to survive 500 cycles in the Mars ambient environment (-120 to +20°C). Heating of mechanical components, such as motors, may increase this range to approximately +85°C for the drive electronics integrated within the motor housing. For qualification, a design margin of 3 is required resulting in a survival of 1500 cycles from -120 to +85°C as the requirement.

The commercial states of the art in this area are the Mil-Spec electronics, rated from –55 to +125°C operation, typically for a few hundred temperature cycles. Generally, the electronics qualified to survive a large number of wide ranged temperature cycles (thousands) are required for under-hood automotive applications, whose temperature range is on the high side, similar to that outlined in the Mil-STD-810 [1] .

We have reviewed available data from industry and academia as well as from NASA/JPL's MUSES-CN, MER and NEPP programs as well as NASA Glenn, etc. and concluded again that the long term low-temperature reliability and thermal cycling data in the temperature range of interest for Mars on critical electronics parts are scarce. Thus, eliminating thermal control for electronics on the Rover becomes a matter of establishing the required reliability and operability for the electronics. Two aspects need to be addressed:

- Reliability and survivability of electronic packaging under the stress conditions induced by thermal cycling.
- Reliable operation and required functionality of electronics parts and devices in the required, wide temperature range for extended periods of time.

There is no proven assembly and packaging technology that is commercially available and can optimally absorb the required number of cycles (1500) within the required temperature range (-120 °C to +85 °C). After extensive review and collaboration with Johns Hopkins University Applied Physics Laboratory (APL), Auburn University, University of Maryland (CALCE), industry consultants and many JPL projects and sections, a Chip-on-Board (COB) strategy was selected as the most likely to survive the above environmental conditions.

The objectives of this experiment were to: 1. Select a high density interconnect and packaging technology that will achieve the volume and function requirements while surviving –120°C to +85°C for at least 1,500 cycles (3 x 500), and 2. Validate the technology selection by identifying appropriate materials set for COB technology including substrates, wires, die attach materials and coating materials, determining failure modes, and predicting lifetime. Ultimately, this will result in a design guideline (understand capabilities) and a processes guideline (understand capabilities).

Background

The test vehicles was designed to examine the survivability and lifetime of a chip-on-board approach for a Mars mission motor driver application.

The overall strategy is to: 1 Perform screening experiments. 2. Perform a full factorial experiment of best candidate materials (Test Vehicle 1). 3. Design a "passives" test vehicle, which may address a number of related issues including: various capacitors, resistors, inductors, packaged and unpackaged FETs, multilayer issues including blind and buried vias. 4. Perform a revised experiment based on information gathered from TV-1 and alternative candidate materials. 5. Make a prototype of the best estimate of the final hardware design and perform initial screening tests that will lead to flight qualification of the circuit.

This paper covers the second step, the full factorial TV-1 experiment. Future test papers will cover items 3-5.

Scope

The goal of this test vehicle is to: evaluate COB materials combinations; identify failure modes; collect lifetime data. Expected failure modes are: Die cracking die separation, wirebond failures; changes in resistance, die strain, metallurgy changes.

The overall approach to the initial test vehicle is to isolate the wirebond chip-on-board lifetime technology issues from any others in the assembly. Items such as multilayer boards, blind or buried vias, passive components or surface mounted components will be tested in future vehicles.

Experimental Design

The experimental design for TV-1 was selected to find the best combination of materials to survive the requirements outlined in Section 1 and to cycle them to failure to determine the ultimate lifetime of the assembly. The baseline assumption in this particular design is that the chip-on-board sub-assembly will be the weakest link in the entire electronic assembly. This assumption will be tested with future test vehicles.

Materials properties in the low temperature range are not well understood. The materials will be characterized by APL down to low temperatures (<-120C). Ultimately, the COB sub-assembly will be modeled for future predictions and variations in materials and in their properties by CALCE at the University of Maryland.

Materials Selection

Figure 1 shows the chip-on-board structure that is the subject of TV-1. The materials related to this technology are:

1. the integrated circuit,
2. the wirebonds,
3. the die attach material,

4. the substrate
5. the overcoating.

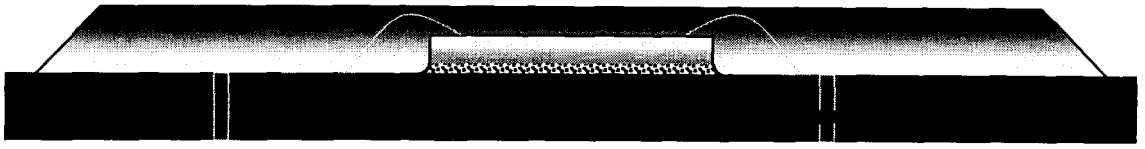

Figure 1. Chip-on-Board configuration being tested in TV-1.

These are all of the materials involved in this wirebond COB technology with the exception of the materials internal to the integrated circuit, which are intimately related to the performance of the integrated circuit and being tested under a different task. After numerous discussions with various representatives including, APL, Auburn, JPL, University of Maryland and a number of industry representatives, an initial list of candidate materials was determined. This list is shown in Table I. Resource constraints would not allow complete testing of all above materials, so a downselect was made through a series of meeting with the above listed parties. The downselect thought process is described below.

Table I. Initial Candidate Materials List.

	Materials
Die	Si -CMOS, Si-SOI
Substrate	Polyimide , LTCC (A-6 or 841), Al_2O_3, DBA, Cyanate Ester
Encapsulant	Epoxy (Hysol 4450, 4402, 4401), Silicone based, Parylene, Uralane 5750
Attach	Epoxy (84-1, 84-3), Solder (Sn63, In, InSn, AuSn), UV Curable
Wire	Au, Au-Pd, Al, TAB

Materials for items one and two are somewhat standardized in the industry and have limited variation. For the integrated circuit, the assumption is that the material will be some form of Si. There may be some subtle differences in bulk properties of the Si between various process categories such as CMOS and SOI, and even more subtle difference between vendors for any particular process. In the current experiment, it was assumed that these differences are somewhat smaller than the differences in the other materials. Although this is thought to be the case, both CMOS and SOI die materials will be characterized by APL. Again, this assumption can be checked by future vehicles if a problem becomes apparent. As a result, all of the die for TV-1 will be Si CMOS.

A similar circumstance occurs for the bonding wire. An industry standard for military and space product is to use 1.0 mil (25micron) Au. Although some commercial applications are using 0.7 mil (primarily to save money), the smaller diameter has reduced strength and as a result is not being considered. Some larger wire diameters have also been used in high power applications. However, when using ball bonding, these wires form a ball that is too large to fit on most standard IC pads. Since ball bonding has the most process history and is the most used technique, TV-1 will use ball bonding with 1.0 mil Au wire. Some variations in the Au wire are available in terms of elongation due to processing or additives. At this time, TV-1 will use JPL standard Au wire with is 5-8% elongation.

For die attach materials, the team's initial decision was to select a candidate material from each of the major material categories, therefore, an epoxy, a silicone and a solder were selected. The epoxy initially selected was Ablebond 84-1, which has the most military and space flight history, however, it is known to be brittle at cold temperatures. The vendor was contacted and asked for recommendations for a more flexible version of the material. The vendor recommended two candidate materials, Ablebond 976-1 and Ablebond 967-1. Ablebond 967-1 was selected due to its lower glass transition temperature of 75°C. Silicones were considered because of their very low Tg and high compliance. The Dow-Corning material HIPEC Q1-4939 was recommended by APL based on their experience.

A number of solders were considered. Three primary criteria drove the solder selection decision; 1. no phase transition in the temperature range being tested, 2. minimal formation of intermetallic structures incorporating Au (present on both the die and the substrate), and 3. high compliance. With these three criteria, In was the best candidate material. After some research into the area, no indication of harmful intermetallic InAu structures has been found.

Some concern was expressed regarding the relatively low melting point of In (158°C). This could be an influence in two areas. First, additional assembly processing could take the In die attach near its melting point if not carefully considered. Second, some diffusion of the Au interfaces could occur during operation if the die were operating at an elevated temperature. The first concern can easily be removed by attention to the assembly process, which has been done.

The second concern is remedied by the physics of the materials selected. The In-Au phase diagram in Figure 2 shows that a slight amount of Au diffused into pure In increases the melting point dramatically. The mixture rate in this area is 63.1°C/% at 1%, 94.7°C/% at 2%, 121°C/% at 3%, 139.5°C/% at 4%, and 157.9°C/% at 5%. The system is therefore self limiting as long as the processing or use temperature does not get too close to the peritechtic point at about 54

weight% In. Too close is defined as >70% of the mp (813 K at the peritectic) in degrees K which in this case is 569 K (296°C).

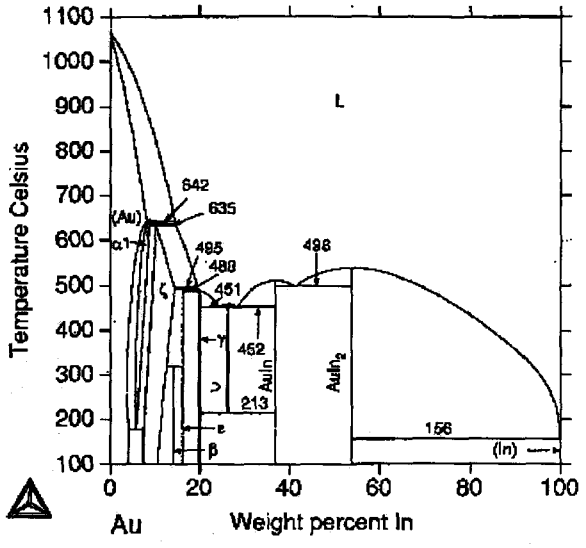

Figure 2. In-Au Phase Diagram [2]

Substrates were selected in the following manner. Polyimide was selected as it has the best properties for an organic and is the most common space flight circuit board material. Alumina was selected because of its military and space heritage for use in hybrid circuits as well as superior expansion and toughness. Low temperature cofired ceramic (LTCC) was selected as having good expansion properties as well as its ease of incorporating multilayer design, which is likely to be required based on the constraints of the application.

Overcoat materials are being considered for protection of the exposed wirebonds as well as possibly enhancing the mechanical strength. This second point is controversial and some studies indicate that some overcoats may actually deteriorate the mechanical strength of the chip-wire-board system. As a result, some boards will be tested without any overcoating at all.

Again, representative materials from three different categories were chosen. An epoxy (FP-4402) a silicone (HIPEC Q1-4939) and parylene-C. The first two materials are considered "glob-top" materials encapsulating the entire COB sub-assembly and the third is a thin coating. The epoxy has an extensive military and space flight heritage, the silicone was selected for its compliance properties. The parylene also has space flight heritage and is considered a very low stress material.

Experimental Description

Design of Experiments

In addition to the screening experiments, a full factorial experiment on the materials will be performed using the matrix shown in figure 3. Along with the full factorial experiment, ten additional parts will be tested containing no overcoating as a baseline.

			No. of Substrates
•Substrate 1			
	–Die attach 1		
		Encapsulant 1	10
		Encapsulant 2	10
		Encapsulant 3	10
	–Die attach 2		
		Encapsulant 1	10
		Encapsulant 2	10
		Encapsulant 3	10
	–Die Attach 3		
		Encapsulant 1	10
		Encapsulant 2	10
		Encapsulant 3	10
•Substrate 2			
	–Die attach 1		
		Encapsulant 1	10
		Encapsulant 2	10
		Encapsulant 3	10
	–Die attach 2		
		Encapsulant 1	10
		Encapsulant 2	10
		Encapsulant 3	10
	–Die attach 3		
		Encapsulant 1	10
		Encapsulant 2	10
		Encapsulant 3	10
•Substrate 3			
	–Die attach 1		
		Encapsulant 1	10
		Encapsulant 2	10
		Encapsulant 3	10
	–Die attach 2		
		Encapsulant 1	10
		Encapsulant 2	10
		Encapsulant 3	10
	–Die attach 3		
		Encapsulant 1	10
		Encapsulant 2	10
		Encapsulant 3	10
			270

Constants for first round
1. Au wire
2. Wirebond dimensions

Baseline of 10 parts with no encapsulant to be run separately
Substrates double sided with mechanical die only on back side
Backside die up to 22mm

Die Sizes
2.5mm
5mm,
10mm

Figure 3. Full Factorial Experimental Design.

A full factorial experiment was selected to provide the best data possible for the generation of stress models (see section 4). Alternatives, such as d-optimal designs were reviewed, however, because they do not account easily for second order interactions, the team agreed that a full factorial would be most suitable.

With selected substrates being examined and destructively tested at 500, 1000 and 1500 cycles, eight parts would remain for full lifetime testing giving an initial sample size of ten parts for each material combination. With three substrate types, three die attach and three coating materials the total number of combinations is 27. With 10 parts each, this comes to 270 parts.

Test Vehicle

Test vehicle 1 is shown (front and back) in figure 4. The test vehicle accommodates three die (2.2mm, 5mm, 10mm) on the front electrically

connected, and a single mechanical die (up to 20mm) on the back. The test vehicle also incorporates two daisy chains to test via continuity independently. .

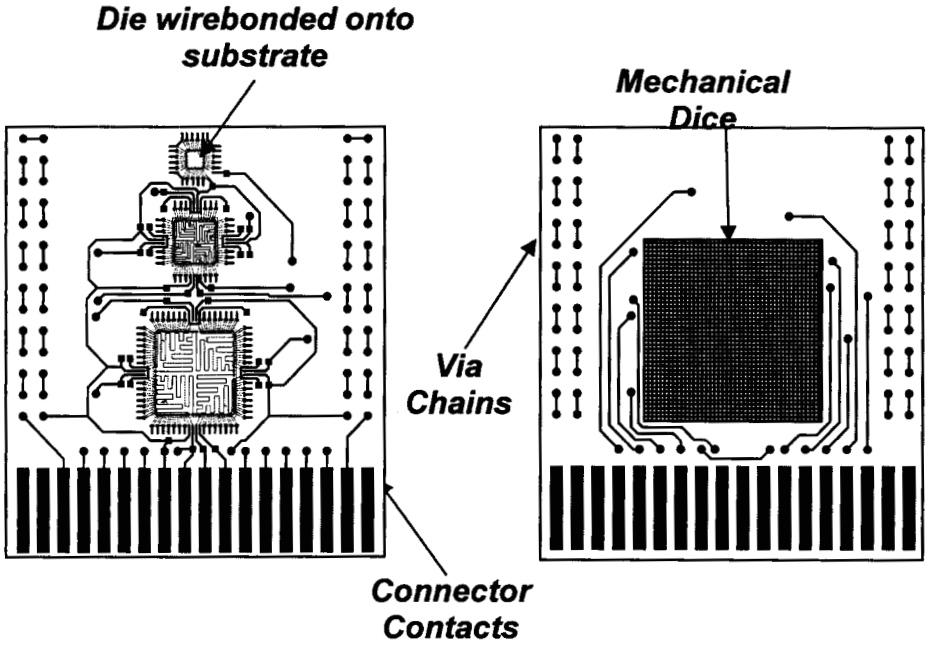

Figure 4. Test Vehicle 1

The assembly of the test vehicles followed the general flow shown in figure 5 with the appropriate time and temperature for the different die attach and encapsulant materials.

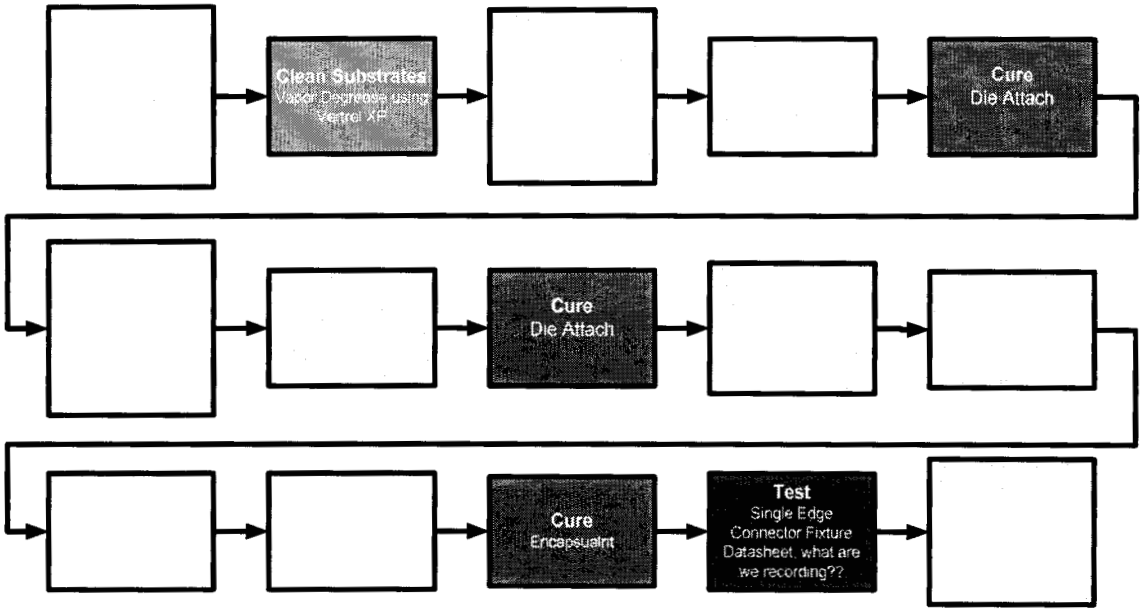

Figure 5. General Assembly Flow

Curing of encapsulants and adhesives is designed to provide the combination of highest compliance and lowest glass transition temperature.

Test Die

A test diec is shown in figure 6. The 5 and 10 mm die was supplied by APL. They include both resistance gauges as well as peripheral daisy chains segmented into 4 quadrants. The die contain 8 meander resistance gauges rotated for each quadrant. To reduce the total number of test channels required (for 270 substrates), the team decided to only use the 4 exterior resistance gages.

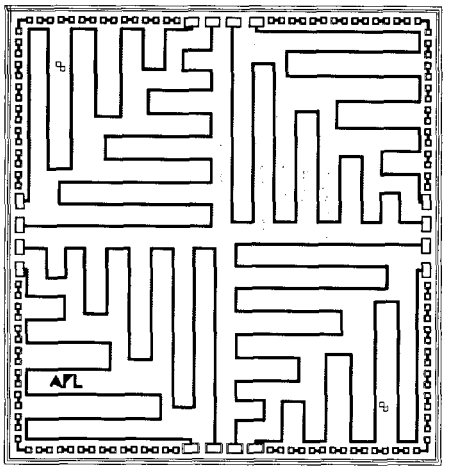

Figure 6. 10mm Die for Test Vehicle 1.

The 2.2 mm test die was supplied by JPL from MOSIS wafers. This test die has a daisy chain only. The die sizes were selected to incorporate the most likely sizes to be encountered in the expected actuator design. The resistances gauges have a common ground and the daisy chains have a common ground. Each resistance gauge and dice daisy chain is measured independently through the connector. Each quadrant daisy chain has an independent probe point.

Test Flow

All of the assemblies will be visually inspected to JESD22-B101 [3] and tested, with the resistance values being recorded, for continuity prior to being placed in the environmental chamber.

All of the assemblies were visually inspected to JESD22-B101 and tested, with resistance values being recorded, for continuity immediately upon removal from the environmental test chamber. Any visual damage or changes were noted on the lot traveler. The common performance requirements and related tests for TV-1 are listed in Table II. These tests are a subset of those required by typical defense and space systems. Additional testing is planned for a later time.

Table II. Thermal Cycling Validation Criteria.

Validation Test	TP Section	Reference	Electrical Test	Acceptance Criteria [a]
Thermal Cycling	3.2.1	IPC-SM-785	Electrical continuity failure	Less than 10% change in resistance over 1500 cycles at 10% Weibull cumulative failures

[a] Failure of a test board in a specific test does not necessarily disqualify a materials set for use in an application for which that test does not apply. Electrical performance requirements for a particular circuit apply only to parts containing that circuit.

The test flow for the standard sequence of environmental testing is shown in figure 7.

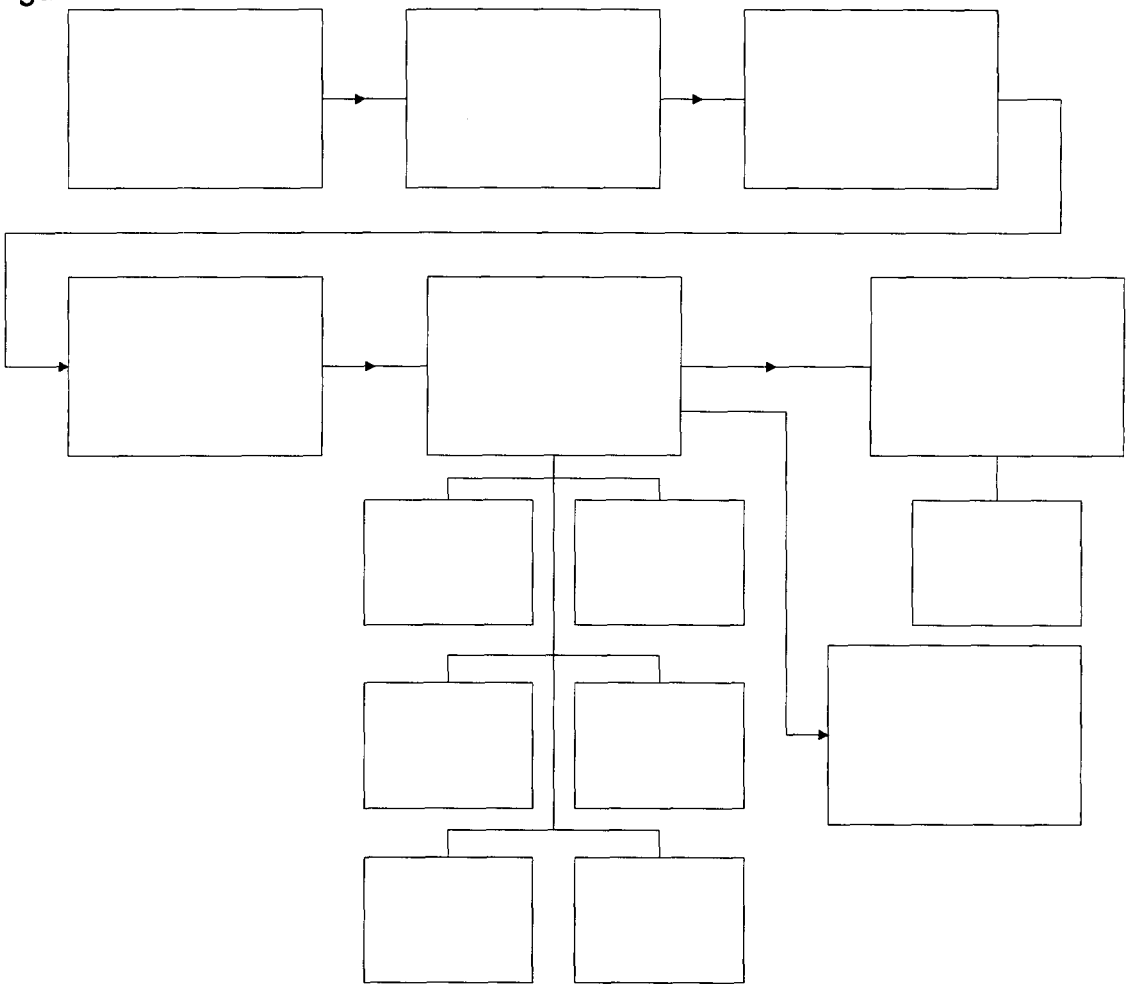

Figure 7. Experimental Standard Environmental Test Flow

Electrical Continuity Testing

Electrical continuity testing will be performed prior to and during all environmental tests. The test setup and equipment are shown in figure 8. Data is recorded through a GPIB interface from both the cold chamber as well as the continuity

test set-up. The monitoring will be a continuous scan during the temperature cycling and other environmental testing using a digital sampling rate of one measurement per second.

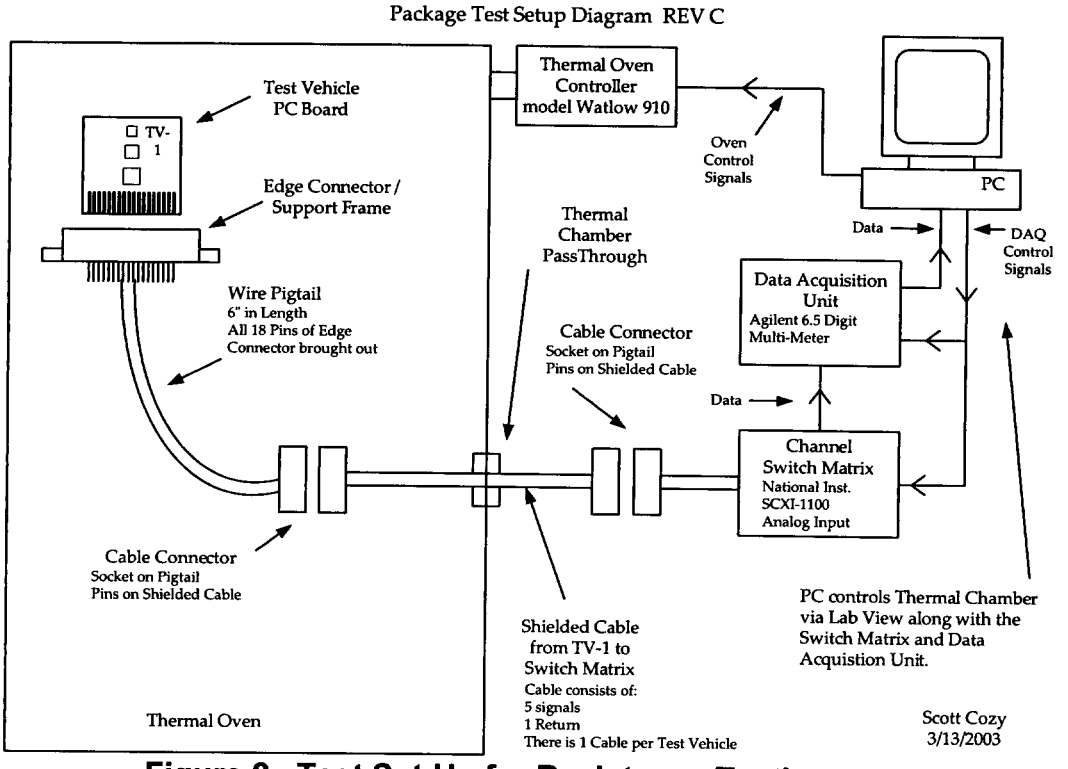

Figure 8. Test Set-Up for Resistance Testing

Thermal Cycle Testing

This test determines a test specimen's resistance to degradation from thermal cycling. Perform this test in accordance with IPC-TM-650 [4] and the following procedure. Continuously monitor the electrical continuity of the solder joints during the test. Place one set of test vehicles in thermal chamber at -120°C to +85°C with a ramp rate of 5°C/min and a dwell of 10 min at each extreme as shown in Figure 9. Cycle until 63% failures achieved.

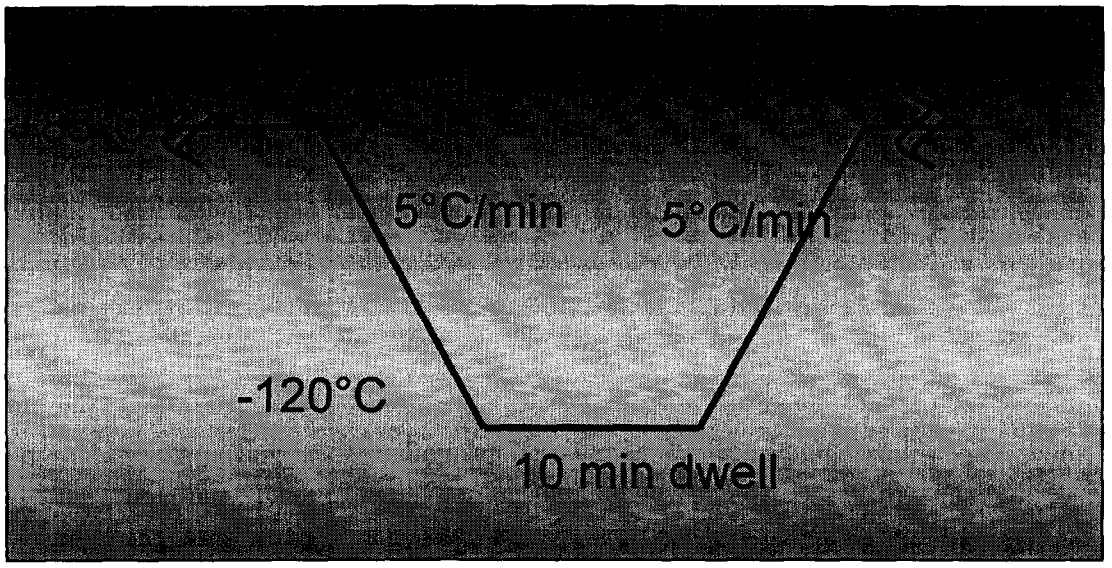

Figure 9. Thermal Cycle Test Environment

Table III. Thermal Cycling Test Methodology

Parameters; TV-1	• -120°C to +85°C • Cycles: Until 63% failures or greater • Decision point at 5000 cycles if 63% failure not yet achieved • 5°C/minute ramp • 10 minutes, dwell after test vehicle reaches temperature
Number and Type of Specimens	10 boards for each material combination
Trials per Specimen	1
Acceptance Criteria	Less than 10% change in resistance and no catastrophic failures up to 1500 cycles

Mars environment is expected to cycle between -120°C and +20°C, however, this circuit is designed to be adjacent to actuators or drive motors which will heat the samples to as high as +70°C while operating. The requirement for the electronics at the actuator is to survive 500 sol with the worst case ambient being -120°C to+70°C. To provide margin for the application, it was agreed with the program office that 1,500 cycles from -120°C to+85°C is an appropriate cycle acceptance range. Record data and compare to acceptance criteria as specified in TP Section 3.1.1. Optical images will be taken prior to testing and at specified intervals. Cross-sections and EDS will be performed on samples removed at 1,000, and 1,500 cycles.

Statistical Approach

Statistical considerations are essential for meaningful conclusions that will hold up under scrutiny. As such, the numbers of components on the test vehicle and

the test sample sizes have been selected to provide statistically meaningful results.

Statistical review of the data generated by the testing is of importance to generate credible models. Statistical distribution of failures will be represented by a Weibull distribution. As the testing is performed and failures occur, Weibull distribution coefficients will be determined for the data collected as discussed in IPC-9701, section 5.2 [5]. The data of most interest are the first failures; the number of cycles required to reach 63.2% failures (called the characteristic life or alpha); the failure free period; and the Weibull shape parameter (beta).

When one failure mode occurs on a component, the whole component is considered failed. In order to generate useful Weibull plots, ideally 50% of the assemblies must fail with a 63.2% component failure rate. This requires many testing cycles (many hundreds to many thousands depending on the type of component).

Project technical representatives discussed sample size at length. The sample size for each materials combination was selected to be 10. To achieve a 90% confidence level at 10% cumulative failures, a minimum sample size of 21 is required. The stakeholders felt that the 10-sample size rather than 32 as specified in IPC-9701 would provide statistically meaningful results. IPC-SM-785, *Guidelines for Accelerated Reliability Testing of Surface Mount Solder Attachments* [6], has equations for calculating the minimum number of failure-free test cycles for a given cumulative failure probability percentage with sample size and design life cycle requirement.

Materials Characterization

The temperature range in which the electronic packaging materials need to survive and function has been extended beyond the vendor specifications and the MIL standards for the Mars mission. Understanding material behavior in the Mars low temperature environment is critical for assuring reliability of the electronics. Physics-of-failure reliability assessment requires appropriate temperature-dependent material property inputs. Obtaining temperature-dependent material stress-strain relationships is essential for stress analysis and failure analysis model development and implementation. The Applied Physics Laboratory is performing materials characterization tasks to measure the properties of materials at the extreme low temperature. Specifically, dynamic modulus and stress-strain measurements of the candidate materials will be measured to -120°C or below. Modulus and glass transition temperature (Tg) will be measured using a dynamic mechanical analyzer (DMA). The Interferometric Strain/Displacement Gage (ISDG) technique will be used to perform non-contact strain measurement as a function of temperature. The ISDG measurement will be taken using selected materials from the table that exhibit strong temperature

dependency as well as Au wire. Table VI lists the candidate materials that will be measured using the two techniques.

Table IV. Candidate Materials for Characterization.

Die Encapsulant	Die Adhesive	Substrate
Hysol 4402	Ablestik 84-1	Polyimide
Hysol 4450 (4451)	AI 8414	LTCC
Parylene C	ZVR-6000.2	Ceramic
HIPEC Q1-4939	TC-611	
UVE-1017-2	Ablebond 976-1	
	Ablebond 967-1	

Modeling

Wirebond Model

A geometric function will be selected to simulate a ball-wedge wire loop profile. Examples of the geometric function can be Lennard-Jones potential function, Weibull distribution function, lognormal distribution function, and cubit spline function. With appropriate boundary conditions, minimization of the potential energy developed from the geometric function will determine the parameter set. Thermal mechanical stress in the Au wire can be derived based on the deformation function and the wire properties. When encapsulation is used on the COB system, an additional set of boundary condition will be used to simulate a curved beam on a elastic foundation. An alternative method is to develop a special-purpose Raleigh-Ritz finite element approach to simulate and analyze stress in the wires. Figure 10 shows an initial diagram for the wirebond model. A chip attach model is planned as materials properties become available.

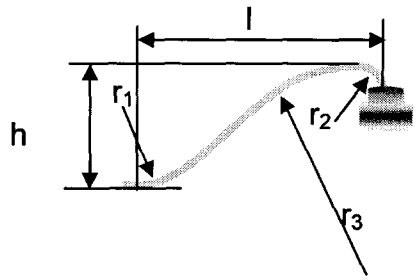

Figure 10. Diagram for Wirebond Modeling.

Results

The results presented here are taken from the experiment after a majority of the modules had seen 500 thermal cycles. The modules were installed in the cycle test chamber sequentially to accommodate the large number of modules in the experiment.

Measurement of all of the modules took place after 50 cycles, 300 cycles and 500 cycles. The first fifty cycles were not monitored live. After the first 50 cycles, 24 modules (384 channels) and rotated through different modules.

Typical temperature of the chamber is shown in Figure 11. This data is obtained from the average of four thermocouples across the chamber with a typical variation of less than ± 5°C during the ramps and ± 3° during the dwells.

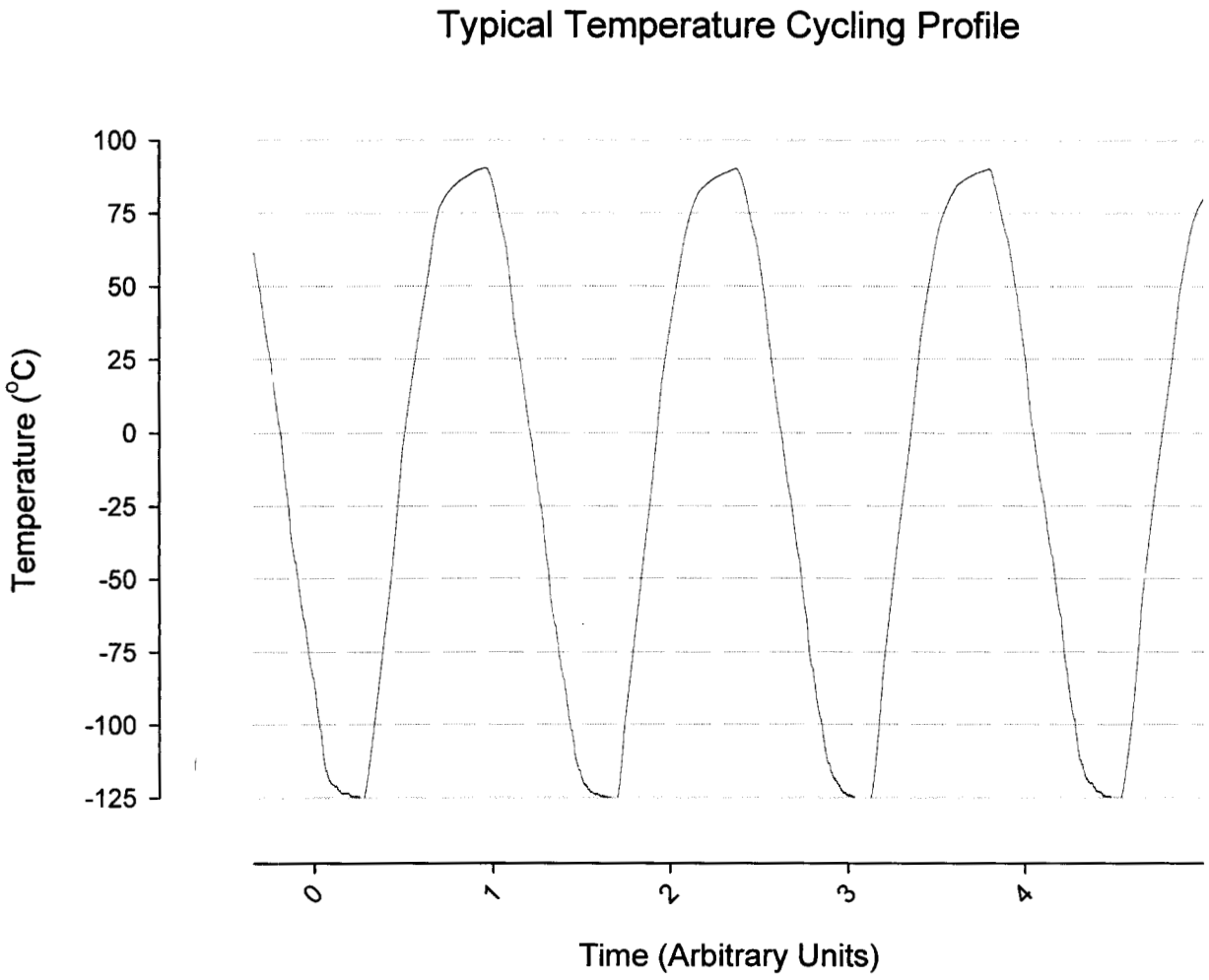

Figure 11. Typical environmental chamber temperature profile

A typical test vehicle substrate measurement is shown in Figure 12.

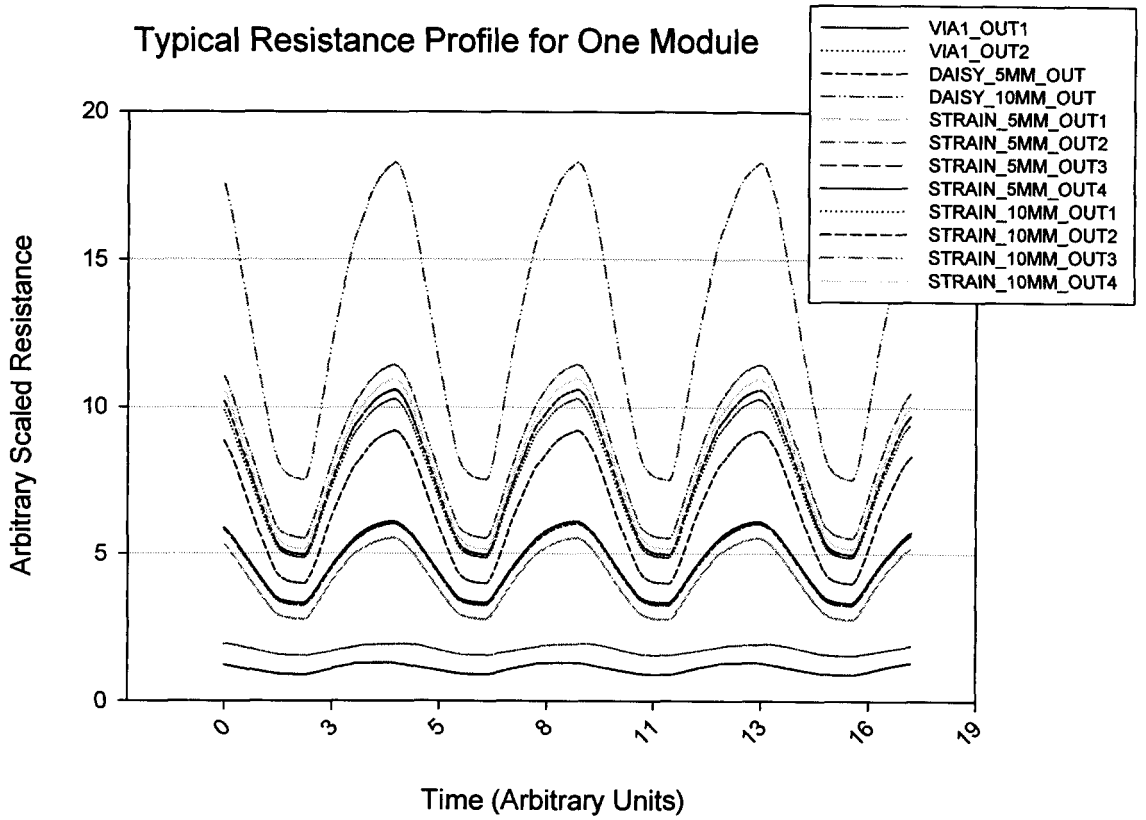

Figure 12. Resistance measurement of typical test vehicle.

The two bottom curves are for the two via chains. The central set of curves corresponds to the resistance gages and the daisy chain on the 5mm die with the uppermost being the daisy chain. The top set of curves corresponds to the resistance gages and the daisy chain for the 10 mm die. Again, the uppermost curve is the daisy chain. The resistances for the 2.2mm die were out of the range for the automated measurements and were only measured manually at intervals.

Some of the resistances were measured to be opens almost immediately. Others failed progressively by becoming noisy and eventually failing. Figure 13 shows one of the early intermittent portion of one of these failures near 500 cycles.

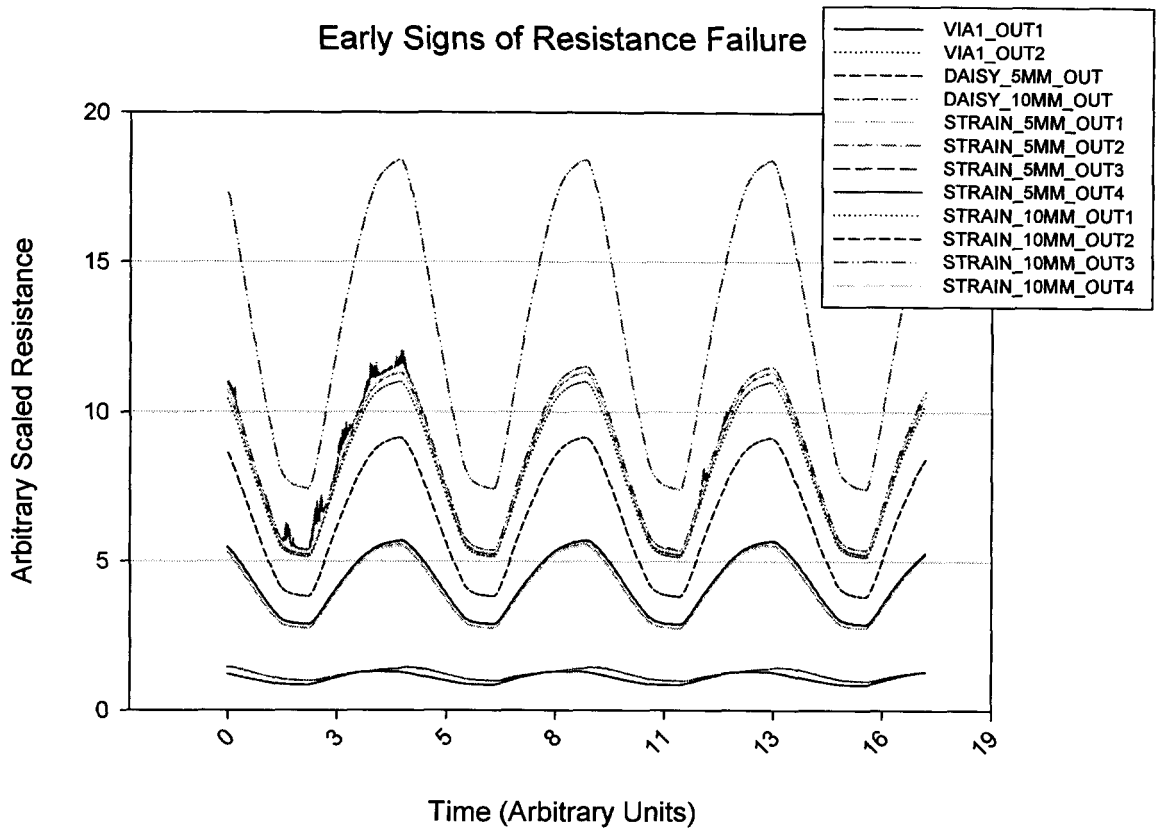

Figure 13. Intermittent failure of a resistance chain cycles.

A complete measurement of all modules was made periodically. Tables V and VI show the distribution of modules with at least one open circuit at 250 and 500 cycles. Note that not all modules started cycling at the same time, therefore not all combinations are represented on each table. All combinations of silicone die attach and epoxy overcoat and the combination of polyimide, solder and epoxy were removed after ~250 cycles and the test on these materials combinations discontinued due to excessive early failures. The measurements for all of the test vehicles were made at room temperature. Additional failures were found on selected vehicles that were monitored during the cycling process.

Table V. Failures after approximately 250 cycles for materials combinations seeing at least 250 cycles. Shaded areas indicate one or more open in resistance measurements.

Substrate	250 Cycle Survival Die Attach	Overcoat	Substrate Number										
Polyimide													
	Epoxy	Epoxy	-1		1096	1097	1117		1119	1121		1131	
	Epoxy	Silicone	-2	1001	1007	1015	1025	1026			1041	1112	
	Silicone	Epoxy	-4					1124				1129	1116
	Silicone	Parylene	-6	1069	1074	1049	1090	1091	1092	1098	1099	1108	-----
	Solder	Epoxy	-7										
Al2O3													
	Epoxy	Epoxy	-1	411	412	413	414	415	416	417	418	419	420
	Epoxy	Silicone	-2	321	322	323	324	325	326	327	328	------	330
	Silicone	Epoxy	-4		2			5			8	9	10
	Silicone	Parylene	-6	332	333	334	335	336	337	338	339	340	331
	Solder	Epoxy	-7	481	482		484		486	487		489	490
	Solder	Silicone	-8	401	-----	403	404	405	406	407	408	409	410
LTCC													
	Epoxy	Epoxy	-1	50	51	52	53	54	55	56	57	58	59
	Epoxy	Silicone	-2	27	28	29	30	38	40	41	42	44	49
	Silicone	Epoxy	-4	6			13		15	16	17	18	19
	Silicone	Silicone	-5	20	23	24	25	31	34	43	45	46	47
	Silicone	Parylene	-6	21	22	26	32	33	35	36	37	39	48
	Solder	Silicone	-8	008	005	077	060	079	072	078	063	076	------

Table VI. Failures after approximately 500 cycles for materials combinations seeing at least 500 cycles. Shaded areas indicate one or more open in resistance measurements.

Substrate	500 Cycle Survival Die Attach	Overcoat	Substrate Number									
Polyimide												
	Epoxy	Epoxy	1072	1096	1097	1117					1131	
	Silicone	Parylene	1069	1074	1049	1090	1091	1092	1098	1099	1108	-----
Al2O3												
	Epoxy	Silicone		322	323	324	325	326	327	328	------	330
	Silicone	Parylene	332	333	334	335	336	337	338		340	331
LTCC												
	Epoxy	Epoxy	50	51	52	53	54	55	56	57	58	59
	Epoxy	Silicone	27	28	29	30	38	40	41	42	44	49
	Silicone	Silicone	20	23	24	25	31	34	43	45	46	47
	Silicone	Parylene	21	22	26	32	33	35	36	37	39	48

X-ray images were taken of a number of the failures. These images show wirebond separation at the top of the arch and at the ball. Figures 14 and 15 show examples of x-ray images of these failures.

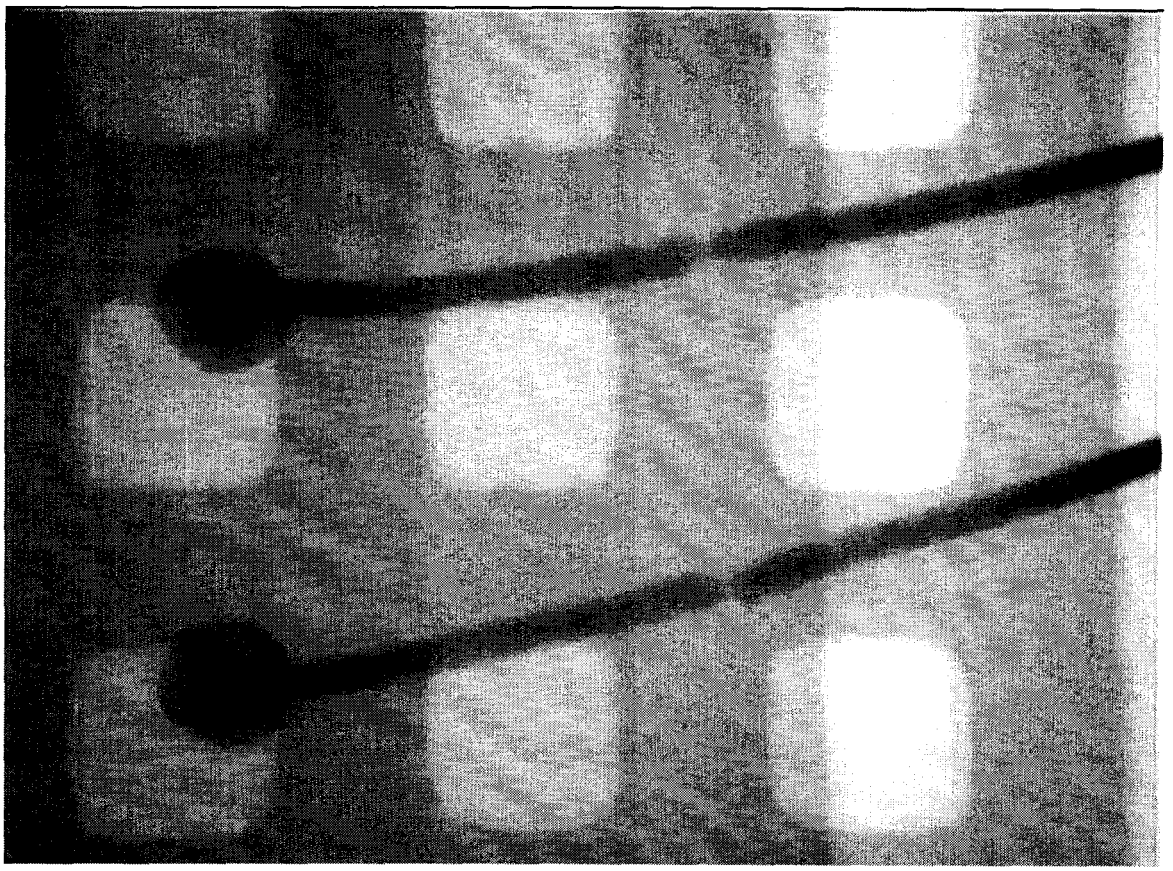

Figure 14. X-ray image of wirebond top of arch failure.

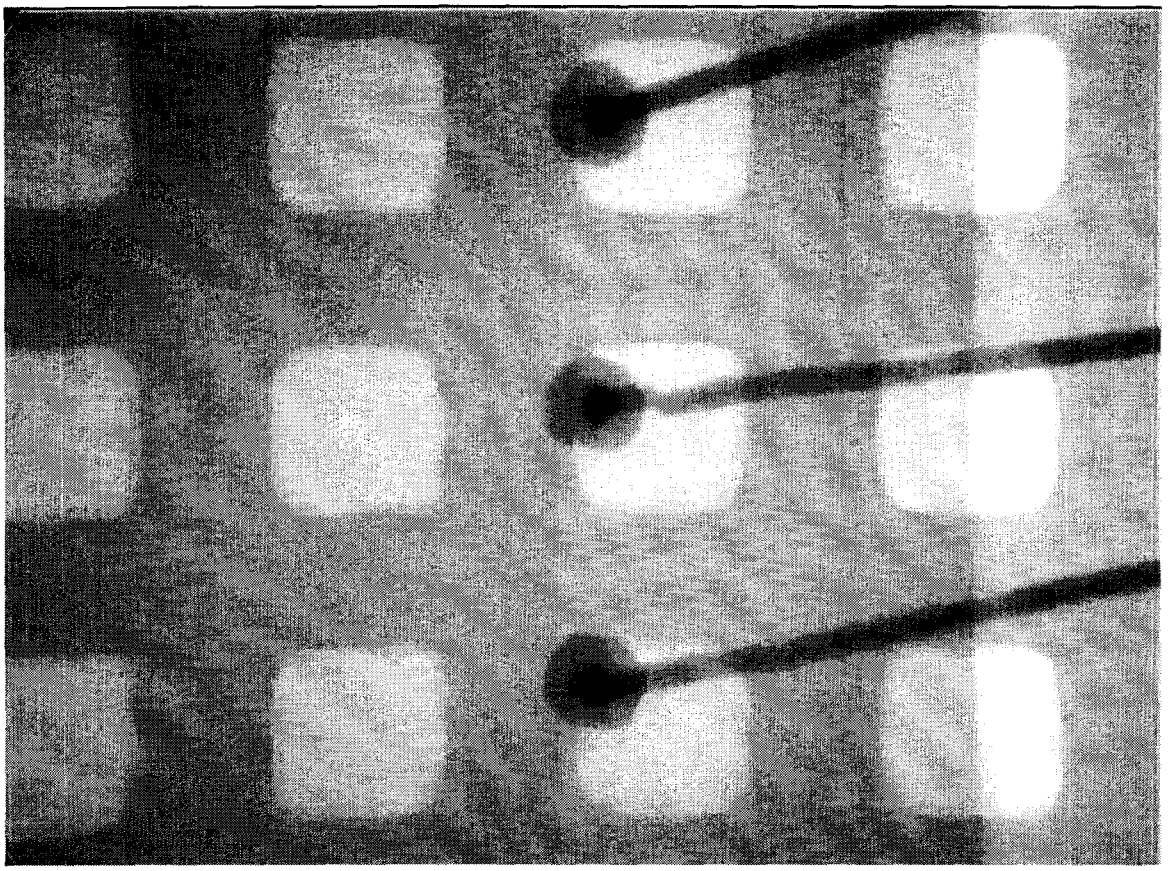

Figure 15. X-ray image of wirebond break near ball.

Discussion

The chamber typically approached 90°C at its peak and -128°C at is low end. The profile was designed to make sure all objects in the chamber were above 85°C or below -120°C for more than five minutes.

Since all of the conduction paths measured were entirely metallic, typical change in resistance of metallic conductors as a function of temperature was observed. This change in resistance is attributed to reduction of phonon interference with the electron drift velocity as temperature is reduced.

A calibration die was added, suspended by Kapton tape. This die has essentially no stresses on it due to manufacturing. The resistance values obtained from it may therefore be subtracted from the mounted die. Any trends or hysteresis should be clear from this de-convolution. Figure 18 shows an example of the de-convoluted plot.

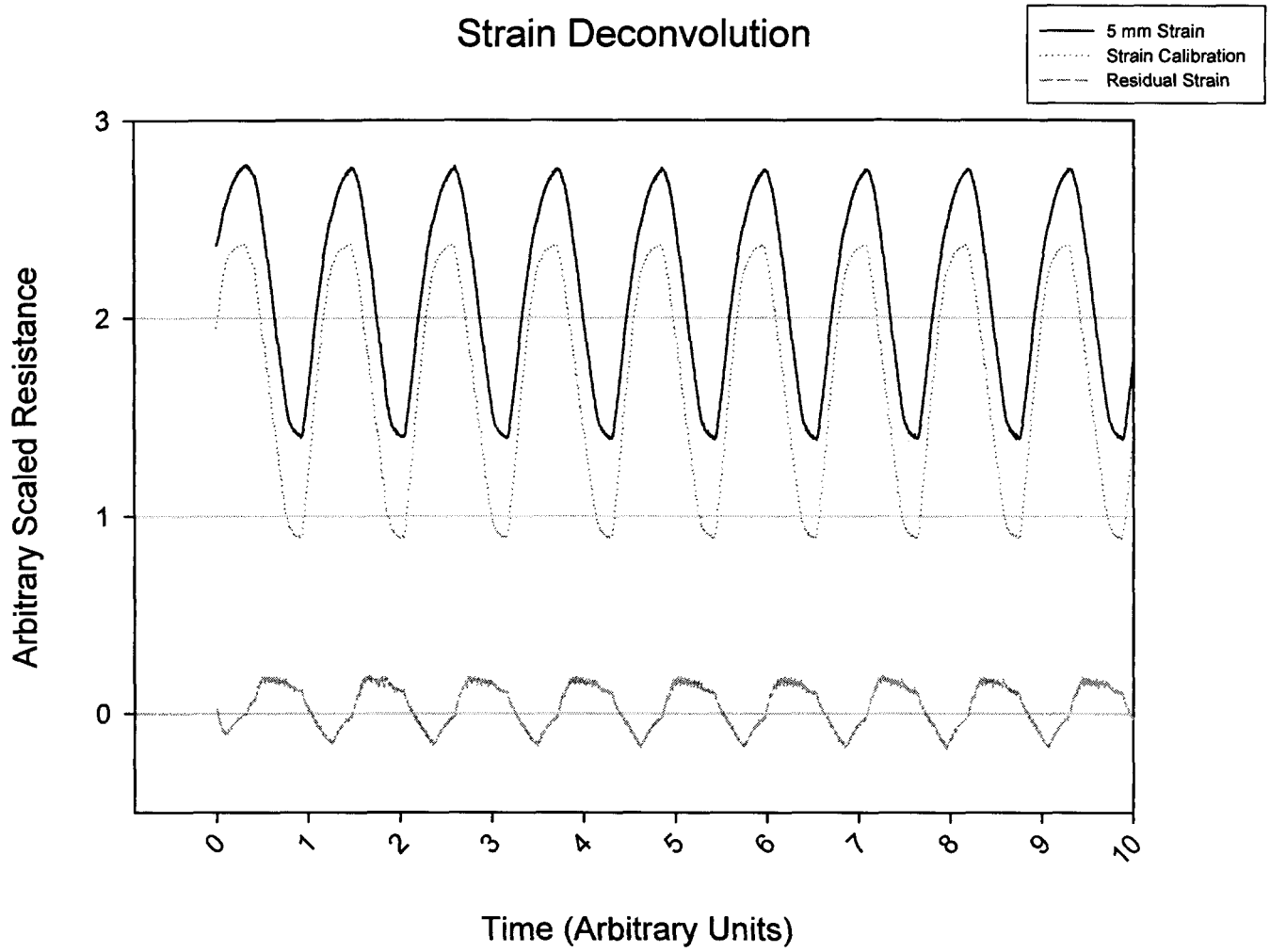

Figure 16. De-convoluted cycle plot subtracting the total metal resistance change from the measurement.

Early modeling results show that the highest stress areas for the wirebonds are at the top of the arch and near the ball. The materials characterization and modeling efforts are still in their early stages and will be reported on, in detail, at a future time.

Conclusion

- All combinations of epoxy overcoat and polyimide substrate or silicone die attach are not viable.
- Intermittent failures were detected during cycling indicating that rapid or continuous monitoring is necessary
- Six of eight combinations that made it to 500 cycles have no failures

- An additional three combinations made it to 250 cycles with no failures
- Wirebond breakage is the only failure mode detected so far
- Preliminary models are in exact agreement with observed failures

Acknowledgements

This work was performed under the NASA's Mars Focused Technology at JPL (JPL contract number 102159)

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