Single-Event Upset in Evolving Commercial Silicon-on-Insulator Microprocessor Technologies

F. Irom, *Member, IEEE*, F.H. Farmanesh, G.M. Swift, *Member, IEEE, and* A.H. Johnston, *Fellow, IEEE, and* G. I. Yoder

***Abstract* –Single-event upset effects from heavy ions are measured for Motorola and IBM silicon-on-insulator (SOI) microprocessors with different feature sizes and core voltages. Multiple-bit upsets (MBU) in registers and were measured and compared with single-bit upsets. Also, the scaling of the cross section with reduction of feature size for SOI microprocessors was discussed.**

I. Introduction

Single-event upsets (SEU) have been a concern for many years for integrated circuits operating in space environments. A basic method for improving the SEU immunity without degrading the performance is to reduce the SEU-sensitive volume. This can be accomplished through the use of silicon-on-insulator (SOI) substrates. For SOI processes the charge collection depth for normally incident ions is reduced by more than an order of magnitude compared to similar processes fabricated on epitaxial substrate. SOI technology has potential advantages for SEU compared to CMOS bulk counterparts, because, from a fundamental standpoint, charge collection is limited to the shallow depth of the silicon film. However, other factors, such as lower operating voltages, reduced junction capacitance and amplification by parasitic bipolar transistors may limit the degree of improvement in SEU sensitivity that can be obtained with commercial SOI processors [1].

Commercial microprocessors with the PowerPC architecture are now available that use partially depleted silicon-on-insulator processes to improve performance. A recent study of first-generation SOI microprocessors from two different manufacturers showed that although the cross section was lower than for processors with bulk/epitaxial substrates, the threshold LET was very nearly the same [2]. An early study of charge collection by Massengill, *et al.* [3] as well as more recent work on the sensitivity of SOI structures to neutrons and alpha particles [4,5] have shown that charge multiplication by the parasitic bipolar structure increases the collected charge by as much as a factor of ten compared to charge deposited by the primary particle interaction. That mechanism is the likely reason for the low threshold LET of commercial SOI processors. Although manufacturers consider atmospheric radiation effects in their designs [6,7], the relatively low charge produced by alpha particles and neutrons is roughly equivalent to an LET of 2 MeV- cm^2/mg. Thus, hardening efforts by manufacturers are relatively ineffective in improving radiation hardness in the more severe environments in space.

Upsets in the L1 cache – a 256-kbit D-Cache and 256-kbit *i*-cache for the latest PowerPC devices - are the largest contribution to upset rates for most applications of unhardened commercial processors. The sensitivity of the cache to SEUs and multiple-bit upsets (MBUs) is of great concern for microprocessors in space. This paper examines single-event upset in advanced SOI commercial microprocessors, comparing upset sensitivity in registers and the D-Cache for several generations of devices with different feature sizes and core voltages. Multiple-bit upsets and asymmetry in register and cache Multiple-bit upset cross sections are also discussed. Results are presented for SOI processors with feature sizes of 0.18 and 0.13 μm.

II. Experimental Procedure

A. Device Descriptions

The Motorola 7455 and IBM 750FX are the first generation of the PowerPC family to be fabricated with SOI technology. They use partially depleted technology without body ties. The Motorola device has a feature size of 0.18 μm with a silicon film thickness of 110 nm and internal core voltage of 1.6 V. A low power version of this processor operates with internal core voltage of 1.3 V. The IBM part is fabricated with a more scaled process, using a feature size of 0.13 μm, silicon film thickness of 117 nm and core voltage of 1.4 V [8]. Both devices are packaged with "bump bonding" in flip-chip BGA packages.

Recently, a more advanced version from Motorola, with a feature size of 0.13 μm, silicon film thickness of 55 nm and internal core voltage of 1.3 V, has been announced. SEU measurements with this device provides a direct comparison of the effects of scaling and process changes for current SOI processes with regard to radiation hardness for devices from a single manufacturer.

Table 1 summarizes the recent SOI generation of the PowerPC family. The feature size is reduced from 0.18 to 0.13 μm, with core voltage reduced from 1.6 to 1.3 V. The die size ranges from 34 to 106 mm^2 and transistors count ranges from 33 to 58 million.

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F. Irom, F.H. Farmanesh, A.H. Johnston, and G.M. Swift are with Jet Propulsion Laboratory, California Institute of Technology, Pasadena, CA 91109 USA (email: farokh.irom@jpl.nasa.gov)

G.I. Yoder is with NASA Johnson Space Center, Houston, TX 23681 USA (email : geoffrey.l.yoder@nasa.gov)

Table 1. Comparison of Motorola and IBM SOI PowerPC Family of Advanced Processors.

DEVICE	Feature Size (μm)	Die Size (mm^2)	Transistors Count (million)	Core Voltage (V)
Motorola 7455	0.18	106	33	1.6
Motorola 7455*	0.18	106	33	1.3
Motorola 7457	0.13	98	58	1.3
IBM 750FX	0.13	34	33	1.4

* This is a special low power version of the Motorola SOI PowerPC 7455.

B. Experimental Methods

Radiation testing was done at the Texas A&M cyclotron, irradiating devices from the back of the wafer (package top), correcting the LET to account for energy loss as the beam traversed the silicon. Details of the testing, and ion energies are described in [2,9].

A complex method was required to examine Multiple-bit errors in L1 D-Cache. The D-Cache was initialized under specified conditions prior to irradiation and then disabled. Then a clearly recognizable pattern, designed to be distinctly different from contents of the cache, was placed in the external memory space covered by the cache. In our test method, "do noting with strip chart", the processor was programmed to perform a one word instruction in a small infinite loop and write a snapshot of the upper half of the D-Cache to a strip chart in the physical memory every half second. After the irradiation ended, an external interrupt triggers a program to count state changes in the D-cache. Also, very low flux rate $2x10^2$ and short irradiation time were used for MBU measurements.

III. Test Results

A Register Tests

Motorola Processors

Fig.1 displays results of cross section measurements for the Motorola SOI PowerPCs 7455 (feature size 0.18 μm). Registers (sum of FPR, GPR, and SPR) for "0" to "1" and "1" to "0" transitions. Note the pronounced asymmetry in the response. The threshold LET for "0" to "1" transitions is about 6 MeV-cm^2/mg, about a factor of six higher than for transitions in the opposite direction. The cross section for the two logic directions is also different.

We repeated SEU measurements on a special version of Motorola PowerPC 7455 that operates with lower internal core voltage, 1.3 V. The asymmetry in Registers was more pronounced.

Recently, we measured SEU on a new advanced version of the SOI processor from Motorola, PowerPC 7457. The Motorola PowerPC 7457 has a feature size of 0.13 μm and internal core voltage of 1.3 V. Similar asymmetry but more pronounced was observed for this new processor.

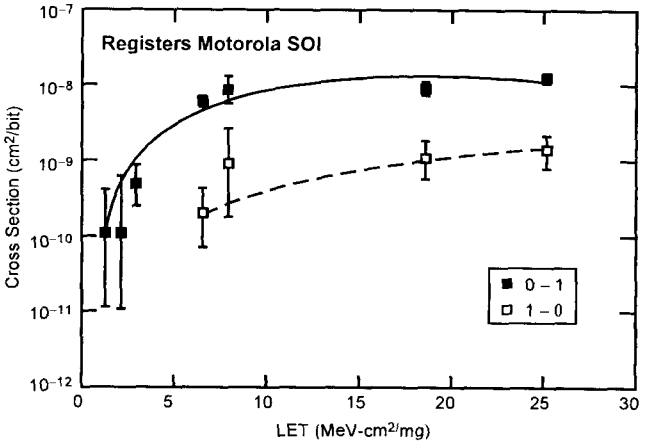

Fig. 1. Heavy-ion cross-sections for registers (FPR+GPR+SPR) of the Motorola SOI PowerPC 7455 for "1" to "0" and "0" to "1" upsets

IBM Processors

A similar asymmetry was observed between "0" to "1" and "1" to "0" upsets for the IBM SOI PowerPC registers (FPR+GPR+SPR), although the asymmetry was reversed (worst for "1" to "0" upsets) compared to results for the SOI processor from Motorola. Fig. 2 shows the results. The saturated cross section for "1" to "0" upsets is 7 x 10^{-9} cm^2/bit.

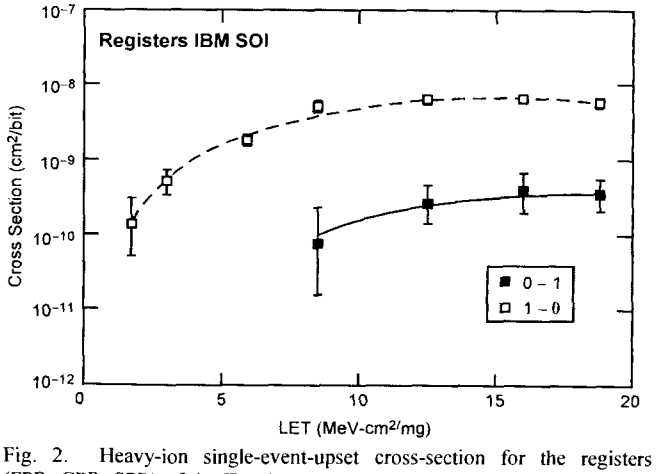

Fig. 2. Heavy-ion single-event-upset cross-section for the registers (FPR+GPR+SPR) of the IBM750FX SOI PowerPC for "1" to "0" and "0" to "1" upsets.

It is interesting to note that asymmetry was barely evident in register tests of the Motorola G4 processor, with bulk substrate, as shown in figure 3. Note that exactly the same test approach was used for both types of processors. The saturated cross section of the SOI processor is about 10^{-8} cm^2/bit, about an order of magnitude lower than that of CMOS epi PowerPC (G4), which has nearly the same feature size as that of the 7455 SOI version. Similar differences in cross section between SOI and bulk technology devices were reported in Reference 10 and 11.

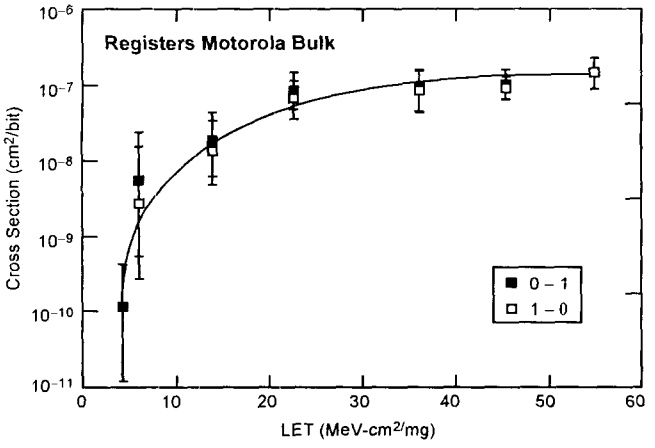

Fig. 3. Heavy-ion single-event-upset cross-section for the Registers (FPR+GPR+SPR) of the Motorola 7400 PowerPC for "1" to "0" and "0" to "1" (older bulk processor, not SOI)

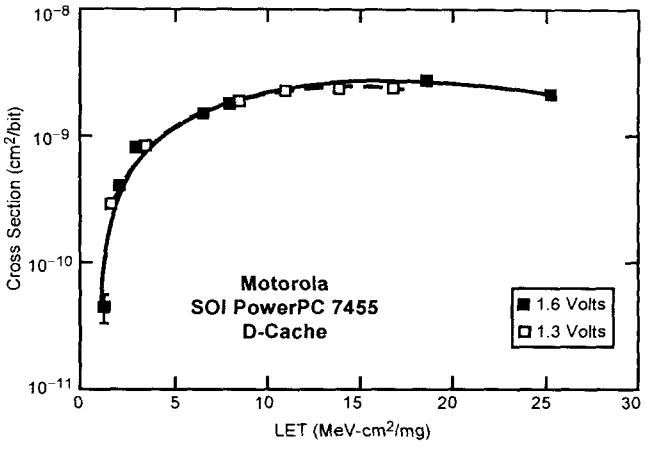

Fig. 4. Comparison of the heavy-ion single-event-upset cross-section for the D-Cache of the Motorola 7455 with two different internal core voltages.

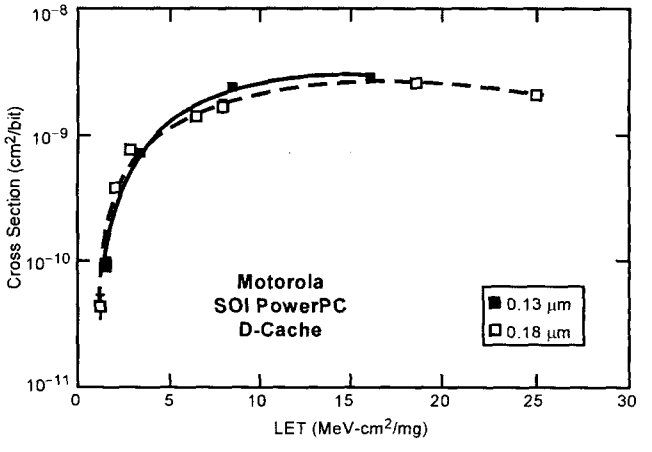

Fig. 5 Heavy-ion single-event-upset cross-section for the D-Cache of the Motorola 7455 and 7457 PowerPC's.

B Cache Tests

We reported SEU measurements on the for Motorola SOI PowerPC 7455 and IBM PowerPC 750FX (feature size 0.13 μm) [2]. Tests of the D-Cache in the SOI version of the Motorola and IBM processors did not show the asymmetry in response for different stored logic levels that was seen in the register tests; the cross section was the same for upsets in both directions in the SOI processors as well as the CMOS bulk (with epi- substrate) counterparts. The "saturation" cross section at high LET, where the curve becomes nearly flat, was about a factor of three lower for the cache than that observed for registers for both the SOI and bulk processor types. This is directly related to the more compact design used for 6-T memory cells within the cache compared to memory cells in the registers [12].

We also repeated SEU measurements on a special version of Motorola PowerPC 7455 that operates with lower internal core voltage, 1.3 Volts. Fig. 4 compares the result of the measurements on the Motorola PowerPC 7455 with core voltage of 1.6 Volts [2] with the results of the Motorola PowerPC 7455 with l core voltage of 1.3 Volt. There is no change in SEU cross section for D-Cache.

Recent, measurements of the D-Cache SEU on the SOI PowerPC 7457 shows that similar to the previous D-Cache SEU measurements, the cross section for "1" to "0" transitions is the same as that for "0" to "1" transitions. Fig. 5 compares result of the D-Cache for this new processor with results for PowerPC 7455. The large number of storage locations within the data cache allows more statistically significant numbers of errors to be measured, decreasing the error bars due to counting statistics. The error bars are ~2 sigma and result from Poisson statistics. For the data points where statistical error bars are not shown, they are smaller than the size of the plotting symbols.

It is somewhat surprising that the SEU results for the two SOI processors are so similar, given the difference in feature size and core voltage. Similar agreement was observed between D-Cache results for IBM PowerPC 750FX and Motorola PowerPC 7455 [2]. These results suggest that scaling between 0.18 and 0.13- μm feature size has little effect on SEU sensitivity. However, this trend may not continue as devices and core voltages are changed to even lower values.

C Functional Errors ("Hangs")

We also examined complex functional errors ("hangs") where the processor operation is severely disrupted during irradiation. We detected hangs by applying an external interrupt after the irradiation was ended; if the processor responded to the interrupt, then the processor was still operational to the point where normal software means could likely restore operation. If the interrupt could not restore operation, then the status was categorized as a "hang." In nearly all cases, it was necessary to temporarily remove power from the device in order to recover, and reboot the device.

In order to roughly scope problems with hangs, we calculated the hang cross section defined as the number of times the processor would not respond to the external interrupts divided by the total fluence to which the processor had been exposed, including runs with no observed hangs. This was done for each LET. Figure 6 compares estimated cross section for hangs for two nominal internal core

voltages during heavy-ion SEU measurements of the PowerPC 7455. The threshold LET appears comparable to that obtained for register and errors. The cross section per device due to "hangs" is about 10^{-6} cm^2 for LETs above 6 MeV-cm^2/mg.

Although the *threshold* LET for "hangs" is low, the cross section is small enough so that the expected incidence of "hangs" is not very high in typical space environments. For example, the probability of "hangs" from galactic cosmic rays is about one in 25 years for the Motorola SOI processor.

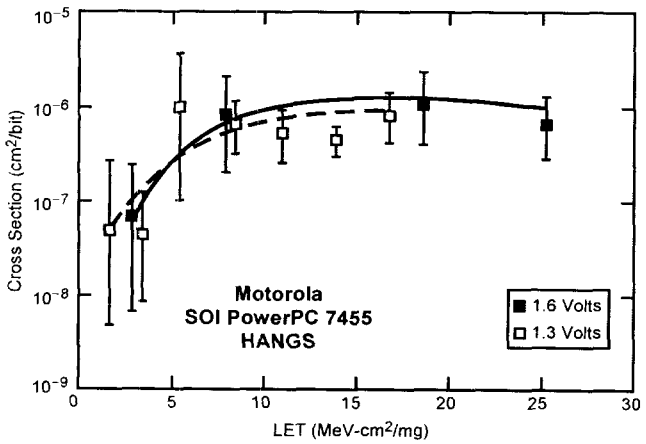

Fig. 6. Comparison of the heavy-ion single-event-upset cross-section for the hangs of the Motorola SOI PowerPC 7455 with two different internal core voltages.

D Multiple-Bit Upsets

Measurements of multiple-bit upsets are not straightforward for these complex devices because of the latency period that is needed between successive measurements of registers or cache. Low flux rates are required, which conflicts with many of the requirements for detecting single-bit errors, functional errors, and doing tests in a time-efficient manner. We measured multiple-bit errors on the registers and D-Cache.

Figures 7 shows the multiple-bit upset rate – defined as two or more bit upsets in the D-Cache for the Motorola SOI PowerPC 7455. For comparison we also show results for single upsets. The MBU upset rate is about 200 times lower, and begins to occur at relatively low LETs. The MBU upset rate for the register is about 20-25 times lower compare to the single rates and also, begins to occur at relatively low LETs. These results are somewhat surprising because of the very shallow charge collection depth from the silicon film (110 nm for this device). This is discussed further in section IV.

IV. Discussion

A. Scaling Trends

Scaling for high-performance technologies depends heavily on reducing feature size, but also requires a reduction in power supply voltage [14]. Considerable work has been done showing that the critical charge for scaled devices is expected to be lower for more advanced devices [15]. This often leads to the conclusion that single-event

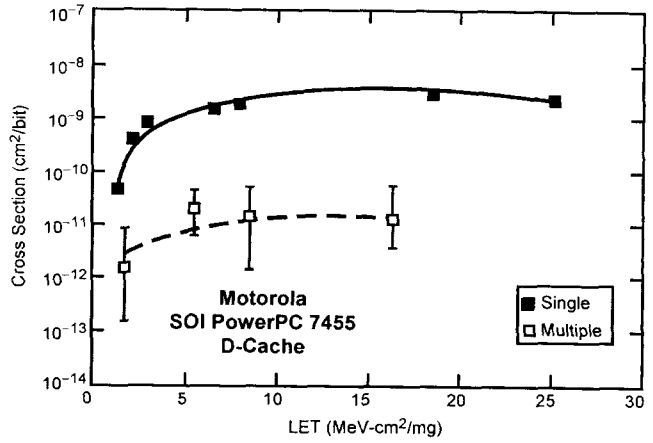

Fig. 7. Comparison of MBUs and SEU cross-sections for registers of the Motorola SOI PowerPC 7455.

upset will be far more severe for highly scaled devices. However, this has not been observed for high-performance devices such as microprocessors [16]. Other factors cause less charge to be collected as devices are scaled to smaller feature size. As discussed in the Introduction, the threshold LET of commercial processes has changed very little with scaling, and is only slightly influenced by the concerns of mainstream manufacturers with atmospheric radiation. However, the saturation cross-section has steadily decreased with smaller feature size. Fig. 8 shows how the cross section for registers has changed over several generations of the PowerPC family [the abscissa is a logarithmic (*base 2*) inverse of scale reflecting the approximate doubling of feature size over various generations of CMOS devices]. The dashed lines show a slope of minus one-half, reflecting the assumed dependence of area on the square of the feature size. There is a decrease of nearly a factor of ten in cross section with the transition to SOI processes.

The earliest results, with 0.5 μm feature size, are from Bezerra, *et al.* in 1997 [13]. New results for test SRAMs from the Sandia CMOS-7 SOI process are also include from Dodd, *et al.* [14]. The Sandia results agree well with the results from the two SOI processors, which have even smaller feature size.

A similar plot for saturation cross sections of the D-Cache is shown in Fig. 9. Again, the cross section trend for SOI processors is about a factor of ten lower than for bulk devices. Note also that the cross section for the D-Cache is a factor of 2.5 to 4 lower than the cross section for registers in the previous figure. That difference is due to the smaller cell area used for cache design, which optimizes performance and reduces chip area. The gate and drain area of transistors in the IBM cache, provided by the manufacturer, are shown for comparison. The total cross section is slightly less than the sum of the areas of the drain and gate, which agrees with results obtained by the Sandia group in microbeam studies of devices from their SOI process, with 0.35 μm feature size [14].

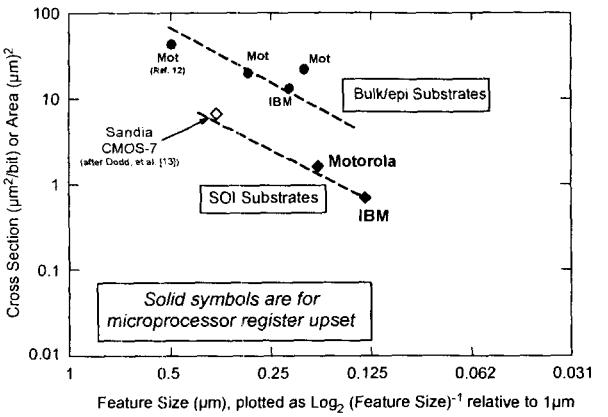

Fig. 8. Scaling trends for upset in registers (and basic SRAM designs) for Power PC processors. Results for test SRAMs from Dodd, et al. [13] are also included for comparison.

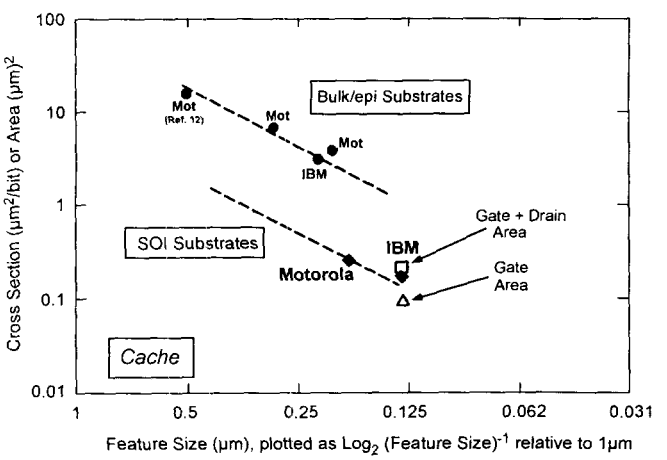

Fig. 9. Scaling trends for upset in D-Cache for PowerPC processors.

The effect of scaling on partially depleted SOI structures is a far more difficult problem. The main advantage of SOI is marked reduction in the thickness of the silicon region for charge collection. To first order, this should decrease the collected charge by more than an order of magnitude compared to bulk/epi devices with equivalent feature size, increasing the threshold LET by at least a factor of ten. However, charge amplification from the parasitic bipolar transistor that is inherent in partially depleted SOI increases the charge by a significant factor. Although the charge amplification effect can be reduced by adding body ties to the structure, that increase the area. Neither of the two SOI processor in our studies use body ties.

Feature sizes, Silicon film thickness and internal core voltages are critical factors in SOI single-event upset. Reduction in feature size should reduce the SEU sensitivity. Decreasing the silicon film thickness increases bipolar gain and reducing the internal core voltage limits the degree of improvement in SEU sensitivity that can be obtained with commercial SOI processors. Table 1 shows the feature sizes, film thickness, and internal core voltages for the SOI generations of the PowerPC family.

Table 1. Summary of Motorola and IBM SOI PowerPC Processors Family.

Device	Feature Size (μm)	Film Thickness (nm)	Core Voltage (V)
Motorola 7455	0.18	110	1.6
Motorola 7455*	0.18	110	1.3
Motorola 7457	0.13	55	1.3
IBM 750FX	0.13	117	1.4

* This is a special low power version of the Motorola SOI PowerPC 7455.

Fig. 5 compares SEU cross-section for D-Cache for PowerPC 7455 operated in two different internal core voltages (1.6 and 1.3 Volts). Clearly there is a good agreement between two sets of data. Although, one might expect cross section with lower core voltage might be larger cross section because of noise.

Reference 2 studied D-Cache measurements for the Motorola 7455 and IBM 750FX. The film thicknesses of the two SOI processors are very the similar. However, the feature size of the IBM device is smaller -0.13 μm- compared to the 0.18 μm feature size of the Motorola device. Their measurements shows that the single-event upset results for two SOI processors are similar, given the difference in feature size and core voltage.

Fig. 4 displays the comparison of D-Cache measurements for the Motorola 7457 and 7455. There is a very good agreement between the data. Also, there is a good agreement between these data with D-Cache result of the Ref. 1 for IBM 750FX. The similarity between D-Cache results of the Motorola 7457 and IBM 750FX is somewhat surprising. The feature size and core voltage of two processors are the same. However, the film thickness of the Motorola 7457 is much smaller - 55 nm – compared to the 117 nm film thickness of the IBM 750FX.

Charge collection will be lower when feature sizes are reduced below about 0.25 μm because the lateral distribution of charge from the ion track will extend beyond the active area. The decreased junction area and lower voltage (required from scaling laws) both contributed to the reduced charge collection. This suggests that charge collection efficiency may be one of the reasons that the overall SEU sensitivity of advanced processor is only slightly affected by scaling. The decrease in critical charge is compensated by smaller area along with decrease charge collection efficiency.

Although it is useful and instructive to make comparisons of single-event upset results as microprocessors within a given family evolve, one must remember that these are complex devices, not test structures. Other factors in the processor design may also affect the way that different processors in the series respond to radiation. There are also different requirements for various registers and functions within the device. For example, access time is a critical

requirement for on-board cache, but cache single-event upset results may not be representative of other types of registers within the device.

The combination of the transition to SOI technology and the decrease in feature size reduces the error rate in deep space by more than a factor of 30 compared to error rates calculated for the Motorola PowerPC 750 (bulk/epi substrate with 0.29 μm feature size) [9]. The error rate in deep space (solar minimum) decreases from 10^{-6} to 3×10^{-8} errors per bit day, and would be approximately halved by taking the asymmetric cross section into account. That is an impressive reduction.

B Multiple-Bit Upset

The sensitivity of the Motorola SOI device to multiple-bit upset was unexpected, because earlier work showed that SOI upset only occurs for gate strikes. However, more recent work has shown that strikes in the drain also contribute to the cross section [17]. The substrate charge collection mechanism that they observed has not been reported in work done by the electron device community, which concentrates on upset effects from alpha particles and atmospheric neutrons, but workers in the device community have not considered the possibility of charge collection beyond the confines of the buried oxide. The substrate charge collection provides a possible mechanism for charge sharing between adjacent isolated films in partially depleted SOI from a particle strike in regions that are closer to the isolation regions. Schwank, *et al.,* discussed the possibility of MBU from displacement currents in the underlying isolation oxide, which is a potential mechanism for MBU in these devices [19].

C Design Issues

Although future processors may use DRAMs, the cache and registers in these processors use 6-T SRAM cells. Design of compact SRAM cells is extremely complex. Although SOI provides some advantages, the history dependence, pattern dependence from bipolar currents and self-heating must all be taken into account [19]. New circuit design approaches using low threshold transistors improve speed and power dissipation, but reduce internal noise margin [20]. These factors, along with geometrical factors (such as extended regions for contacts, which causes asymmetric cross sections in earlier work on 4-T SRAMs [21]) may contribute to the asymmetric cross sections that were observed for registers in the SOI processors.

V. Conclusions

This paper has discussed scaling trends for SEU from heavy ions in the Power PC family of microprocessors, emphasizing upsets in registers and cache. The latest versions of these processors have error rates that are more than 30 times lower than PowerPC 750 processors because of the reduced feature size and the transition to SOI. Multiple-bit upsets were observed in register and D-Cache tests of an SOI processor with 0.18 μm feature size. This is not only important from a fundamental standpoint, but makes implementation of error correction methods more difficult.

For SOI processors with same feature size and silicon film thickness, but different internal core voltages we did not notice any voltage dependence.

There is not a change in SEU cross section for the SOI processors with feature sizes of 0.13 and 0.18- μm. These results suggest that scaling between 0.18 and 0.13- μm feature size has little effect on SEU sensitivity. However, one might expect to see drop in saturated cross section when there is a drastic change in feature size e.g. 0.06 μm (next generation of SOI)

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