Noise Performance of 0.35-μm SOI CMOS Devices and Micropower Preamplifier Following 63-MeV, 1-Mrad (Si) Proton Irradiation

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35-WORD ABSTRACT

This paper presents measured noise for 0.35-μm, silicon-on-insulator devices and a micropower preamplifier following 63-MeV, 1-Mrad (Si) proton irradiation. Flicker noise voltage, important for gyros having low frequency output, increases less than 32% after irradiation.

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1. INTRODUCTION

Analog circuits fabricated in silicon-on-insulator (SOI) CMOS processes have the potential of maintaining required performance over the extreme temperature and radiation environment of deep space. Low input-referred white noise voltage is required to amplify low-level signals from mission sensors. Additionally, low flicker noise voltage is required for gyros and other mission sensors that have important low frequency content. Low noise performance must be obtained over environmental radiation extremes and at micropower levels due to the weight limitations of space power sources.

2. RADIATION EFFECTS ON MOS FLICKER NOISE

Radiation effects on MOS low-frequency flicker noise have been discussed in the literature [1, 2], and it is generally accepted that interactions between carriers and defects near the Si/SiO_2 interface are responsible for flicker noise [2]. MOS gate-referred, flicker-noise voltage, power-spectral density is given by

$$S_{V,flicker} = \frac{K_F}{C_{OX}^2\, W\, L f^{AF}} \text{ (V}^2\text{/Hz)}. \quad (1)$$

In this commonly used bias independent, carrier-density fluctuation model, K_F (C^2/cm^2) is the flicker noise factor, AF is the flicker-noise slope, f is the frequency, W is the channel width, L is the channel length, and C_{OX} is the gate-oxide capacitance. The flicker noise voltage is dependent on the process (PMOS flicker noise is generally lower than NMOS flicker noise) and the total MOS gate area. Low flicker noise requires large area MOS devices like those used in the preamplifier described here.

The measured NMOS flicker noise factor for a 1.2-µm, SOI CMOS, SIMOX process increased from 2.83×10^{-31} to 20.8×10^{-31} C^2/cm^2 following ^{60}Co gamma irradiation to a total dose of 25 Mrad (Si) [3]. The PMOS flicker noise factor increased from 1.37×10^{-31} to 6.90×10^{-31} C^2/cm^2 for the same total dose. The reported NMOS flicker noise factor for a thinner gate-oxide, 0.25-µm bulk CMOS process increased from 2.2×10^{-31} to 5×10^{-31} C^2/cm^2 following 10-keV x-ray irradiation to a total dose of 100 Mrad (SiO_2) [4]. The PMOS flicker noise factor increased from 0.34×10^{-31} to 2.2×10^{-31} C^2/cm^2 for the same total dose. These results suggest that a modest increase in flicker noise could be expected for the 1-Mrad (Si) proton dose considered here, although it is not known if flicker noise has been reported following proton irradiation.

3. EXPERIMENTAL METHODS

The test devices and micropower preamplifier were fabricated in Honeywell's 0.35-µm partially-depleted SOI CMOS process using UNIBOND SOI material [5]. The total dose performance of this process has been reported at room temperature [6] and at 77 K [7]. Total dose performance following proton irradiation has been recently reported [8]. Noise performance following irradiation has not been previously reported.

The test devices and micropower preamplifier were irradiated with 63.3 MeV protons at the Crocker Nuclear Laboratory at the University of California at Davis. Dosimetry measurements used a five-foil secondary emission monitor calibrated against a Faraday cup and are accurate to about 10%. A biased integrated circuit and a second, unbiased (all pins grounded) integrated circuit were irradiated to a total dose of 1 Mrad (Si).

4. MOS DEVICE PERFORMANCE FOLLOWING PROTON IRRADIATION

A PMOS device identical to the one of the preamplifier input devices was evaluated along with a NMOS device identical to one of the preamplifier non-input devices. The PMOS device with dimensions of W/L = 100 µm/20 µm was biased in moderate inversion at a drain current of -0.5 µA. Operation in moderate inversion is used for this preamplifier input device to achieve high transconductance for the operating bias current. This minimizes input-referred white noise voltage and ensures input devices

dominate preamplifier noise. The NMOS device with dimensions of $W/L = 30$ µm/75 µm was biased in strong inversion at a drain current of 1.0 µA. Operation in strong inversion lowers the transconductance for the operating bias current, thereby minimizing the non-input device preamplifier noise contributions. The test devices were diode-connected (drain connected to the gate) and continuously biased in saturation at their operating drain currents during and after irradiation.

The measured input-referred, gate noise voltage density for the PMOS and NMOS devices is shown in Figures 1 and 2 respectively before and after 1-Mrad (Si) proton irradiation. Following irradiation, the flicker noise voltage density at 1 Hz increases 24% for the PMOS device and 32% for the NMOS device while the white noise remains unchanged. Table I lists the gate-source voltage, transconductance, output conductance, white noise density, flicker noise density at 1 Hz, flicker noise factor, flicker noise slope, and flicker noise corner frequency for the devices both before and after irradiation. Transconductance and white noise remain unchanged while output conductance appears to increase following irradiation. This will be investigated further as the output conductance is quite low and difficult to measure for these long-channel devices. The flicker noise factors, related to flicker noise power spectral density at 1 Hz, increase 58% and 76% for the PMOS and NMOS devices respectively.

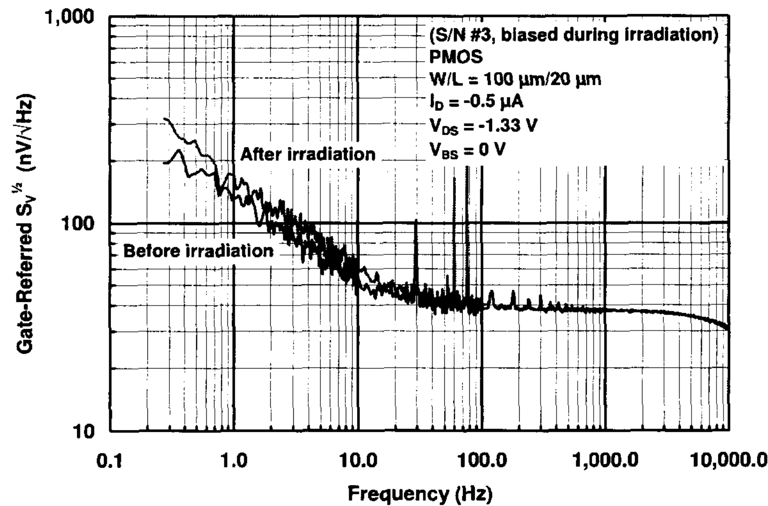

Figure 1. Measured PMOS input-referred noise voltage density before and after irradiation.

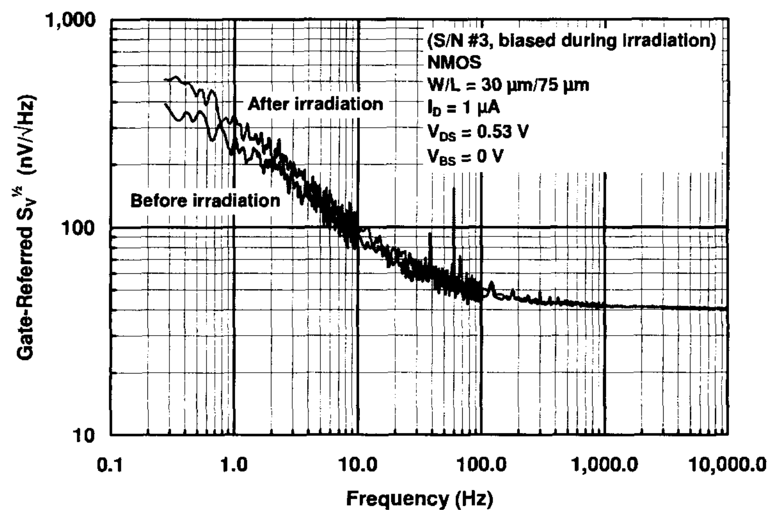

Figure 2. Measured NMOS input-referred noise voltage density before and after irradiation.

TABLE I

DEVICE TRANSCONDUCTANCE, OUTPUT CONDUCTANCE, AND NOISE BEFORE AND AFTER IRRADIATION

	V_{GS} (V)	g_m (μS)	g_{ds} (nS)	$S_V^{1/2}{}_{white}$ (nV/√Hz)	$S_V^{1/2}{}_{total\ @\ 1\ Hz}$ (nV/√Hz)	KF (× 10^{-32} C^2/cm^2)	AF	f_c (Hz)
PMOS device – S/N #3								
Pre-Rad	-0.937	8.813	0.6	37.5	137.0	6.450	1.03	21.7
Post-Rad	-0.947	8.750	1.9	37.5	170.0	10.21	1.05	28.5
NMOS device – S/N #4								
Pre-Rad	0.764	8.750	1.3	41.0	265.0	28.65	1.05	55.0
Post-Rad	0.771	8.750	5.0	41.0	350.0	50.50	1.10	49.0

5. MICROPOWER PREAMPLIFIER PERFORMANCE FOLLOWING PROTON IRRADIATION

Figure 3 shows the schematic of the micropower, differential input voltage preamplifier [9, 10]. Large area PMOS input pair devices (*M1* and *M2*) are used for low input-referred flicker noise voltage, and these devices are operated in moderate inversion for high transconductance efficiency (g_m/I_D) and high transconductance for low white noise. *M1* and *M2* are connected to folded cascode devices *M10* and *M11* with a PMOS active load provided by *M14* and *M15*. Source follower *M16* provides output buffering to drive off-chip or resistive load and can be omitted for on-chip capacitive loads. *M3* and *M4* are resistively degenerated current sources utilizing *M7* and *M8* operating in the deep-ohmic region as degeneration resistors. Current source degeneration is used to reduce the otherwise high NMOS flicker noise contributions of *M3* and *M4*.

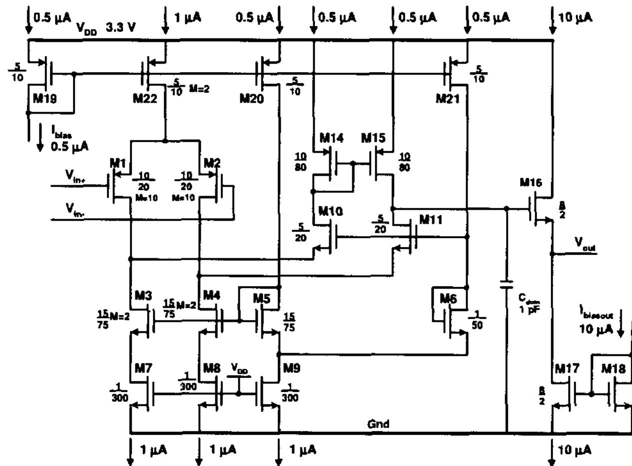

Figure 3. Schematic diagram of the micropower, differential input voltage preamplifier.

Figure 4 shows the measured input-referred, noise voltage density for three samples of the preamplifier. One was not irradiated, another irradiated under bias, and one was irradiated without bias with all terminals grounded. The measured noise at 1 Hz is 250, 305, and 340 $nV/Hz^{1/2}$ for the three samples respectively, indicating an increase in flicker noise voltage of 22% for the irradiated-under-bias sample compared to the non-irradiated sample. The measured 67 $nV/Hz^{1/2}$ white noise, however, is essentially unchanged following irradiation as it is for the test devices. While the irradiated and non-irradiated noise levels are not directly comparable since they are from different samples, the preamplifier flicker noise voltage increase of 22% is almost identical to the 24% increase observed for the PMOS test sample following irradiation. This suggests the preamplifier noise voltage does increase in the 22 – 24% range following irradiation since preamplifier noise is dominated by the input PMOS devices. Flicker noise voltage for the unbiased irradiated preamplifier sample increased 36% above that of the non-irradiated

sample. This suggests that radiation damage might actually be worse if preamplifiers were powered down compared to being under normal bias.

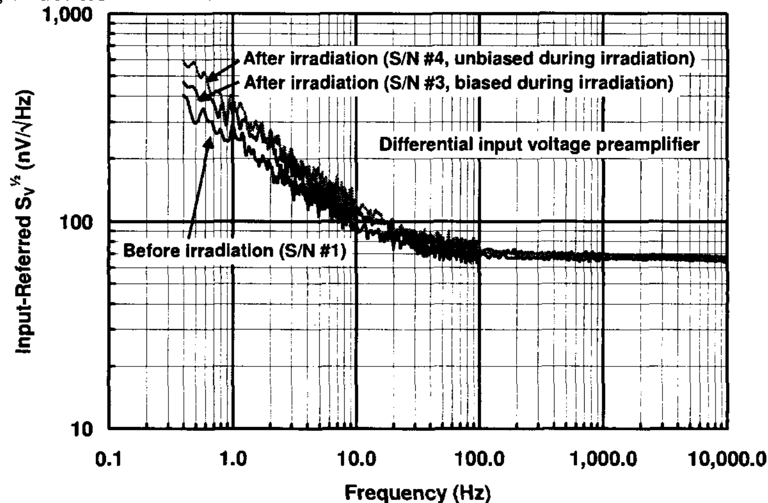

Figure 4. Measured input-referred noise voltage density of preamplifier before and after irradiation.

6. CONCLUSION

Measured flicker noise voltage increases 22, 24, and 36% for a 0.35-μm partially depleted SOI micropower preamplifier, PMOS device, and NMOS device respectively following irradiation by 63.3 MeV protons to a total dose of 1 Mrad (Si). The preamplifier flicker noise increase closely tracks the PMOS device noise increase as expected since preamplifier noise is dominated by PMOS input devices. Transconductance, white noise, and gate-source voltage were essentially unaffected by the irradiation, while MOS output conductance, difficult to measure for these long-channel devices, appeared to increase. Flicker noise, important for processing sensors like gyros having low frequency outputs, can be hardened by sufficient over-design in the pre-irradiation design. This can be done by increasing the area of the MOS devices. Irradiation above 1 Mrad (Si) may be planned to evaluate flicker noise and output conductance, which usually affects open-loop gains, for higher levels of hardness.

REFERENCES

[1] D. M. Fleetwood, T. L. Meisenheimer, and J. H. Scofield, "1/f Noise and Radiation Effects in MOS Devices," *IEEE Trans on Nuc Sci*, vol. 41, no. 11, pp. 1953 – 1964, Nov. 1994.

[2] H. D. Xiong, D. M. Fleetwood, B. K. Choi, and A. L. Sternberg, "Temperature Dependence and Irradiation Response of 1/f-Noise in MOSFETs," *IEEE Trans on Nuc Sci*, vol. 49, no. 6, pp. 2718 – 2723, Dec. 2002.

[3] F. Faccio, P. Aspell, E. H. M. Heijne, and P. Jarron, "Analog Performance of SOI MOSFETs up to 25 Mrad (Si)," *Third Eur Conf on Rad and its Eff on Comps and Sys*, pp. 137 – 141, Sept. 1995.

[4] G. Anelli, F. Faccio, S. Florian, and P. Jarron, "Noise Characterization of a 0.25 μm CMOS Technology for the LHC Experiments," *Nuc Inst and Meth in Phy Res A*, 457, pp. 361 – 368, 2001.

[5] S. T. Liu, W. C. Jenkins, and H. L. Hughes, "Total Dose Radiation Hard 0.35-μm SOI CMOS Technology," *IEEE Trans on Nuc Sci*, vol. 45, no. 6, pp. 2442 - 2449, Dec. 1998.

[6] S. T. Liu, S. Balster, S. Sinha, and W. C. Jenkins, "Worst Case Total Dose Radiation Response of 0.35 μm SOI CMOSFETs," *IEEE Trans on Nuc Sci*, vol. 46, no. 6, pp. 1817 - 1823, Dec. 1999.

[7] W. C Jenkins, and S. T. Liu, "Total Dose Performance at 77 K of a Radiation Hard 0.35 μm CMOS SOI Technology," *IEEE IEEE Trans on Nuc Sci*, vol. 47, no. 6, pp. 2204 - 2207, Dec. 2000.

[8] Y. Li, G. Niu, J. D. Cressler, J. Patel, P. W. Marshall, H. S. Kim, S. T. Liu, R. A. Reed, and M. J. Palmer, "Proton Radiation Effects in 0.35-μm Partially-Depleted SOI MOSFETs Fabricated on UNIBOND," *IEEE Trans on Nuc Sci*, vol. 49, no. 6, pp. 2930-2936, Dec. 2002.

[9] D. M. Binkley, D. H. Ihme, C. E. Hopper, B. J. Blalock, and M. M. Mojarradi, "Design of Micropower, Low-Noise, SOI CMOS Preamplifiers for Deep Space Environments," *2003 15th Biennial Uniy/Govt/Ind Micro Symp*, June 2003.

[10] D. M. Binkley, C. E. Hopper, B. J. Blalock, M. M. Mojarradi, J.D. Cressler, and L. K. Yong, "Noise Performance of 0.35-μm SOI CMOS Devices and Micropower Preamplifier from 77 – 400 K," *2004 IEEE AeroConf.* 2003.