

A Digital Beamforming Processor for the Joint DoD/NASA Space Based Radar Mission

Mark A. Fischman, Charles Le, and Paul A. Rosen
Jet Propulsion Laboratory, California Institute of Technology
Radar Science and Engineering Section
M/S 300-241, 4800 Oak Grove Dr.
Pasadena, CA 91109-8099 USA

Abstract—The Space Based Radar (SBR) program includes a joint technology demonstration between NASA and the Air Force to design a low-earth orbiting, 2×50 m L-band (1.26 GHz) radar system for both Earth science and intelligence-related observations. A key subsystem aboard SBR is the electronically-steerable digital beamformer (DBF) network that interfaces between 32 smaller sub-antenna panels in the array and the on-board processing electronics for Synthetic Aperture Radar (SAR) and Moving Target Indication (MTI). In this paper, we describe the development of a field-programmable gate array (FPGA) based DBF processor for handling the algorithmically simple yet computationally intensive inner-product operations for wideband, coherent beamforming across the 50 m length of the array. The core functions of the DBF—the CORDIC (Coordinate Rotation Digital Computer) phase shifters and combiners—have been designed in the Verilog hardware description language and implemented onto a high-density Xilinx Virtex II FPGA. The design takes full advantage of the massively parallel architecture of the Virtex II logic slices to achieve real-time processing at an input data rate of 25.6 Gbit/s. Tests with an antenna array simulator demonstrate that the beamformer performance metrics (0.07° rms phase precision per channel, -39.0 dB peak sidelobe level) will meet the system-level requirements for SAR and MTI operating modes.

I. INTRODUCTION

Research groups from NASA and the Air Force are currently collaborating on the design of a very large aperture, 2×50 m L-band Space Based Radar (SBR) as a joint technology demonstration for Earth science and defense-related applications. The SBR baseline mission requirements call for a low-earth orbiting, electronically-steerable phased-array radar at a 1.26 GHz operating frequency, with dual processing modes for both Interferometric Synthetic Aperture Radar (InSAR) and Space-Time Adaptive Processing (STAP) / Moving Target Indication (MTI). In terms of Earth science goals, the capability to make global SAR and InSAR observations at L-band frequencies would enable centimeter-precision geodetic imaging (for land surface topography and earthquake hazard forecasting) and measurements of other parameters that are crucial to understanding the Earth's water cycle and energy balance (soil moisture, vegetation height and biomass, sea ice velocity and thickness) [1], [2]. For defense and military intelligence applications, an L-band STAP radar with a large power-aperture product offers the capability to detect enemy threats in the air or on the ground through foliage, during the

day or night, regardless of the weather condition [3].

A key subsystem in SBR is the beamforming network that interfaces between 32 smaller sub-antenna panels (each 1.56×2 m) and the SAR and STAP on-board processing electronics. In missions that preceded SBR such as the Spaceborne Imaging Radar-C/X-band Synthetic Aperture Radar (SIR-C/X-SAR) flown in 1994 [4] and the Shuttle Radar Topography Mapper (SRTM) flown in 2000 [5], beamforming was carried out in the RF electronics using a corporate-fed microwave combiner circuit that extended over the entire antenna length. RF combining was a suitable technology for these past radar missions because the antenna apertures were smaller (≤ 12 m), the system bandwidth was relatively low (≤ 20 MHz), and the radars were mainly operated in a fixed-azimuth (boresight) steering mode. For SBR, however, there are a number of new technical challenges in forming the beams: the antenna spans 50 m and will require long lengths of distributed cabling; also due to the large structure size, the radar is more susceptible to thermal gradients in orbit which can impact phase stability; the radar beam must be steerable away from the boresight direction; and a system bandwidth up to $B=80$ MHz is required for some SAR modes. The central challenge becomes how to combine the wideband radar echoes from each antenna panel while maintaining phase stability and signal coherence across the length of the array.

In this paper, we present the development of a highly phase-stable digital beamformer (DBF) system for SBR, facilitated by field-programmable gate array (FPGA) technology. The DBF concept is to move the analog-to-digital conversion stage of the radar receiver further up in the signal chain—in the case of SBR, to the antenna panel level. Multiple digitized phase-center data from the 32 panels are then sent via high-speed fiber-optic links to a centralized, FPGA-based DBF processor, where the beam steering operations are performed in digital electronics. A time-domain processing technique is used in the FPGA design to achieve real-time operation and to form multiple simultaneous beams required in joint-domain localized algorithms for STAP.

II. BEAMFORMING APPROACH

A functional diagram of the SBR beamforming system is shown in Fig. 1. The DBF must phase rotate and coherently

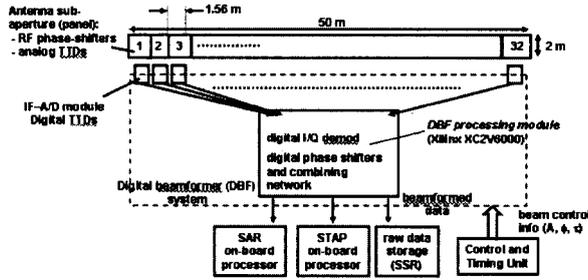


Fig. 1. Functional diagram of the Space Based Radar's digital beamformer (DBF) system.

sum the return signals from all elements of the array at azimuth scan angles up to $\pm 28^\circ$ in spotlight SAR mode or $\pm 45^\circ$ in MTI modes. Because of the large array size and wideband operation, phase-shifters at each transmit/receive (T/R) module are not by themselves sufficient for achieving correlation between antenna panels. Instead, a hybrid approach with true time delay (TTD) devices is used which comprises the following components: 1) 6-bit RF phase shifters at each of the 12×12 antenna elements in a panel, 2) microwave analog TTDs integrated into each panel, with a fine time step resolution of $t_d = 0.25$ ns, 3) digital TTDs which are effected in first-in/first-out memory after each panel's A/D conversion stage, with a coarse time resolution of 5 ns (200 MHz A/D sampling), and 4) digital phase shift correction on the 32 data channels arriving at the DBF processor.

The detailed electrical interface between the DBF, antenna/receiver array, and on-board processor (OBP) is shown in Fig. 2. The received radar signals from the 32 antenna panels in the array are each A/D converted at 8-bit resolution in SAR modes and 12-bit resolution in MTI modes, decimated to a sampling rate of ≤ 100 MHz, and sent via an OC-48 fiber optic link to 32 input ports of the DBF. This yields a maximum input data rate of 25.6 Gbps (800 Mbps per channel). Steering vector data from the radar's beam controller subsystem is sent to the DBF processor to define the amount of phase-shift to apply to steer the receive beam pattern in azimuth. Phase-correction information is also sent to the DBF from the Metrology/Calibration Processor to compensate for errors due to mechanical and electrical length variations in the 32 phase-centers of the array. As part of the technology demonstration for SBR, the raw data channels will also be stored to a solid-state recorder to later verify the correct operation of the SAR and STAP on-board processors.

The performance drivers for the TTDs and phase-shifters aboard SBR are set by the radar's sidelobe level (SLL) requirements in azimuth. Table I summarizes the key requirements and system parameters for carrying out coherent beamforming aboard SBR. The fine (analog) adjustments in each TTD are made at each panel by switching between various lengths of sinuous microwave stripline before the RF-to-IF downconversion and A/D converter stages. The minimum time step resolution, t_d , is therefore limited by the switching losses in this stripline

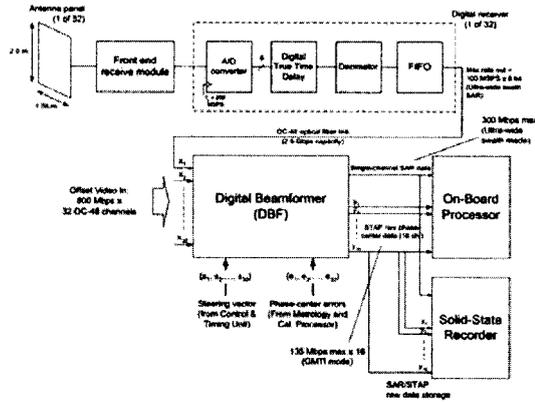


Fig. 2. The Digital Beamformer (DBF) interface and data flow.

parameter	SAR	MTI
Peak antenna sidelobes	-13 dB	-35 dB
Mean antenna sidelobes	-20 dB	-50 dB
Bandwidth B	45-80 MHz	3-10 MHz
Maximum azimuth scan range θ_{az}	$\pm 28^\circ$	$\pm 45^\circ$
Analog TTD adjustment range	≥ 7 ns	
TTD net resolution t_d	≤ 1 ns	

Table I. Key requirements and system parameters for the SBR digital beamformer.

circuit.

Qualitatively, the effect of having less than 100% true time delay adjustment in the array is that there will be a loss of coherence for signal frequency components further from the passband center frequency, $f_0 = 1.26$ GHz. For example, consider the case in which two adjacent antenna panels receive a 3-tone signal having bandwidth B and a remaining time lag t_d . The received signal at panel 1 is

$$x_1(t) = a_0 e^{j2\pi(f_0 - B/2)t} + a_1 e^{j2\pi f_0 t} + a_2 e^{j2\pi(f_0 + B/2)t}, \quad (1)$$

and the signal at the adjacent panel 2 is

$$x_2(t) = a_0 e^{j2\pi(f_0 - B/2)(t-t_d)} + a_1 e^{j2\pi f_0 (t-t_d)} + a_2 e^{j2\pi(f_0 + B/2)(t-t_d)}. \quad (2)$$

The DBF processor then compensates for the remaining time delay in signal x_2 by applying a phase shift of $\phi_d = 2\pi f_0 t_d$. The combined signal between panels is then

$$\sum_n x_n(t) = x_1(t) + e^{j\phi_d} x_2(t) = (1 + e^{j\pi B t_d}) a_0 e^{j2\pi(f_0 - B/2)t} + 2a_1 e^{j2\pi f_0 t} + (1 + e^{-j\pi B t_d}) a_2 e^{j2\pi(f_0 + B/2)t} \quad (3)$$

For the finite bandwidth echo, the phase shift operation therefore causes some dispersion in the panel 2 signal, which leads to a loss of power (coherence loss) at the band edges $f_0 \pm B/2$ of the combined signal:

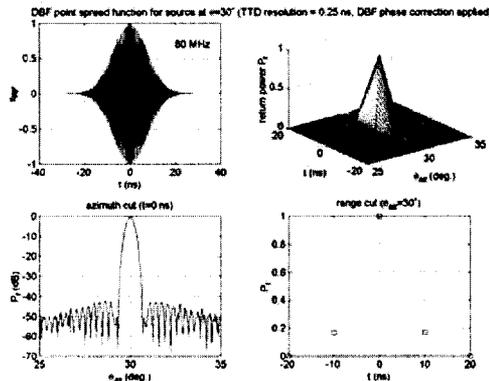


Fig. 3. DBF point-target response for a source at 30° azimuth (TTD resolution = 0.25 ns). From top left to bottom right: the wideband RF return signal; point-target response in azimuth and range; azimuth cut of the response; and range cut of the response.

$$CL \text{ (coherence loss)} = \left| \frac{a_0(1 + e^{j\pi B t_d})}{2a_0} \right|^2 \quad (4)$$

$$= 10 \log_{10} \left[\frac{1 + \cos(\pi B t_d)}{2} \right] \text{ [dB]}$$

From (4), the time-bandwidth product Bt_d must be kept small ($\ll 1$) in order to minimize the coherence loss. For example, in the case of a full bandwidth 80 MHz return echo and the nominal time resolution of $t_d = 0.25$ ns, there is only a 3.6° error ($\pi B t_d$ radians) in the DBF's phase shift operation at the band edges. The resulting coherence loss is negligible (< 0.01 dB). Losses become more noticeable (a tenth of a dB or more) for $t_d > 1$ ns, and rapidly deteriorate once the TTD resolution approaches the scale of the digital sampling interval (5 ns).

Numerical floating-point simulations of the hybrid time-delay/phase-shift system have been developed in the MATLAB programming language to confirm the beamformer performance. The DBF output is expressed as

$$y(t) = \sum_{n=0}^{N-1} w_n x_n(t), \quad (5)$$

where $w_n = \exp(-j2\pi f_0 t_{dn})$ represents the steering vector that imparts the final phase correction and x_n represents the received channels from $N = 32$ antenna panels. The radar's response to a point target was solved in both azimuth (space) and range (time) dimensions for an 80 MHz echo. The detected RF signals are modeled as short-pulse Gaussian waveforms having a 3 dB width of $1/B$:

$$x_{RF}(t) = e^{-\ln 4 \cdot (Bt)^2} \cos(2\pi f_0 t). \quad (6)$$

A point source is located at $\theta_{az} = 30^\circ$ in azimuth to approximate the maximum scan angle in spotlight SAR

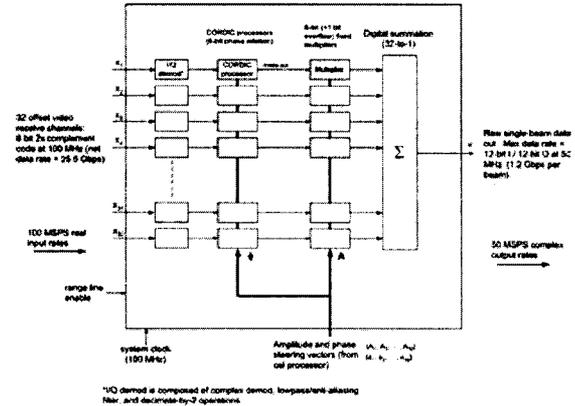


Fig. 4. System level diagram of the DBF processor. (This implementation is shown for the spotlight SAR mode only.)

mode. For the array taper, a Hamming amplitude distribution is applied across the 32 panels to reduce sidelobes.

Fig. 3 shows the point spread function of the beamformer for $t_d = 0.25$ ns. Shown are (a) the RF return waveform, (b) impulse response in both azimuth and range dimensions, (c) azimuth cut of the response, and (d) range cut showing the power detected samples at $\theta = 30^\circ$. The data show that the beamformer exhibits low sidelobes of -42 dB in the azimuth plane, and that there is virtually no loss of coherence in the power detected sample at $t = 0$ ns in range (center of pulse). This performance satisfies the most stringent peak SLL requirement of -35 dB for MTI radar modes. It follows that a TTD time resolution of 0.25 ns is adequate for maintaining phase coherence across the array panels at up to 80 MHz bandwidth.

III. DBF PROCESSOR DESIGN AND SIMULATION

A. CORDIC Digital Phase-Shifter Technique

The main components of the DBF processor are illustrated in Fig. 4. Each of the 32 processor channels contains a digital I/Q demodulator, a digital phase-shifter, and an amplitude scaling module. After phase rotation and scaling, the 32 sub-channels are added together in a digital combiner network to generate either a single receive beam for SAR or multiple simultaneous beams (a primary beam plus several neighboring auxiliary beams) for STAP/Joint Domain Localized processing. The beamforming operation described in (5) has a total equivalent processing performance of 26×10^9 op/s for real-time, simultaneous SAR and MTI processing.

One of the key design aspects for achieving highly precise phase-shift computations in real-time is use of the CORDIC (Coordinate Rotation Digital Computer) technique [6], [7]. In CORDIC, the phase shift operation is carried out through a series of M smaller rotation stages at particular arctangent intervals, i.e., in phase shift intervals

$$\phi_m = \pm \tan^{-1}(1/2^m), \quad m = 0, \dots, M. \quad (7)$$

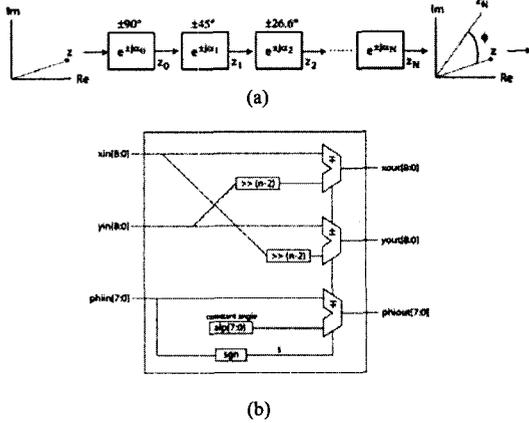


Fig. 5. (a) CORDIC phase shift technique and (b) module implementation onto an FPGA.

The sign of each ϕ_m value is chosen so that the net rotation (the sum of all ϕ_m angles) approaches the desired phase shift angle ϕ :

$$\phi = \sum_{m=0}^M \phi_m. \quad (8)$$

The phase precision can therefore be improved by increasing the number of iterations M . The choice of rotation angles in (7) is understood by looking at the math expression after each iteration. If z_m represents the complex output of the m^{th} CORDIC stage and $z_{m-1} = x_{m-1} + jy_{m-1}$ represents the complex input of that stage, then

$$z_m = z_{m-1} e^{\pm j \tan^{-1}(2^{-m})} = \frac{1}{\sqrt{1+2^{-2m}}} \left[(x_{m-1} \mp 2^{-m} y_{m-1}) + j(y_{m-1} \pm 2^{-m} x_{m-1}) \right]. \quad (9)$$

From (9), the rotation in arctangent intervals can be accomplished with just a series of adders and subtractors and with binary right-shift (divide-by- 2^m) operators, which are straightforward to implement in digital logic.

By reducing trigonometric functions into a set of simple math operations, the CORDIC algorithm is well suited for a high-throughput FPGA design. Fig. 5 shows the signal flow and implementation for the CORDIC phase shifter. The sequence of phase rotations can be implemented in the FPGA as a systolic digital process, where a series of repetitive logic functions are pipelined together. The simple math operations in each systolic cell make it possible to synthesize FPGA logic that can meet the throughput timing constraints of the DBF.

A fixed-point (bit-true) CORDIC phase shifter module and testbench were designed in the Simulink language to study the effects of finite bit precision. The testbench generates input test vectors (1000 randomly distributed complex samples and phasor arguments) for both the CORDIC device under test and for an ideal, floating-point

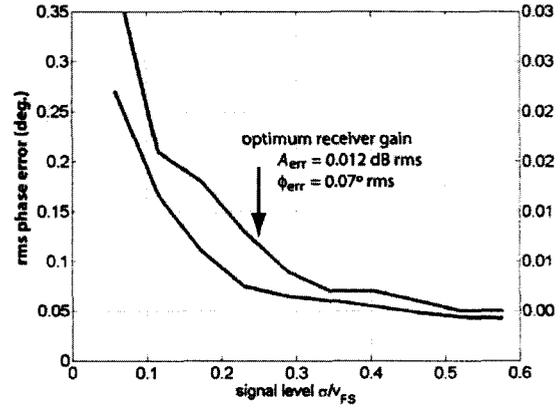


Fig. 6. Amplitude and phase precision simulation results for the 15-bit / 15-stage CORDIC phase-shifter. The root-mean-square errors are plotted as a function of the input signal level (normalized to full scale).

phase shifter. The amplitude and phase error statistics could then be calculated from the difference between the ideal and fixed-point output vectors.

After experimenting with various bit widths for the CORDIC's x , y , and ϕ registers, it was found that a 15 stage CORDIC with a 15 bit register width (8 bit A/D integer data + 6 fractional bits + 1 overflow bit) yielded sufficient precision for meeting the antenna sidelobe requirements [shown in the following section]. The fixed-point simulation results for the 15-bit CORDIC design are plotted in Fig. 6. This graph shows the rms phase and amplitude errors for the CORDIC output as a function of the normalized input signal level, σ/v_{FS} , where σ is the standard deviation and v_{FS} is the full scale value of the digitized input signal. Of special importance in conventional SAR processing is the return level $\sigma = 1/4 v_{FS}$, because this is the optimum point for the signal-to-noise plus distortion ratio (i.e., the digital processor is neither limited by quantization noise nor by saturation). At this signal strength, the CORDIC module performed with rms amplitude and phase precisions of 0.012 dB and 0.07°, respectively.

B. Antenna Array Simulator

To link the bit-true CORDIC performance to the actual sidelobe level performance of the beamformer, an SBR antenna array simulator named *channelSim* was developed in MATLAB. *channelSim* generates the 32 wideband digital output channels from the panel radar electronics modules in the 50 m array. These output vectors are then connected to the fixed-point device under test—a bank of 32×15 -bit CORDIC phase-shift modules designed in Simulink. The simulator generates the full bandwidth radar return signals received and combined over 12 azimuth antenna elements per panel for the case of a point target located at θ_{az} . As in the coherence loss tests, a target location of $\theta_{az} = 30^\circ$ and a bandwidth of $B=80$ MHz were chosen to emulate the digital beamforming in spotlight SAR mode, which is considered the most stringent condition for preserving coherence

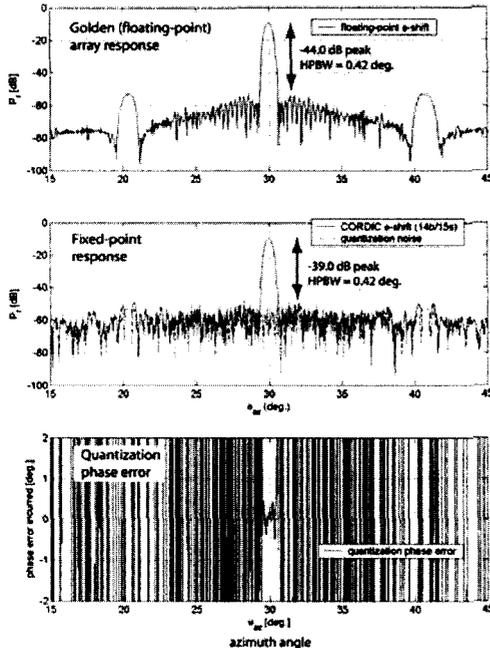


Fig. 7. Ideal (floating-point) and bit-true simulations of the DBF sidelobe level performance. The 15-bit CORDIC phase-shifter design yields a peak azimuth SLL of -39.0 dB and a quantization phase error of 0.3° at the center of target.

because it uses both a wide bandwidth and a wide scan angle. Other modeling assumptions and conditions in *channelSim* include:

- A simplified antenna panel model with no phase-wrapping errors (perfect TTD adjustment within each panel).
- No electrical or mechanical distortion across the array.
- Up to 0.25 ns TTD resolution error between panels.
- Taylor amplitude weighting across 32 azimuth channels, uniform amplitude illumination within each panel.
- 8-bit maximum quantization from each panel's electronics module output.
- Receiver gain set to the optimum level ($\sigma = \frac{1}{4}$ full scale).

Simulations of the bit-true DBF processor were run to test the peak and mean sidelobe level performance in the presence of quantization errors. Fig. 7 shows the some of the array pattern results. The peak SLL using the 15-bit CORDIC implementation is -39.0 dB below the main lobe, thus meeting the most stringent requirement of -35 dB in MTI modes. (By comparison, this performance is within 5 dB of the -44.0 dB peak SLL for the ideal floating-point model of the DBF.) A comparison between the golden and fixed-point DBF performance also reveals that the grating lobes near 20° and 40°, which arise from the uniform illumination on each panel, are masked out by the quantization noise floor in the bit-true implementation. The implication for the antenna design is that it is suitable (and preferable for simplifying the antenna electronics) to use a uniform amplitude gain rather than a taper across the T/R elements within each panel. Bit-true testing of the

beamformed pattern over the entire azimuth plane ($-90^\circ \leq \theta_{az} \leq +90^\circ$) resulted in an equivalent mean hemispheric SLL of -65.2 dB, which satisfies the -50 dB worst case requirement for SBR.

IV. FPGA IMPLEMENTATION

The 6 million gate Xilinx Virtex II FPGA (XC2V6000) has been chosen as the processing platform for implementing the DBF algorithms. The advantages of this particular FPGA are its high logic density, large number of I/O ports, and reconfigurable SRAM-based technology which eases development time and cost. Although it is not a requirement to fit all beamforming operations onto a single FPGA chip, logic area savings is an obvious goal for reducing the overall chip count (for mass, volume, and power savings) and for integrating advanced radar processing features onto the DBF (for example, FFT cores for channel equalization or range compression).

The logic for a single, synchronous 32-to-1 DBF combiner has been designed and implemented at the register transfer level in the Verilog hardware description language. As part of the design flow, a suite of software tools have been used, including Xilinx XST (for logic synthesis) and ModelSim (for functional Verilog simulations). An important part of the hardware verification is also to confirm, bit-for-bit, a perfect match between the fixed-point MATLAB/Simulink models described in Section III and the hardware simulation results in ModelSim. This has been accomplished by transferring test vector data between these two software tools, so that Verilog hardware components such as the CORDIC module can effectively be “dropped” into the Simulink environment as a device-under-test and tested over a large number of data points.

Results from the Xilinx mapping analysis tool show that the current DBF design uses 51% of the available logic slices aboard the XC2V6000. Because multiple combiners will eventually need to be instantiated to support simultaneous, multiple beamforming modes in MTI, the board-level design of the DBF will require more than one Virtex II part. In terms of speed performance, the post place-and-route static timing analysis passed at a maximum clock rate of 56.2 MHz, which gives more than 10% timing margin above the required 50 MHz clock rate for processing complex baseband data.

V. CONCLUSION

A digital beamforming architecture and FPGA-based processor have been developed to enable advanced spaceborne SAR/MTI measurement scenarios in the very large aperture (50 m) L-band Space Based Radar. Recent research efforts at NASA/JPL have involved DBF algorithm development, fixed-point modeling, and digital hardware implementation (hardware description language coding, synthesis, and testing), which have led to the delivery of working FPGA firmware that meets SBR's baseline requirements for phase precision and antenna sidelobe level

response. The DBF processor and its related technologies—modular antenna design, digital RF receivers, and fiber-optic data distribution—will have important implications for improving the overall phase-stability and calibration of large aperture radar systems like SBR.

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REFERENCES

- [1] P. A. Rosen, S. Hensley, I. R. Joughin, F. K. Li, S. N. Madsen, E. Rodriguez, and R. M. Goldstein, "Synthetic aperture radar interferometry," *Proc. IEEE*, vol. 88, no. 3, pp. 331-382, Mar. 2000.
- [2] J. T. Booth, D. L. Evans, C. Heeg, Y. Kim, and D. M. Tralli, "A plan for living on a restless planet," *Earth Observ. Magazine*, pp. 14-21, Nov. 2003.
- [3] P. A. Rosen and M. E. Davis, "AFRL/JPL Space-based Radar development 2002-2003 final report," *Report to NASA Earth Science Technology Office*, JPL task plan 80-6881, pp. 11-14, Mar. 2003.
- [4] R. L. Jordan, B. L. Huneycutt, and M. Werner, "The SIR-C/X-SAR synthetic aperture radar system," *IEEE Trans. Geosci. Remote Sensing*, vol. 33, no. 4, pp. 829-839, July 1995.
- [5] D. L. Evans and A. Freeman, "Beyond SIR-C/X-SAR," *Proc. IEEE Aero. Applications Conference*, vol. 2, pp. 49-55, Feb. 1996.
- [6] J. E. Volder, "The CORDIC trigonometric computing technique," *IRE Trans. Elec. Computers*, pp. 330-334, Sept. 1959.
- [7] R. Andraka, "A survey of CORDIC algorithms for FPGA based computers," *Proc. 1998 ACM/SIGDA symp. field programmable gate arrays*, pp. 191-200, Monterey, CA, Feb. 1998.