

VIBRATION BEHAVIOR OF CSP ASSEMBLIES WITH AND WITHOUT UNDERFILL

Reza Ghaffarian, Ph.D.
Jet Propulsion Laboratory, California Institute of Technology
Pasadena, California
818-354-2059, Reza.Ghaffarian@jpl.nasa.gov
Namsoo P. Kim, Ph.D., Karen Coates
The Boeing Company

ABSTRACT

The test results for numerous chip scale package assembly performed under MicrotypeBGA Consortium led by the Jet Propulsion Laboratory have been published previously. Cycles-to-failures (CTFs) of assemblies with underfill to 3,000 cycles of -30 to 100°C and 1500 in the range of -55 to 125°C are presented. The virgin of these assemblies with numerous chip scale packages and a control TSOP were also subjected to two vibration levels for upto 6 hours to characterize their times-to-failures (TTFs). Assemblies with and without underfill were tested. This paper presents vibration behavior of these assemblies along with optical and SEM cross-sectional micrographs taken after failures.

Key words: Vibration, CSP, microBGA, TSOP, underfill, solder joint reliability, thermal cycle

INTRODUCTION

Although the expression "CSP" (chip scale package) is widely used by both suppliers and users, its definition has evolved as the technology has matured. When introduced to the market, a very precise definition was adopted by a group of industry experts. CSP was defined as a package that is up to 1.2 or 1.5 times larger than the perimeter or the area of the die. Soon, it became apparent that suppliers were using the term CSP to promote a miniature version of a previous package, namely, the ball grid array (BGA).

A rapid transition to a much lower size was difficult both for package suppliers and end users. Suppliers had difficulty in building such packages and users had difficulties in accommodating the need for the new microvia printed wiring board (PWB), chiefly, because of routing requirements and increased cost. Other issues for accepting the "interim definition" by industry included needed maturity in assembly and infrastructure. For example, the use of pitches other than 0.5 mm, including 0.75 and 0.65, was aimed at using a standard PWB design rather than a microvia in order to avoid the elevated cost of the latter.

Thus, in reality, CSPs are miniature new packages that industry has already implemented, and there are many unresolved technical issues associated with their implementation as they become available. Technical issues themselves also change as packages mature. For example, in early 1997, packages with 1 mm pitch and lower were the dominant CSPs, whereas in early 1998 packages with 0.8 mm and lower became the norm for CSPs. Now, packages with 0.4 mm pitch have become available.

In addition to finer pitch PWB design/assembly challenge, new package configurations including the use of flip chip die rather than wire bonds and stacked die within packages or CSP stack with peripheral attachment will add additional complexity when the package reliability are being developed. New unknown potential failure mechanisms will add to such challenges.

CSPs and newer stack versions have their own unique form factor not seen in SMT and many of them may not be able to meet traditional reliability test requirements for commercial application. Also, because of their wide usage in portable electronics, additional emphasis has been placed on specific new tests such as bend and drop tests to meet reliability requirements for such products. The small form factor with large functionality necessitates use of area array packages with small, rigid balls not having the resistance to thermal and mechanical exposure required for these products[1-4].

However, rapid changes in electronics have reduced thermal cycle life expectancy in favor of CSP implementation. Requirements for dynamic loading, especially for cell phone applications, may be resolved by the use of underfill [5] or corner staking [6] despite knowing their drawbacks of imposing additional costly process steps and introducing reworkability in most cases. Limited test results become available on vibration behavior of BGAs [7,8], but data are scarce for vibration performance of CSP, especially for high reliability applications.

Purpose of This Paper

Underfill has been widely used to improve solder joint reliability of area array flip chip die attachments by at least an order of magnitude. Underfill is used both within packages and on the PWB. It acts to absorb the CTE mismatch and consequently reduce stress significantly by distributing it uniformly through the solder joints. Underfilling, however, is undesirable because of the additional process requirements increase cost and reduce manufacturing throughput. Another drawback of underfill is the inability to rework defective parts. Progress has been made to reduce the negative impact of underfilling by shortening the process time through the use of snap cure polymers and enabling reworkability by the development of reworkable underfills.

So, if we assume that underfill improves reliability, then one thought might be that if everything else failed to improve reliability of CSPs, underfilling might be the ultimate undesirable solution. This approach for CSPs was used by Sony when its passport size camera was first introduced in early 1997. Investigators have shown that underfill materials and processes play a key role on the assembly reliability. Literature data on the effects of underfill on assembly reliability is limited, especially for the effect of package types including those modified for relieving stress mismatch between die and substrate.

The effect of underfilling on long-life thermal cycle behavior of various CSPs were presented first. The investigation aimed to answer some of the key questions on the interaction of package type and underfill on thermal cycle behavior. Further work was carried out on the same type of test vehicles to characterize vibration behavior under two levels (7.8 and 16.9 Grms) and three time intervals (2, 4, and 6 hours). The purpose of test was to determine TTFs and understand failure mechanisms of CSPs with and without underfill.

This paper presents CTFs and TTFs for various CSP assemblies with and without underfills. Assemblies were inspected visually and cross-sectioned after test completion using optical and scanning electron microscopy (SEM) to determine crack initiation and propagation. Photomicrographs of these samples were also included.

CSP TEST MATRIX

Test Vehicle (TV)

Eleven packages from 28 to 275 I/Os as listed in Table 1 were used. A photo of an assembled test vehicle with underfill used for vibration testing is shown in Figure 1. The TSOP was used as control and had no underfill. The PWBs were fabricated from FR-4 and BT (bismaleimide triazine) materials (which were available in the resin copper coated form) and a high temperature FR-4. The boards were double sided, standard and microvia. Four

types of surface finishes were considered, the majority were organic solder preservative (OSP)

Solder Paste/Volume

Three types of solder pastes were included:

- no-clean;
- water soluble (WS);
- rosin mildly activated (RMA).

Three stencil thicknesses were included, but the majority of test vehicles used a 6 mil thickness.

TV Features

All packages were daisy-chained, and had up to two internal chain patterns. Packages had different pitches, solder ball volumes and compositions, and daisy-chain patterns. In most cases, these patterns were irregular and much time and effort was required for the PWB design. The test vehicle (TV-1) was 4.5" by 4.5" . .

Underfill

Several assemblies had underfilled packages even though it was known that the packages may not require underfilling. This was done in order to better understand the impact of underfill on solder joint reliability for different CSP styles. Package O required underfill, and of these packages, the majority were underfilled. Several were not underfilled in order to better understand the reliability consequence of not using underfill for this package.

Environmental Testing

The test vehicles were monitored continuously during the thermal cycle and random vibration test for electrical interruptions and opens. The criteria for an open solder joint specified in IPC 9701[9], Table 4-3.3.3, for thermal cycle was used to interpret electrical interruptions for both thermal cycle and vibration. Failures detected by continuous monitoring were verified manually at room temperature (RT) after subsequent removal from thermal cycle chamber or from the random vibration table. For vibration, checking was done at two hour intervals. Details of wiring attachments and monitoring equipment are discussed below.

Vibration Test Set Up and Monitoring

Test set up is shown in Figure 2. The Anatech Event Detector and the lap top computer used to record the electrical data were both plugged into an extension-cord-type power strip with internal surge-suppression. The electrical connection from the Anatech to the TVs was made by soldering 20 gauge wire to the through hole connections on the TVs. The wires and ribbon cable that connected the TVs to the Anatech were shielded with a ground braid (refer to figures 3 and 4).

A jumper wire was soldered from a ground pin on each TV to the ground braid which shielded the wires. This ground braid was also clamped to the ground braid that

ran from the Anatech system ground to earth ground. The shielded wires were hung by a bungee cord from the ceiling in order to distance them from the vibration table which emits strong electromagnetic fields. The Anatech program was not run until the power to the vibration table was turned on. This prevented false failures due to the power surge which occurs when the table is initially powered up.

Manual and Continuous Monitoring

Prior to vibration testing, the resistance for each daisy-chain channel was measured by probing and the results were documented. The resistance was also checked intermittently during testing (when the table was off) to verify failures. At the end of testing, all daisy-chain channels were measured again.

During vibration testing, continuous electrical monitoring was performed using an Anatech event detector which has 200 nanosecond detection limits for opens, where opens are loop resistances of >1000 ohms.

Accelerometer

The control accelerometers were placed on the vibration fixture as shown in Figure 4. Each control accelerometer was attached with a 6-32 fastener, with a force of 10 in-lbs. For each TV, one response accelerometer was placed near the center of the board and another accelerometer was placed near the ceramic package, as shown in figures 3 and 4.

Vibration Mounting Fixture

The shaker table used for this experiment is shown in Figure 2. Two assemblies identified as SN 037 and SN 062, without and with underfill, respectively, were mounted on the shaker table using simple support fixturing (translation is fixed, rotation is not). The simple support fixturing was used, since this was the fixturing used for another program at Boeing in order to be able to directly correlate data. This fixturing was chosen since modeling has shown that using fixed edge boundary conditions results in excessive restraint of curvature/displacement during vibration testing. It was shown analytically that an unreasonably severe acceleration level (>50 Grms) may be needed to initiate failures in leaded components within the desired 3 hour timeframe. A force of 10 ft-lbs was used to tighten the clamps around the TVs.

Vibration Test Profiles

Two assemblies SN 037, without underfill, and SN 062, with underfill, were exposed to 2 hours of random vibration testing at a level of 7.8 Grms, followed by 2 hours at 16.9 Grms. After total of 4 hours of exposure at the two level, the assembly with no underfill (SN 037) was removed for failure analysis. The assembly with underfill (SN 062) was further vibrated at the level of 16.9

Grms for an additional 2 hours. The input profiles are shown in Figures 5 and 6..

Thermal Cycle Profiles

For reference, data gathered under two thermal profiles are also included. The profiles were:

- Cycle A: The cycle A condition ranged from -30° to 100°C and had an increase/decrease heating rate of 2° to $5^{\circ}\text{C}/\text{min}$ and a dwell of about 20 minutes at the high temperature to assure near complete creep of the solder. The duration of each cycle was 82 minutes.
- Cycle B: The cycle B condition ranged from -55° to 125°C , with a very high heating/cooling rate. This cycle represent near thermal shock since it utilized a three region chamber: hot, ambient, and cold. Heating and cooling rates were nonlinear with dwells at the extreme temperatures of about 20 minutes. The total cycle lasted approximately 68 minutes.

THERMAL CYCLEE RESULTS- POSITIVE/NEGATIVE EFFECT OF UNDERFILL

CTFs test results for assemblies with underfill were analyzed and compared to standard assemblies without underfill. Three categories of CSP assemblies with underfill based on their impact on reliability were identified: (1) improvement by underfilling, (2) minimal effect, and (3) degradation due to underfilling.

Table 2, provides a summary of CTFs for the TAB CSP-1 assembly that underfilling had negative effect, i.e. reduced CTFs for underfilled assemblies. This Table includes test results to 3,000 cycles under A condition ($-30/100^{\circ}\text{C}$) and to 1,500 cycles under B condition ($-55/125^{\circ}\text{C}$). Under both cycle conditions, assemblies with underfill showed much lower CTFs than those with no underfill. Assemblies showed no failure to 3,000 under A condition, whereas the assemblies with underfill failed at 996, 1385, 1727, and <2000 cycles. Note that the TAB CSP package decouples the die CTE mismatch by use of a stress dampening elastomeric materials layer and flexible TAB lead interconnects.

Results for a leadless 28 I/O package case with improved CTFs for underfill condition are plotted in Figure ??

As expected, cycles to failure increased as temperature cycling range decreased. CTFs for the B condition ranged from 372 to 546 with an $N_{63.2\%}$ (No) of 465 and an m Weibull value of 7.2. For A condition, it ranged from 641 to 1007 cycles with an $N_{63.2\%}$ of 839 cycles and an m value of 7.5.

Results for test vehicles with underfills are also shown in Figure 6. Under the B thermal cycle condition, underfilled assemblies showed only one failure out of four assemblies at 1374 cycles when the group was subjected

to a total of 1,500 cycles. Under condition A, no failure was observed for the underfilled assemblies to a total of 3,000 cycles. These limited test results clearly indicate significant improvement can be achieved by underfilling for this category of peripheral leadless package.

RANDOM VIBRATION RESULTS

Times-to-Failures

TTFs under random vibration for assemblies with and without underfills are listed in Table 3. Note that the first 2 hours (120 minutes) random vibration were performed at 7.8 Grms. Except for Chip-on-flex with 206 I/Os, all assemblies survived 2 hours at this level of random vibration. TSOP that was used as a control package, was the only one that showed no failure to 6 hours of random vibration, 2 hours at 7.8 and 4 hours at 16.9 Grms. Note that TSOP was not underfilled in both assemblies and both showed no failures. In contrast, wafer level CSP was underfilled on both assemblies and their TTFs were in the same range. This may indicate that dynamic behavior of the two assemblies were similar.

Most non underfilled assemblies were failed within half-an-hour after the random vibration level increased from 7.8 to 16.9 Grms. The one with the longest surviving time was the TAB CSP, 46 I/O package, the one showed negative effect on CTFs with underfilling. In general, underfilled assemblies had higher TTFs and survived a total 3 hours of random vibration; three assemblies showed no failures to a total of 6 hours of random vibration (2 hours at 7.8, 4 hours at 16.9 Grms).

1st, 2nd, 10th Daisy Chain Interruptions

Table 3 lists TTF interruptions observed for the first time as well as 2nd and 10th electrical interruptions. The first interruption is reported as assembly failure as defined by IPC9701 specification and they are listed in Table 3. However, it is apparent that time differences between the first and the tenth interruptions are generally small with a maximum difference of 11.6 minutes. One assembly, chip-on-flex, 206 I/O, showed a significant differences between the first and the 10th electrical interruptions. The first failure occurred after only 18.2 minutes and it took another 163 minutes before the 10th interruption was detected during continuous electrical monitoring.

SEM Microscopy

Scanning Electron Microscopy (SEM) photomicrographs and cross-sectional microscopy for the leadless package, 28 I/O after 4 hours of random vibration at two levels of 7.8 and 16.9 Grms are shown in Figures 7-9. Even though this part failed after 137 minutes, no significant microstructural damages are observed when removed from vibration table and cross-sectioned after 240 minutes. There are however, signs of hair line cracks that visually could be observed only at a relatively high

magnification. It appears that these cracks are induced only on one side of package, pins towards top right corner. From cross-sectional micrographs, fine cracks in solder are apparent under the pin close to body. A crack an angle propagated and angle towards the void formed on top of the via with further initiation away from the via and its extension to the toe. These cracks are different from those generally formed due to thermal cycles that show clear signs of microstructural changes with widening between the crack surfaces.

CONCLUSIONS

- The effects of underfill on thermal cycles-to-failures may be positive, neutral, or negative depending on package types. It improved the reliability of leadless package, was neutral for chip-on-flex, and had negative effects on the TAB CSP reliability.
- All packages with or without underfill survived 2 hours of random vibration at 7.8 Grms and most failed within 4 hours of additional vibration at 16.9 Grms. Underfilling improved resistance to vibration. TSOP with no underfill was the only package that survived 6 hours of vibration.
- Hair line cracks induced by vibration are significantly more difficult to detect visually compare to more pronounced cracks with gross microstructural changes formed by thermal cycling.

ACKNOWLEDGMENTS

The portion of research described in this publication was carried out at the Jet Propulsion Laboratory, California Institute of Technology, under a contract with the National Aeronautics and Space Administration.

We express our special thanks to Boeing ACME team for their support. The authors would like to acknowledge Ken Evans at JPL and the in-kind contributions and cooperative efforts of MicrotypeBGA Consortium team members who supported the build of test vehicle. Special thanks are also extended to package suppliers and board manufacturers as well as other team members who have made contributions to the progress of this program. Sincere thanks to program managers at NASA Electronic Parts and Packaging Program (NEPP) for their continuous support and encouragement.

REFERENCES

1. Fjelstad, J., Ghaffarian, R., Kim, YG., *Chip Scale Packaging for Modern Electronics* (Electrochemical Publications, 2002)
2. Ghaffarian, R., "Chip Scale Package Assembly Reliability", Chapter 23rd in *Area Array Interconnect Handbook* (Kluwer Academic Publishers, edited by Karl Puttlitz, Paul Totta, 2002)

3. Ghaffarian, R., et al. "CSP Consortia Activities: Program Objectives and Status," Surface Mount International Proceedings, August 23-27, 1998, pp. 203-230
4. Ghaffarian, R., "Long-Life Reliability of CSP Assemblies With and Without Underfill" Surface Mount International Proceedings, Sept 22-26, 2002, pp. 332-339
5. Zhang, S., "Enhancement of CSP Mechanical Strength using Underfill or Bonding Material" Assembly Process Exhibition and Conference (APEX) Proceedings, Mar 29, Ap 2, 2003
6. Toleno, B.J., "Processing and Reliability of Corner Bonded CSPs" International Electronics Manufacturing Technology (IEMT) Proceedings, July 16-18, 2003
7. Wong, T.E.; Palmieri, F.W.; Fenger, H.S.; "Under-filled BGA Solder Joint Vibration Fatigue Damage" Thermal and Thermomechanical Phenomena in Electronic Systems Proceedings, 2002. IThERM 2002, Page(s): 961 -966
8. Lee, S.-W.R.; Lui, B.H.W.; "Evaluation of Board Level Reliability of Pb-free PBGA Solder Joints". 8th International Symposium on Advance Packaging Materials Proceedings, 3-6 March 2002, Page(s): 82 - 89
9. IPC 9701,"Performance Test Methods and Qualification Requirements for Surface Mount Solder Attachments". Published by IPC, Association Connecting Electronics Industries

Table 1 CSP Package Configurations Matrix

Package ID	Package Style	Package Size (mm)	Pad Size (mm)	Pitch (mm)	I/O Count	Package Thickness (mm)	Ball Dia (mm)
B	Leadless-1	7 x 13.6	0.35 x 0.7	0.8	28	0.8	-
C	TAB CSP-2	7.43 x 5.80	0.4	0.75	40	0.885	0.3
D	TSOP44	18.61 x 10.36	0.27 x 0.5	0.8	44	1.13	n/a
E	Leadless-2	7 x 12.3	0.30 x 0.75	0.5	46	0.8	n/a
F	TAB CSP-1	7.87 x 5.76	0.4	0.75	46	0.91	0.3
G	Chip on Flex-1 (COF-1)	0.3" x 0.3"	.010 in.	.020 in.	99	1.75	0.3
J	Wire Bond on Flex-1	12.1 x 12.1	0.375	0.8	144	1.4	0.5
K	Wire Bond on Flex-2	12 x 12	0.25	0.5	176	0.5	0.3
M	Chip on Flex-2 (COF-2)	0.5 x 0.5	.010 in.	.020 in.	206	1.75	0.3
N	Ceramic CSP	15 x 15	0.4	0.8	265	0.8	0.5
O	Wafer Level	0.413 x 0.413	.010 in.	.020 in.	275	-	0.3

* All measurements are in mm unless otherwise specified

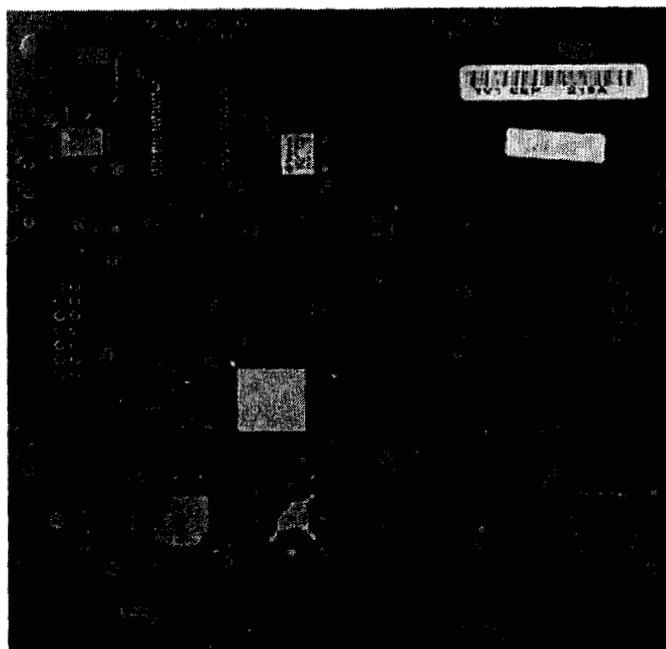


Figure 1 Photograph of the underfilled test vehicle with eleven CSPs, I/Os from 28 to 275, all undefiled except TSOP

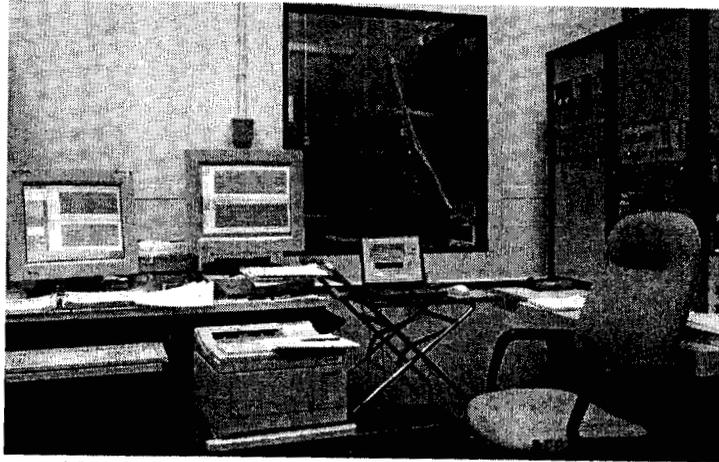


Figure 2 Vibration test set up with electrical monitoring equipment at Boeing facility

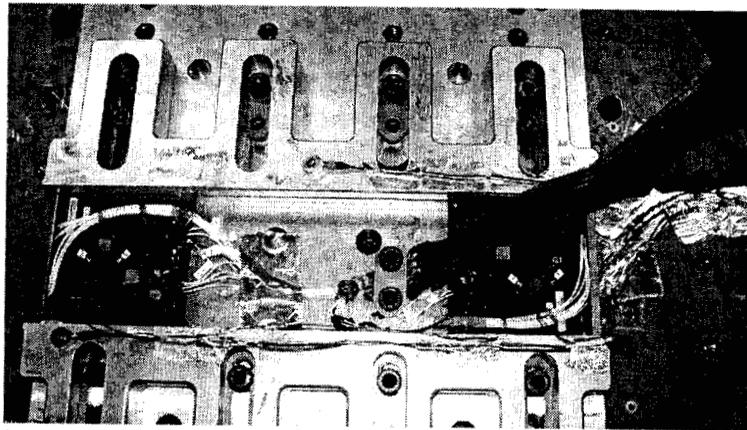


Figure 3 Test vehicles with and without underfill (right), location of accelerometer, and connection to vibration table.

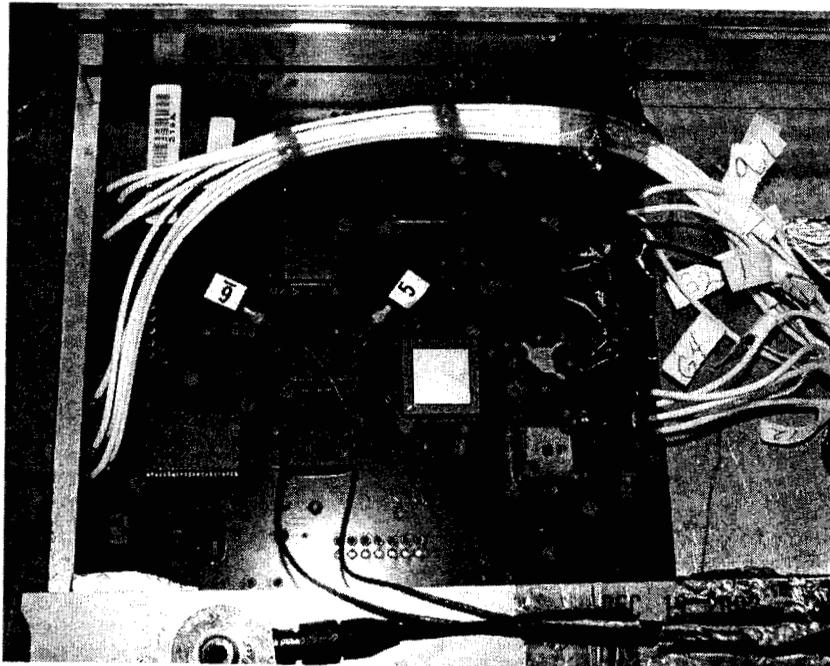


Figure 4 Details of wire connections and location of two accelerometers (near the center)

Figure 5 Random vibration spectrum with 16.9 Grms level that was applied to assemblies for up to 4 hours

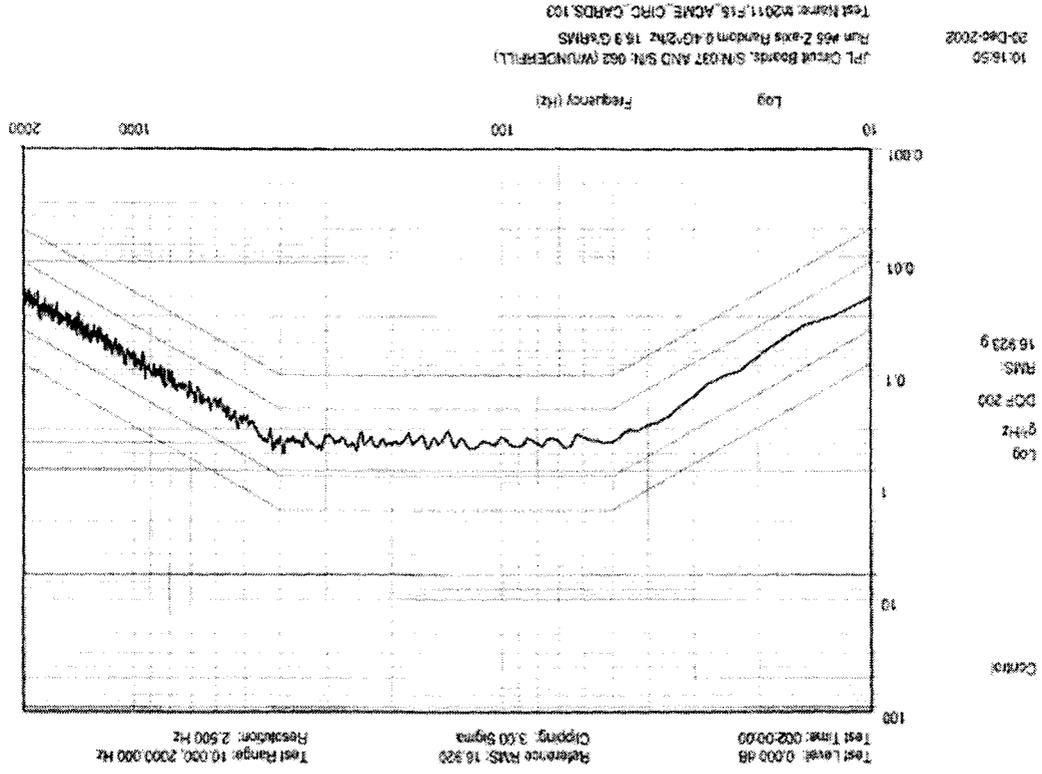
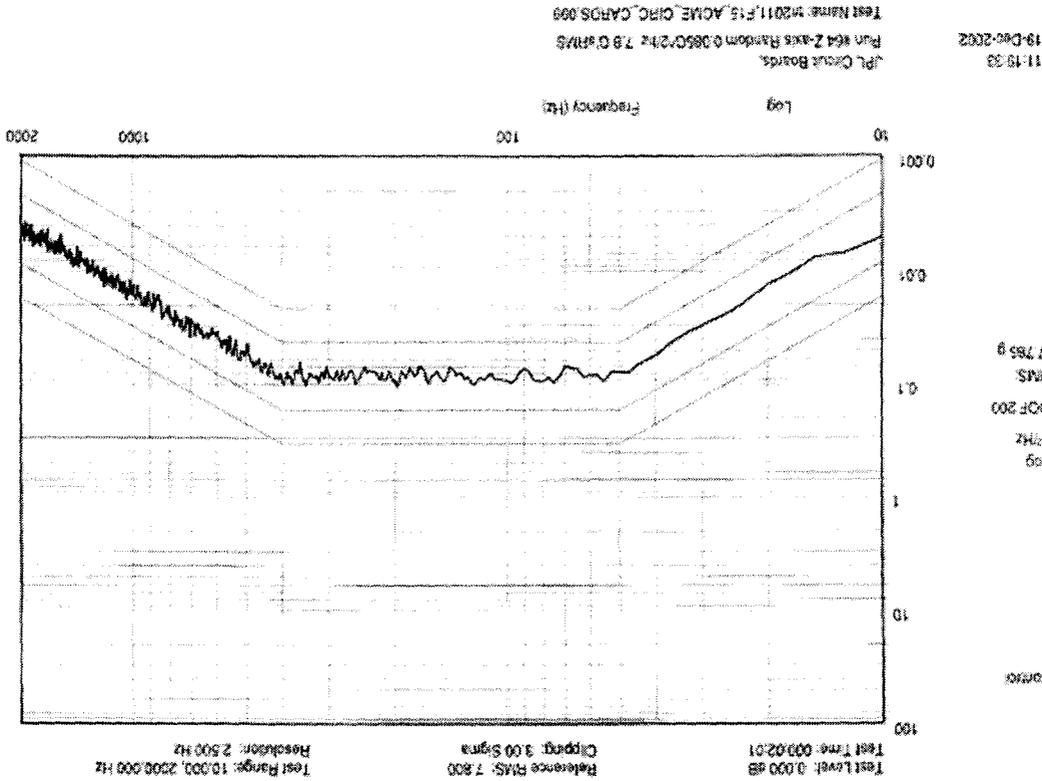
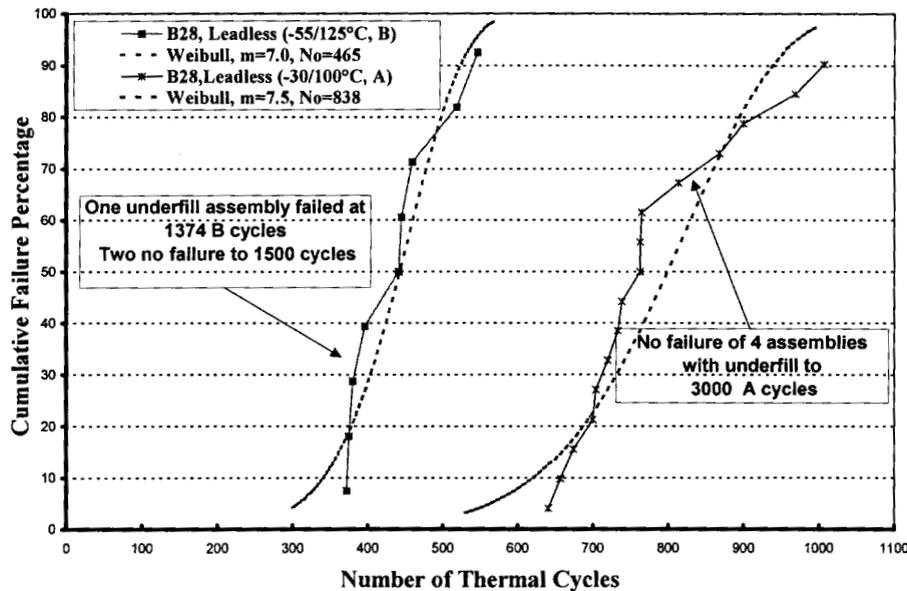


Figure 5 Random Vibration spectrum with 7.8 Grms level and 2 hours of test duration



**Table 2 Comparison of cycles-to-failures for assemblies with and without underfill.
CTFs decrease due to underfilling**

Package & thermal cycle condition	No Underfill Number and cycles to failure	With Underfill Number and cycles to failure
Package F, TAB CSP, -55°C to 125°C, B, 1,500 Cycles	3 out of 10 failure at 709, 896, and 1,380 cycles	3 out of 3 failures at 32 (?), 142, 710 cycles
Package F, TAB CSP-1, -30°C to 100°C, A, 3,000 cycles	No failure (15 assemblies)	4 out of 4 failure at 996, 1385, 1727, and <2000 cycles



**Figure 6 Cycles-to-failures for a 28 I/O leadless package without and with underfill and their Weibull distributions.
CTFs increased for underfilled assemblies**

**Table 3 Random vibration failure times in minutes for assemblies with and without underfill.
Improvement for underfilled assembly**

Package & I/O	No Underfill (SN037) Time in minutes (Total time 4 hours, 2 hours at 7.8 Grms, 2 hour at 16.9 Grms).	With Underfill (SN62) (Total time 6 hours, 2 hours at 7.8, 4 hours at 16.9 Grms)
TSOP, 44 I/O	No Failure (increased resistance, 4 hours, RT)	No Failure
Leadless-1, 28 I/O	136.7	No failure
Leadless-2, 46 I/O	152.9	207.9
TAB CSP-1, 46 I/O	223.1	330.4
TAB CSP-2, 40 I/Os	155.9	207.9
Wire bond on flex-1, 144 I/O	161.6	No Failure
Wire bond on flex-1, 176 I/O	No Part	No Failure
Chip on Flex-1, 99 (I/O)	No Part	No Failure
Chip on Flex-1, 206 (I/O)	No Part	18.2
Ceramic CSP, 265 I/O	136.7	234.4
Wafer Level CSP, 275 I/O	164.7 (underfill)	182

Table 4 Random vibration failure times for the 1st, 2nd, and 10th interruption in daisy chain continuity, 2 hours at 7.8, 2 additional hours at 16.9 Grms for no underfill, and 2 more hours at 16.9 for the underfilled assembly

Package & I/O	Minutes to 1 st interruption No Underfill (Underfil).	Additional Minutes to 2 nd interruption No Underfill (Underfil).	Additional Minutes to 10 th interruption No Underfill (Underfil).
TSOP, 44 I/O	No Failure	No Failure	No Failure
Leadless-1, 28 I/O	136.7 (No failure)	4.5 (NF)	6.1 (NF)
Leadless-2, 46 I/O	152.9 (207.9)	NA(0.1)	NA (1.5)
TAB CSP-1, 46 I/O	223.1 (330.4)	0.3 (3)	11.6 (only 3 interruptions)
TAB CSP-2, 40 I/Os	155.9 (207.9)	0.1 (.1)	1.5 (1.5)
Wire bond on flex-1, 144 I/O	161.6 (No Failure)	0.1 (NF)	1.5 (NF)
Wire bond on flex-1, 176 I/O	No Part (No Failure)	NP (NF)	NP (NF)
Chip on Flex-1, 99 (I/O)	No Part (No Failure)	NP (NF)	NP (NF)
Chip on Flex-1, 206 (I/O)	No Part (18.2)	NP (38.4)	NP (162.9)
Ceramic CSP, 265 I/O	136.7 (234.4)	0.5 (0.1)	2.1 (1.5)
Wafer Level CSP, 275 I/O	164.7 (182)	0.1 (0.1)	2 (1.3)

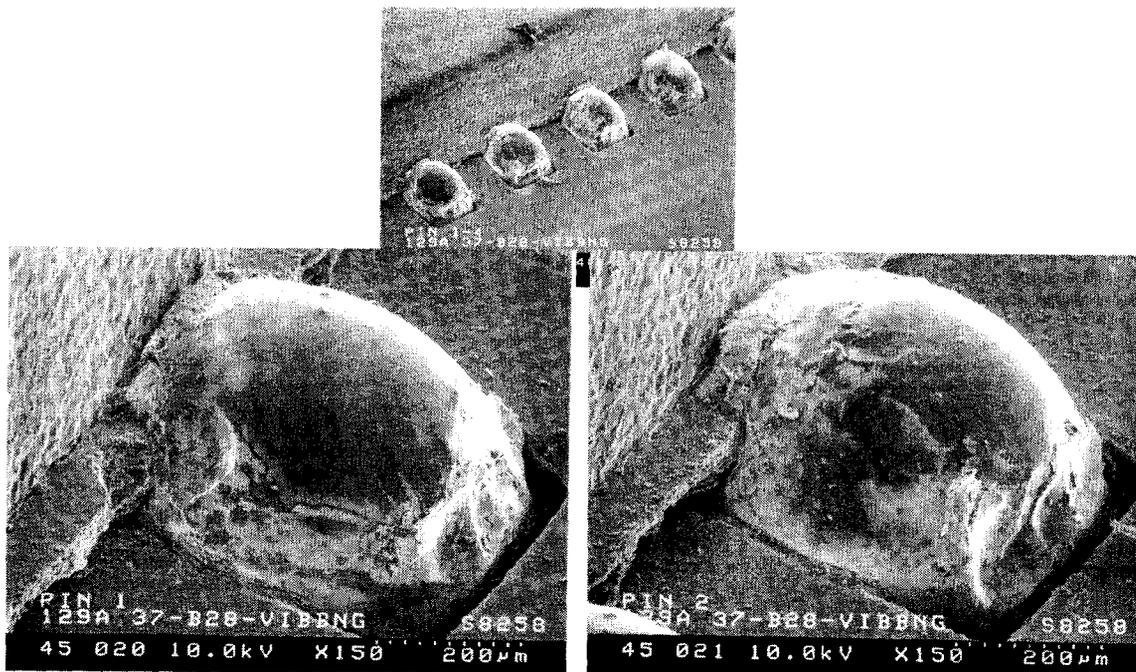


Figure 7 SEM Photo micrograph of pin1-4, top left corner, away from the center of board, after 2 hours at 7.8 Grms and additional 2 hours at 16.9 Grms. No apparent damage due to vibration

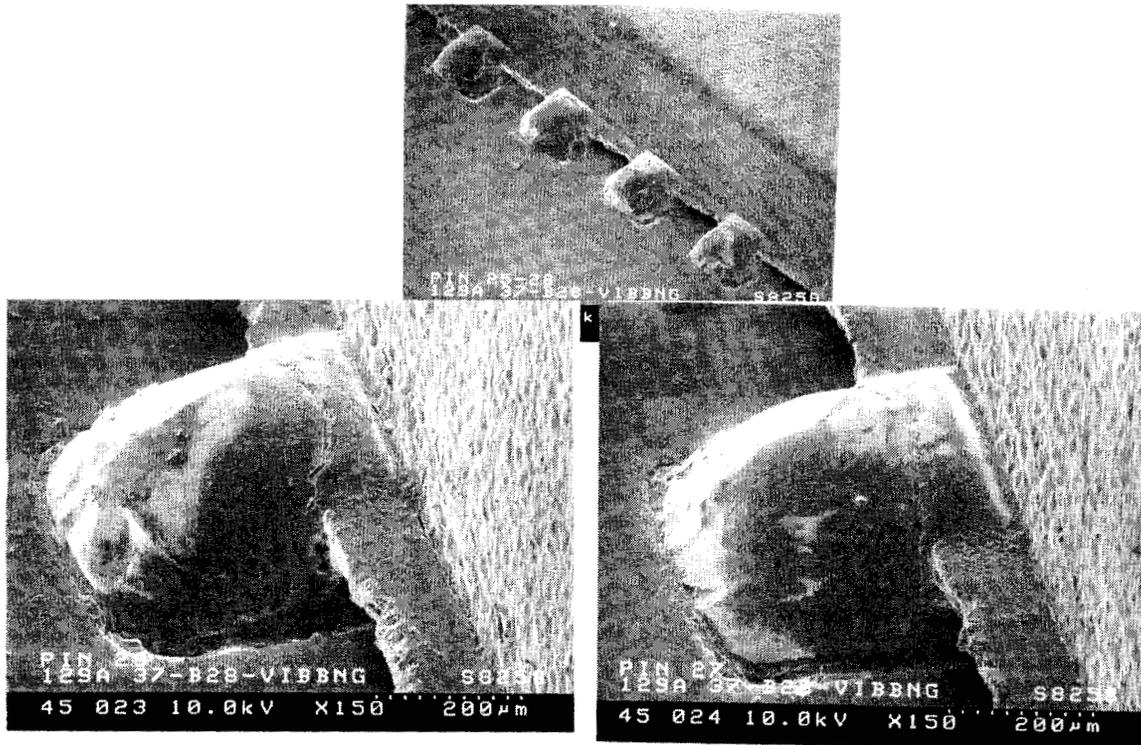


Figure 8 SEM Photo micrographs of pins 25-28, top right corner, away from center of board, after 2 hours of vibration at 7.8 Grms and additional 2 hours at 16.9 Gmrs. Hair line cracks are apparent on the enlarged pin 28 (left) and pin 27 (right)

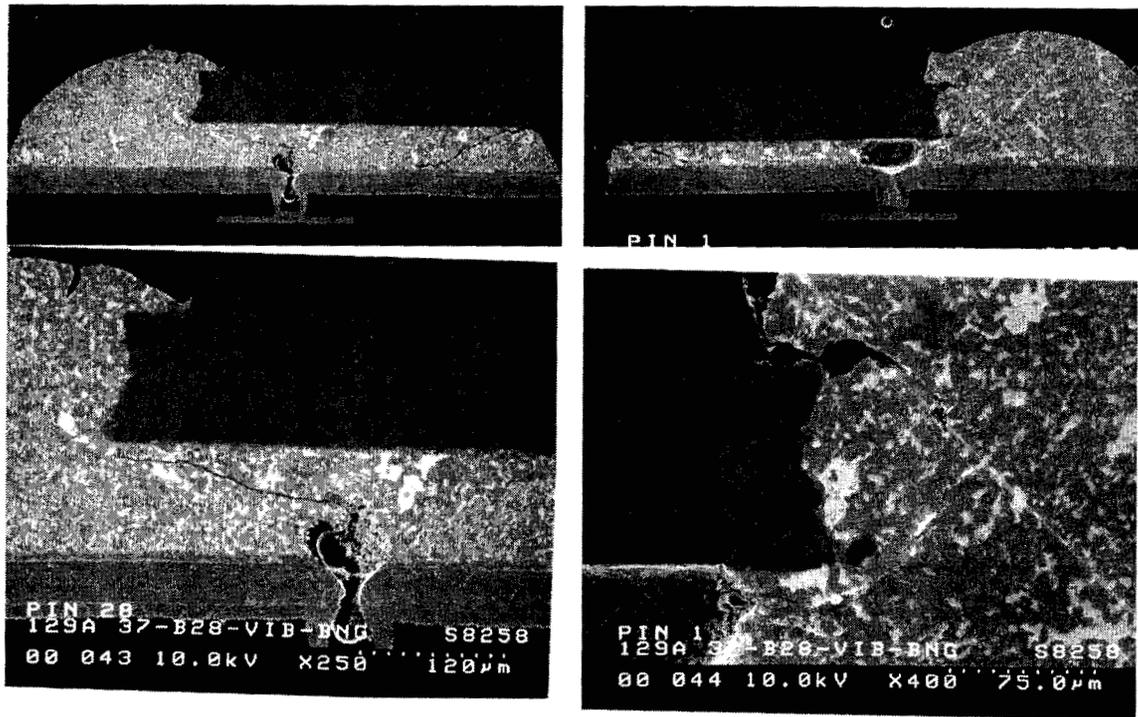


Figure 9 SEM cross-sectional photomicrographs of pins 1 and 28 (top left and right corners) with hair line cracks in solder joint under the pin extended to the toe