

Endurance Cycling Results in Extreme Environments

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Abstract—A new test bed for life testing flash memories in extreme environments is introduced. The test bed is based on a state-of-the-art development board. Since space applications often desire state-of-the-art devices, such a basis seems appropriate. Comparison of this tester to other such systems, including those with data presented here in the past, is made. Limitations of different testers for varying applications are discussed. Recently developed data, using this test bed is also presented.

testing. Time considerations usually cause the most trouble with life testing. When equipment must be tied up for months, however, other issues also press test development. The advantages, relative to long term use, of this tester will be compared to other testers used by JPL.

A particular application of the development board to life testing is presently cycling devices. The devices under test are the Samsung and Toshiba 256Mb NAND flash memories (K9F5608 and TC58256, respectively). For this application the environment involved is purely temperature, as the parts are being exercised at -30° C, and $+100^{\circ}$ C. Results of this testing will be discussed.

Solutions to particular testing questions bring along the possibility of improving methodology. To that end, this tester includes a large set of improvements over previous test methods. The limitations of the tester will have to be considered for any particular application. However, for life testing of flash memories in extreme environments, the limitations are generally clear of the test needs.

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1. INTRODUCTION

Flash memories continue to be an interesting solution for nonvolatile data storage in space missions. These missions include requirements on device function in extreme environments. Space and other high reliability applications of flash memories must have knowledge of device parameter degradation or failure due to such environments. Since flash memories under consideration are usually state-of-the-art, commercial driven products, information about such degradation is not widely available, if known. So it is often the job of the customer to understand the impact of environmental effects.

A new tester has been developed for life testing at JPL. This tester is based on an FPGA SoC development board with many capabilities. Attractive qualities of the development board include flexibility, size, cost, and ability to exercise devices near their specified speeds.

Testing mechanisms that immediately appear under stress are also important. However, such testing is by nature short, and therefore lacks many of the challenges of life

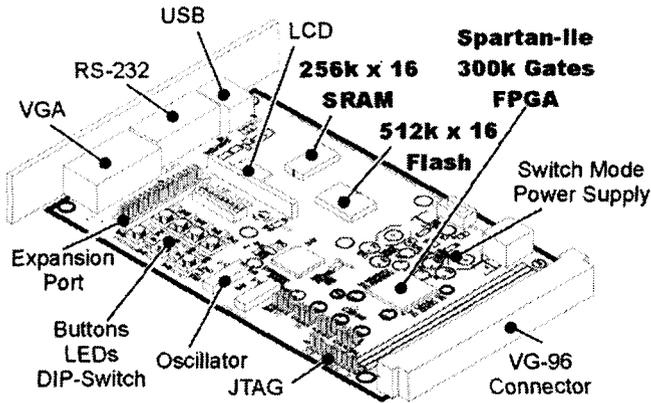
2. DESCRIPTION OF TESTER

A. Platform for Tester

The new tester is based on the Trenz Electronic's TE-XC2Se board. This is a small (160mm by 100mm) SoC development board with a wide variety of capabilities. A Xilinx XC2S300E Spartan IIe FPGA makes up the core of the board, though improved boards with upgraded FPGAs are also available.

Figure 1 is a diagram of the board's layout. Designers might use this board in two ways. The board has built-in test switches and LEDs, as well as a LCD, all of this would allow communication with an embedded program. There are also several I/O options to suit differing needs of a computer interface. For the tests discussed later, the RS-232 port was used for I/O and was controlled by the FPGA. At the time the test was developed, use of the

USB port was not directly supported by the software bundled with the development board.



TE-XC2Se Spartan-IIe Development Platform

Figure 1. The layout of the SoC development board used for test development. The devices and interfaces are all available to the Spartan-IIe.

This board has several advantages by itself. First, it is inherently real-time. Computer interface limitations are thus reduced. Second, development of test configurations is made in HDL, though the Xilinx MicroBlaze soft processor core allows c-based development also. Thus development is state-of-the-art, and can include third party HDL options, such as a USB controller. Third, the device is small and inexpensive. Tests can be compartmentalized and scaled linearly with ease. If necessary an entire developed test could be stored for future implementation.

B. Development Platform to Test Application

The first use of the development board by JPL is for life testing of flash memories. Flash memory testing brings certain problems to the table that other memories do not. There are typically long wait periods during programming and erasing where status must be checked. In many cases architecture for erasing and writing can be different, and selectable by the user application. Failure to choose the fastest configuration can result in doubling life-test time. Also some flash memories require maintaining a bad block list in order to meet operating specifications. This block list may be required to expand toward end of life.

The tester was designed for life testing 256Mb NAND flash memories from Toshiba and Samsung. The goal being to test ~30 to end of life in various environments. Both devices (Samsung K9F5608 and Toshiba TC58256) require the maintenance of a bad block list, and require asymmetric erase and programming architecture. For fastest operation the largest size of “burst write” and “burst read” are used.

Life testing must support many devices at a time, otherwise total test time increases with number of DUTs. However, since test requirements called for several devices for each environment, six DUTs are connected to one development board. The combination of the development board and the six DUT daughter card is dubbed the Trenz Based Tester (TBT).

To fit all the functionality for asymmetric erase and write, as well as bad block monitoring, and six DUT support in to the tester, the Xilinx MicroBlaze soft processor core was used to program the FPGA. This choice was doubly beneficial since existing c-based PC code was ported easily.

Figure 2 shows the internal routing of buses, as configured using the support software for the development board. The connection to the SRAM was necessary because the bad block list is different for each of the six DUTs, and can be as large as 1kB for each. The SRAM functionality was seamlessly integrated due to the bundled software.

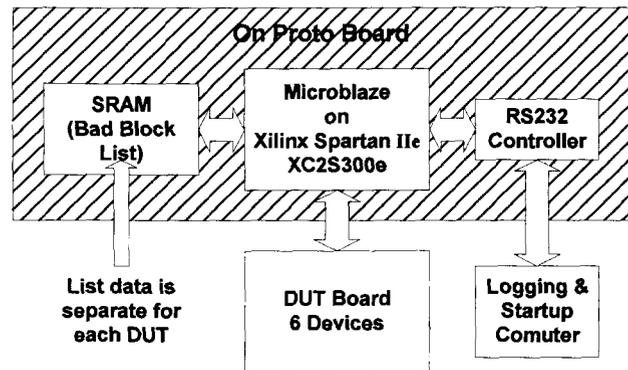


Figure 2. This is the functional layout of the TBT. Note that the Spartan IIe connections are all made via Trenz library software.

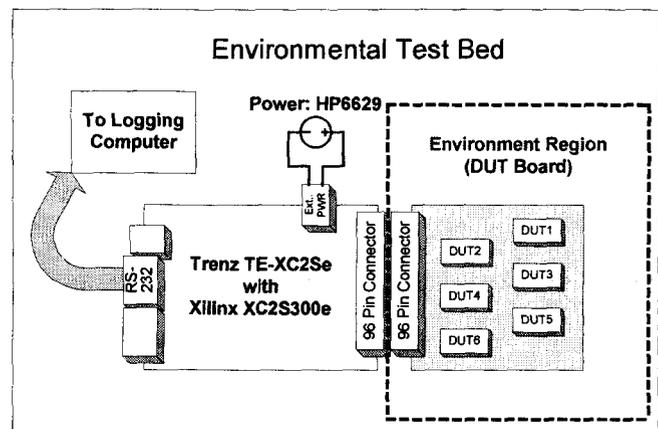


Figure 3. Hardware layout of the TBT includes the Trenz SoC development board, DUT board, power connection, and logging connection.

The hardware layout is quite simple for this application. It is drawn in figure 3. Although the tester is shown cut at the 96-pin connector for environmental testing, this is only demonstrating the current test configuration. The development board has been verified to work in vacuum. The development board was not tested for temperature, moisture, or charging environments for this work. With proper shielding of the development board, the tester may be placed in a radiation environments with only an RS-232 connection to the outside (e.g. long term TID testing).

3. COMPARING ALTERNATIVES

A. Other Solutions

Before the TBT can be assessed as a life tester, its competition must be considered. There are, of course, absolute conditions that might be considered pass/fail criterion for the TBT. However, how it stacks up to the competition is of greater value since not all tests require the same capabilities. The next few paragraphs introduce similar testers, and give brief descriptions of their test methods. This list is not meant to be exhaustive, it is provided for comparison of these methods only. Selection of a "best" solution for all situations is not considered a goal of presenting this information. Each of these testers had or has a purpose that is not necessarily comparable to the TBT.

One test method to examine was used for the compiling of data presented last year by G. Swift [1]. The failure mechanisms of interest were the flaky bit and the block erase fail. To obtain this information, the test was conducted at -55°C for 100k cycles. The devices were from a lot designated for construction of a Non-Volatile Memory Slice (NVMS), and the most expeditious solution for life testing seemed to be use of an engineering board with the same layout as the slice.

Since the entire slice had the same requirements as the devices, the entire test solution was placed in the environmental chamber, and cycles were put on the memory array. The board was designed with a layer of hardware abstraction desired for the intended application. That abstraction limited device visibility.

The second life testing solution presented for comparison is that used for obtaining data by L. Scheick and D. Nguyen [2]. The data was collected using an Advantest 3342 test system. This test system is designed around complete characterization of one device. Therefore, testing was done one device at a time. The failure mechanism studied was the ability of the device to erase properly (to all "1's"), and to program properly (to all "0's"). Since single device life testing is so slow on flash

memories, effective data rate was increased by reducing the fraction of the device tested at any time.

The TBT should also be compared directly to the test system it is based on. All of the code, and the test architecture, were derived from a PC based tester built on a custom PCI digital I/O board. The original intention of the PC based tester was single part characterization for radiation single event effects (SEE). SEE testing is often exploratory in terms of failure mode. So that tester was kept as flexible as possible. All control signal waveforms were developed by code running on the PC. Two inherent life-testing limitations derive from this. The first is the test has a maximum speed defined by the PCI bus, this includes a bus turn-around penalty of $\sim 300\text{ns}$. The second is that for flexibility, only one device could be controlled at a time.

B. Testing Complications

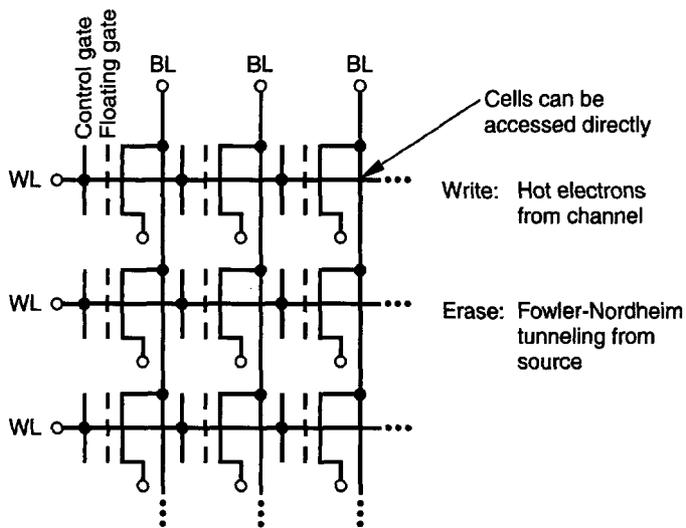
The largest problem with high statistics life testing of flash memories is the amount of time involved in erase-write-read cycling of just one device to end of life. Table 1 shows a breakdown of manufacturer's specifications for this type of cycling. The table assumes only one write and one read per address, per cycle of the device. It assumes filling buffers and reading from buffers for every read and write cycle. The most beneficial partitioning of the device for each operation is assumed (for example the 128Mb NOR device is programmed most quickly at 32 bytes per program command).

Size	Type	Full Life Test (days)	
		Typical	Maximum
128Mb	NAND	13	26
8Gb	NAND	140	270
128Mb	NOR	290	1200

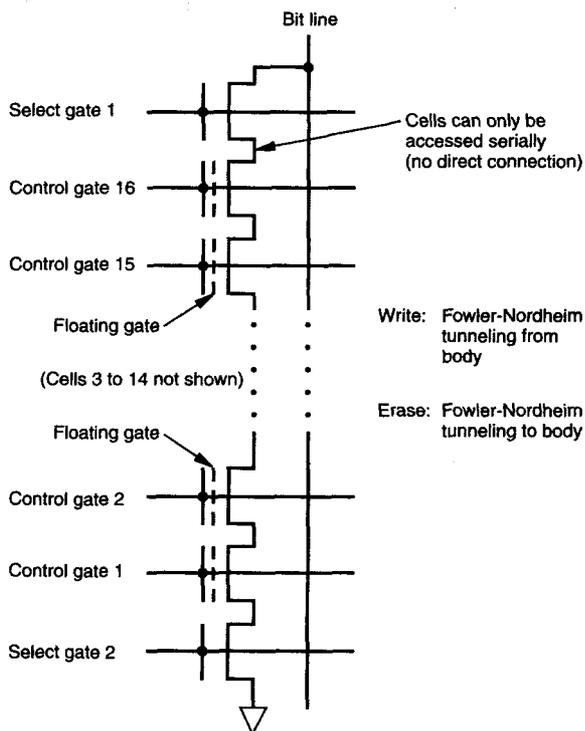
Table 1. The expected and maximum times for full life testing of devices. These are based on manufacturer's "typical" and "maximum" operating parameters.

Because the theoretical fastest times are now approaching a year, it is not clear that the fastest tester is the best. One certainly wouldn't want to double the length of a test by using a slow tester, but tying up an industrial tester on one device for an entire year is a daunting proposition.

The matter is further complicated by the failure mechanisms. Figures 4 and 5 show the architecture for the two flash memory types [3, 4]. The NOR grid structure is inherently more stable because the cells have unique control lines on both bit and word lines. The NAND structure provides a possible set of questions. How would a test be designed to examine read-disturb or program-disturb problems that occur because bit lines are shared? Sampling these wear-out problems could make a life test balloon up quickly.



3 wordlines and 3 bit lines shown
 Figure 4. The layout of flash memory NOR architecture is shown. The array is symmetric for each cell.



Memory stack height is 16 cells, plus 2 select cells
 Figure 5. The architecture of NAND flash memories.

The stacking structure can lead to additional wear out mechanisms requiring different test structures. Environments also complicate the testing puzzle. The possible synergistic effects, such as those reported previously [1], can lead to very large test matrix. Sometimes these effects can cause predictable enhanced aging, speeding up a life test. However, the shortened test time may be penalized by a larger set of environmental test vectors.

C. Discussion and Comparison

The important categories of comparison for flash testing, and the discussed testers seems to be: (1) ability to test at speed; (2) additional cost for additional devices; (3) non-recurring setup cost; (4) flexibility of test patterns; (5) cost of individual tester; (6) cost of operating tester, including people and resources; (7) ability to test multiple environments simultaneously. The test systems are compared in each of these categories in table 2.

Comparison Category	TBT System	PCI System	Advantest Tester	NVMS Tester*
Type of System	Embedded Prototyping	PC Prototyping	Industrial Testing	Application Testing
Test at Speed (1)	Yes	No	Yes	Yes
Scalability Limit (2)	~50	~1	~1	~20
Non-Recurring Cost (3)	Low	Minimal	Low	Low
Test Flexibility (4)	Medium-High	High	High	Low
Cost of Tester (5)	Low	Medium-Low	High	Medium - locks resource
Operating Cost (6)	Low	Medium-Low	High	Low
Multiple Environments (7)	Multiple boards, one PC	Multiple PCs and boards	Multiple Advantest units	Multiple E-Samples

*: assumes an application engineering sample exists

Table 2. This table compares the discussed test systems relative to certain limiting parameters of life testing. The final column, application test, may vary widely depending on the specific application.

Again, this comparison is not inclusive of all general test schemes. Of this set, the best general system for multiple environment full life testing of flash memories is the TBT based on the Trenz development board. For particular applications where one of these categories might be heavily valued, the TBT may not be the best.

4. TEST RESULTS

Data has been produced using the TBT system on Samsung and Toshiba 256Mb flash memories. Getting data quickly took a back seat to working out timing issues

on the TBT. The configuration currently exercises parts about six times slower than optimal.

The setup is cycling 24 flash memories. Twelve of these are being cycled at +100° C with six being Samsung devices at ~34k cycles, and the other six being Toshiba devices at ~48k cycles. The other twelve are being cycled at -25° C, with all of them at about 14k cycles (again six Samsung and six Toshiba devices). Environmental stability limitations have reduced the amount of time available for the low temperature testing. Thus far the data is null. There has not been any observed event with statistical validity.

These parts appear to be immune to the rather benign environments thus far applied. Once this cycling is out of the way, and the TBT proven itself, additional testing will be considered. Among the available test configurations would be much colder or much hotter temperatures. Also some exploration of the synergistic effects of radiation dose and temperature exposure may be examined.

5. CONCLUSIONS

The Trez Electronic's TE-XC2Se based flash memory tester (TBT) is suitable for life testing of flash memories in extreme environments. Such testing is necessary because space applications often include environment requirements outside of the manufacturer's intent. Since desired devices are usually state-of-the-art and therefore market driven, life testing is the burden of the consumer.

Other solutions to the puzzle of life test development exist. These solutions have test data previously reported. In many cases, time demands, or test tuning demands, make these alternatives less desirable. This is especially true given the trend of the industry toward devices requiring years for life testing. Cost of scaling the test system to the number of devices required rules out many of the remaining solutions.

Data produced with the TBT system presently covers a total of 650k device-cycles with testing running smoothly for only a few months. This system requires almost no human attention except to verify the environmental chambers are still operating. To date no measurable device degradation has occurred.

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