



# Novel Multiplexing Technique for Multi-Megapixel Detector Arrays

### Results

- A novel Code-Division Multiplexing technique for imaging arrays based on the Hadamard Transform encoding investigated;
- An architecture for a CMOS based imaging array utilizing the new technique designed;
- The Hadamard-Transform Hybrid Imager (HT-HI) modeled and the ultimate performance figures in comparison with the SOA CCD and CMOS imagers determined.

### Benefits to NRO

Greatly improves space and airborne reconnaissance imaging capabilities by allowing for a very large format, very sensitive imaging camera with high frame rate. The camera would be capable to perform real time imaging of faint objects with high spatial resolution. An additional benefit is a 30-times reduction in power dissipation.

### Parameters of HT-HI

Very large format (10k x 10k)  
 Frame rate >100 fps  
 Low pixel noise < 20e-  
 Dynamic range > 10 bits  
 Snap-shot shuttering  
 100 pW/pixel dissipation

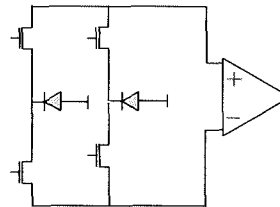
### Comparing to CCD this is...

	similar	better
Very large format (10k x 10k)	▼	
Frame rate >100 fps		▼
Low pixel noise < 20e-	▼	
Dynamic range > 10 bits		▼
Snap-shot shuttering		▼
100 pW/pixel dissipation		▼

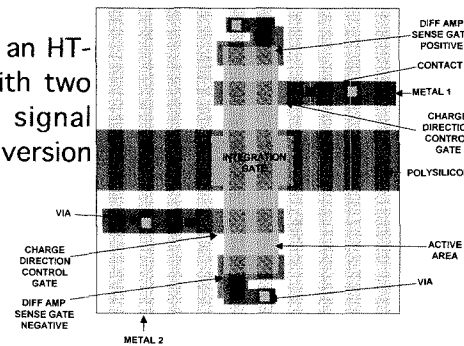
### Principle of Operation and Pixel Architecture

The Hadamard Transform multiplexing implies reading of pixels with a single amplifier not one by one but in groups of N. Each element in the group is multiplied by 1 or -1 according to the HT algorithm and then all signals are added. The procedure repeats N times and every time the sequence of 1 and -1 varies. After that the original magnitude of signals can be recovered. The technique improves the signal-to-noise ratio by  $N^{1/2}$  and reduces the number of hybridization bumps for the CMOS array by N thus allowing for a much larger format. As a result, the new hybrid imager preserves all signal processing and low-power dissipation advantages of CMOS arrays while reaching the format and the sensitivity of best CCD arrays.

Schematics of a 2-pixel HT-HI array with a single read-out amplifier



Layout of an HT-HI pixel with two gates for signal polarity inversion



### Follow-on Work and Contact Information

As the first step (proof-of-concept), JPL is interested to build and demonstrate a small-scale prototype of the HT-HI. Interested parties contact

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