

ON BOARD PROCESSOR DEVELOPMENT FOR NASA'S SPACEBONE IMAGING RADAR WITH SYSTEM-ON-CHIP TECHNOLOGY

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ABSTRACT

This paper reports a preliminary study result of an on-board spaceborne SAR processor. It consists of a processing requirement analysis, functional specifications, and implementation with system-on-chip technology. Finally, a minimum version of this on-board processor designed for performance evaluation and for partial demonstration is illustrated.

1. INTRODUCTION

Spaceborne SAR processing for NASA SAR missions has been carried out by ground processing facilities for two decades. Processing the SAR data on board the spacecraft was an unachievable goal due to lack of necessary technology. Until recently, the capability of a spaceborne computer has been below the range of several million instructions per second. As a comparison, to achieve real-time SAR processing such as a Seasat like mission, it requires at least 10 giga floating point operations (GFLOP) per second. However, the recent aggressive advancement in the very large scale integrated circuit (VLSI) technology has dramatically reduced this gap. On-board computer with over one GFLOP capability has already pursued by several vendors. Thus, on-board SAR processing will be a promising alternative in the near future.

The advantages of processing the SAR data on-board are the followings. First, it allows a higher precision (more bits) SAR data fed into the processor to generate better quality image. Second, it would enable a more effective data compression to reduce the down link data rate and the amount of data to be archived. This is very critical to the success of a multi-band and multi-polarization radar to be flown in the near future. Third, it reduces the cost associated with ground data processing operations. Fourth, it provides a quick feedback to the radar controller to ensure proper radar operation such as using the correct pointing angles and radar parameters for various types of targets.

2. PROCESSING REQUIREMENTS

Prior spaceborne SAR missions including Seasat, ERS, JERS, and SIR series mapped the Earth surface by using a strip mode operation. The newly launched RADARSAT and future ENVISAT further include a wide swath imaging mode named ScanSAR. Both of these imaging modes are considered as basic processing capabilities required by the on-board processor.

2.1. Strip Mode Algorithms

A strip mode SAR system is the most common imaging SAR system. Algorithms for processing a strip mode SAR include (1) range-Doppler algorithm [1], (2) time domain algorithm, and (3) chirp scaling algorithm [2]. Among these algorithms, only (1) and (3) will be considered here due to their higher throughput rate performance.

The range-Doppler algorithm basically is limited to a pointing near zero Doppler. But, when combined with the secondary range compression [3], it may accommodate a relatively larger Doppler

range. In general, it is capable of strip mode SAR processing over a limited range of squint angles. This algorithm is very efficient and having a very good image quality. But, its phase accuracy is worse than the chirp scaling algorithm. This algorithm is considered as a candidate algorithm for a strip mode SAR on-board processing when SAR squinting is not required and when its phase accuracy meets the system requirement. The data flow diagram of this algorithm is depicted in Figure 1.

The chirp scaling algorithm is capable of handling SAR data with very large squint angles and has a very accurate phase in its complex image. The disadvantages of this algorithm is that (1) it is inefficient in handling large changes of the Doppler centroid with range, (2) its efficiency may be degraded by an imperfect radar chirp (nonlinear FM), and (3) it is only an approximation for non-rectilinear geometry. Since it is complementary to the range-Doppler algorithm, it is also considered as a candidate processing algorithm for a strip mode SAR.

2.2. ScanSAR Mode Algorithm

There exists several similar algorithms for ScanSAR processing. A relatively well known algorithm is the SPECAN [4] processing algorithm. The SPECAN algorithm is computationally efficient. It has a very good image quality when the range migration of each target observed in each radar burst is approximately linear. Since the image generated from the SPECAN algorithm is in range-Doppler coordinate, it must be resampled into a projection coordinate before look overlay or beam-to-beam mosaicking. The data flow diagram of this algorithm is depicted in Figure 2.

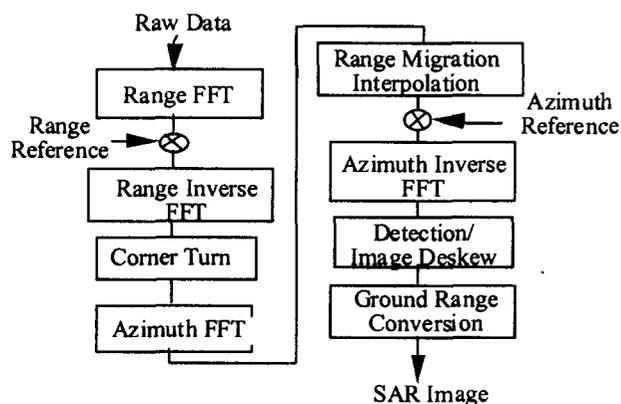


Figure 1. Range-Doppler SAR Processing Algorithm.

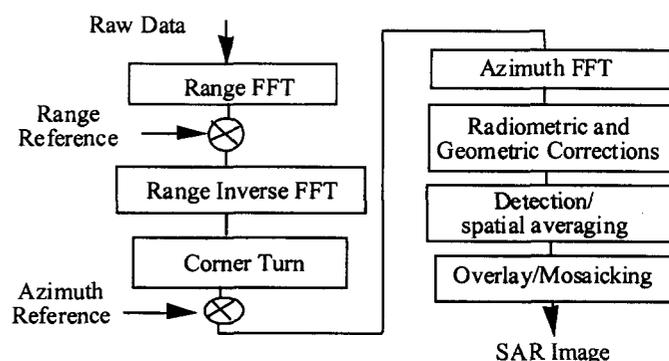


Figure 2. ScanSAR SAR Processing Algorithm.

2.3. FLOPS and Memory Size

The amount of arithmetic operations required must be estimated for assessing the processor computation load requirement. For real-time SAR processing, this load is a function of the input data rate, which is determined by the range sampling bandwidth f_s scaled by the product of range gate window duration T_g and the pulse repetition frequency PRF. The real-time processing throughput rate requirement is therefore the product of the SAR input data rate and the mean number of floating point operations (FLOP) required for each input pixel.

The amount of memory required for SAR processing is estimated based on the required input and output buffer size of each stage for each algorithm. This size is also a function of the radar operating wavelength. Listed in Table 1 are the computation load and memory size requirement for both the strip mode and ScanSAR mode algorithms. The chirp scaling algorithm is more demanding than the range-Doppler algorithm. The SPECAN algorithm is relative less demanding than the strip mode algorithms.

Table 1. Required Computation Load and Memory Size

Requirement \ Algorithm	Range Doppler	Chirp Scaling	SPECAN
Computation Load (GFLOPS)	9.0	10.5	6.0
Memory Size (MBytes)	$640 * R^a$	$800 * R$	$512 * R$

R: the ratio of the radar operating wavelength to the c band wavelength

3. CUSTOM HARDWARE SPECIFICATIONS

A programmable on-board SAR processor implemented on a general purpose computer is of great interest in the future. This approach is studied by estimating the required processing capability through benchmarking the effective FLOP of several candidate platforms.

A more practical approach at the present time is based on custom hardware with system-on-chip technology. A fully pipelined on-board SAR processor is shown in Figure 3. However, in order to reduce the cost of such an approach, one must minimize the number of functional modules by incorporating slightly different functions into a single functional module. The planned functional modules include FFT, memory handling, reference generation and multiply, interpolation, and post image processing.

Specifications of each SAR functional module is briefly described in the following:

- The FFT module performs a standard FFT and can be implemented by using an array of DSP elements. The 200-Mhz FFT module does a 24 bit complex 1024-FFT in 16 uS.
- The memory handling module shall be capable of data buffering, strip mode corner turn, and ScanSAR mode corner. The memory handling module is based on a ping-pong buffer architecture with a multi-mode address control. The multi-mode address control supports the following configurations: one-IN-two-OUT in same dimension, one-IN-one-OUT in different dimension, one-IN-two-OUT in same dimension, one-IN-two-OUT in different dimension. The requirement of minimum number of bits needed to represent a SAR complex or real sample is derived and used to minimize the required power and weight of the memory handling module.
- The reference generation and multiply is based on a multiple LUTs method which generate 1-D and 2-D polynomial functions and weighting functions. It takes sine and cosine of the polynomial functions, and multiplies with the SAR data.
- The interpolation module is based on a programmable inner-product-like processor which performs 1-D weighted sum interpolation along either dimension or 2-D weighted sum interpolation.
- The post image processing module is based on a DSP array which performs image detection, overlay, and look normalization.

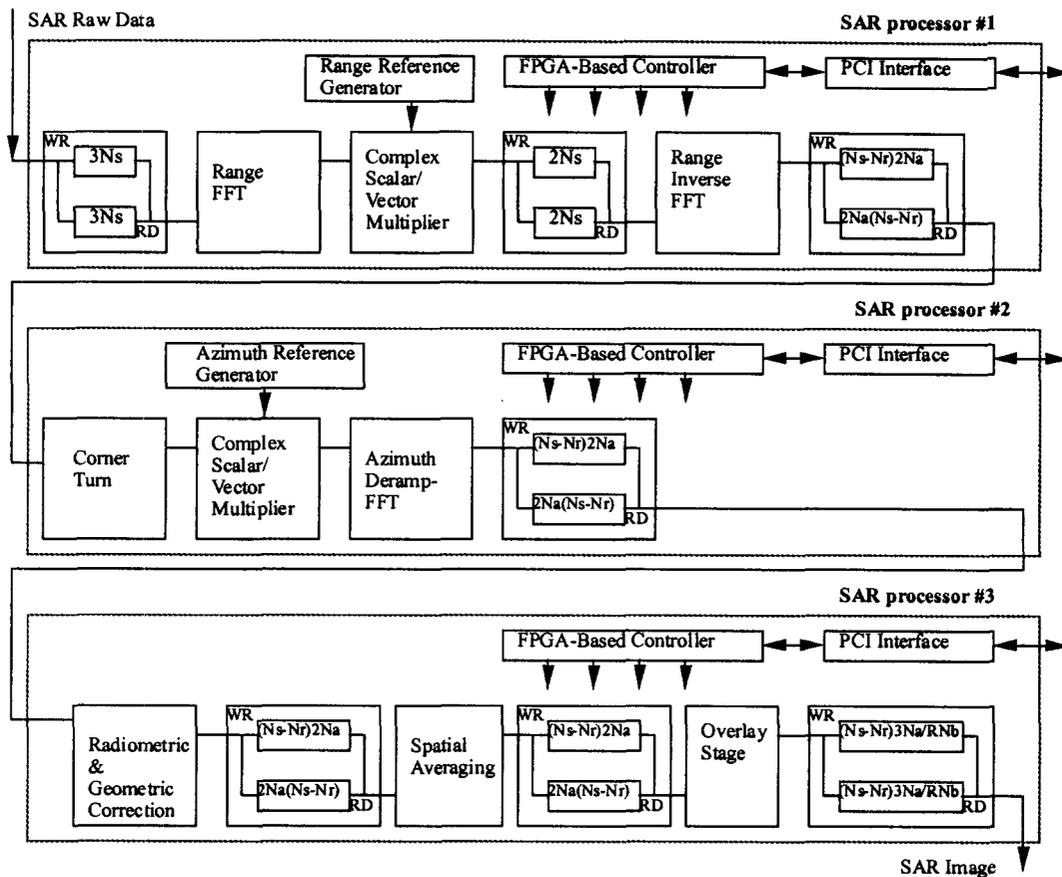


Figure 3. A fully pipeline architecture of an on-board SAR processor.

4. AN EXPERIMENTAL ON-BOARD SAR PROCESSOR

Figure 4 shows an architecture diagram for an experimental on-board SAR processor based on custom hardware. The host computer is a PCI/PowerPC based computer. Special SAR hardware modules are integrated into a single PCI card cage. The five functional modules defined in section 3 can be implemented onto a configurable processor board. Figure 5 shows an architecture diagram of this configurable processor. It includes a PCI interface, a FPGA-based controller, a DSP array processor, a multi-mode memory handling unit, a reference generation and multiply, and a SAR data direct input/output interface. The processor board can be configured for three SAR processing stages shown in Figure 3 : (1) a 2-D frequency domain range compressor, (2) a 2-D frequency domain azimuth compressor, and (3) an interpolation and post image processing board. The proposed SAR processor based on custom hardware provides an effective solution to achieve a high-performance low-power SAR processor for on-board applications at a relatively low cost.

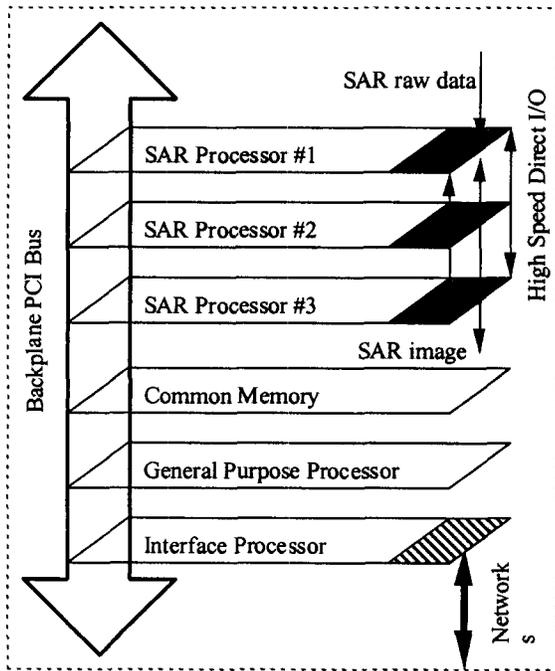


Figure 4. An experimental SAR processor based on a custom hardware.

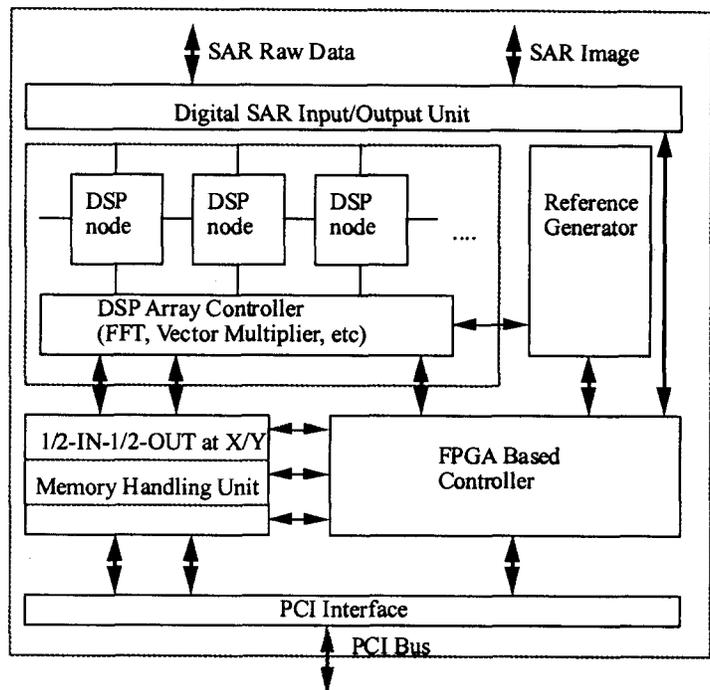


Figure 5. A unified processor architecture for different SAR processing stages.

5. CONCLUSION

A preliminary report on the study result of spaceborne SAR on-board processing is presented. Both strip mode and ScanSAR mode processing algorithms are studied. Implementation approaches include general purpose computer based system and custom hardware based system. An experimental SAR processor architecture is presented.

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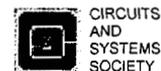
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