MARS SCIENCE LABORATORY

High Altitude Subsonic Parachute Field Programmable Gate Array

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Overview

This paper describes a rapid, top down requirements-driven design of an FPGA used in an Earth qualification test program for a new Mars subsonic parachute. The FPGA is used to process and store data from multiple sensors at multiple rates during launch, ascent, deployment and descent phases of the subsonic parachute test

The Mission

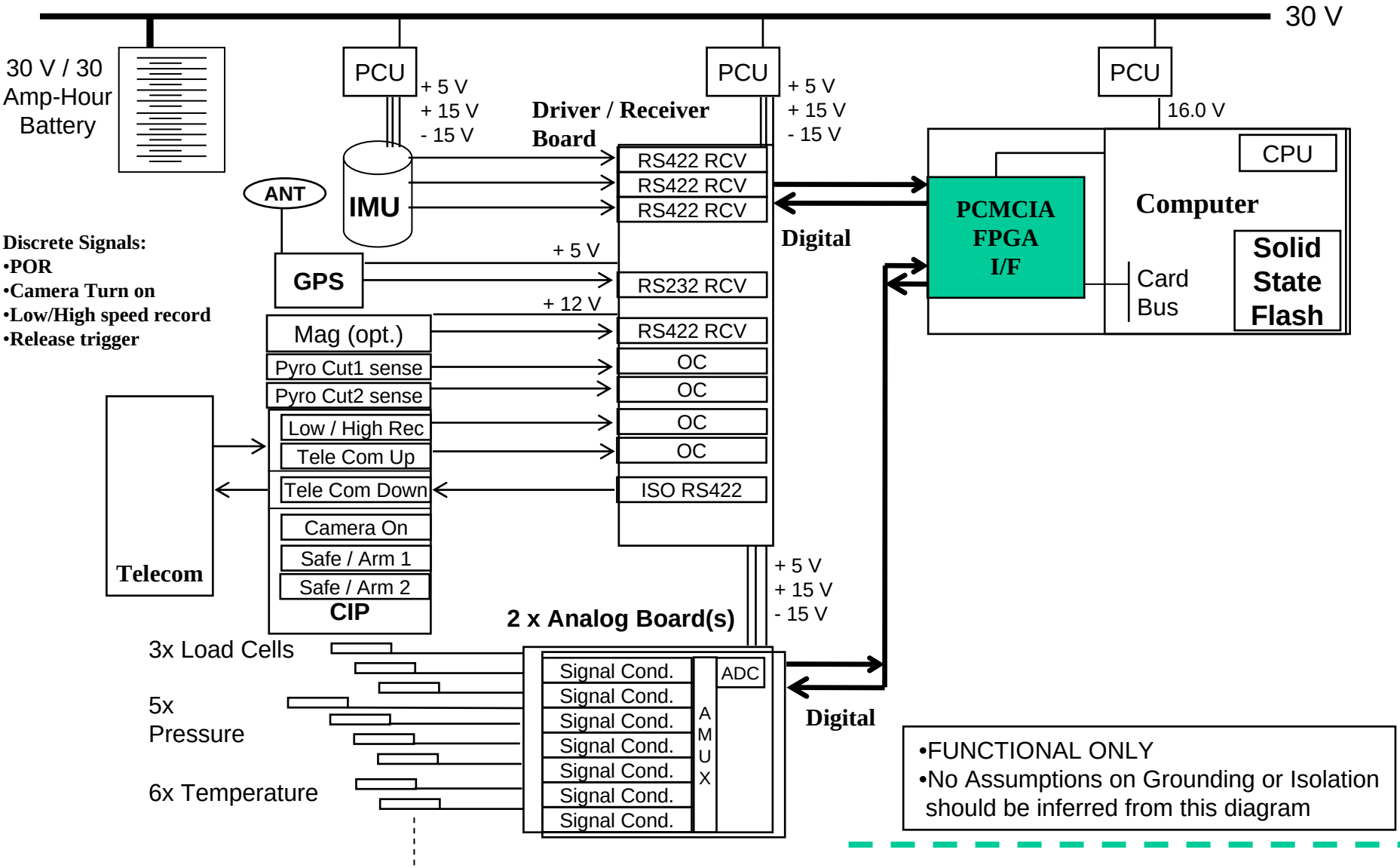
- The current Mars (Viking-heritage) supersonic parachute system was qualified in and used since 1972.
- New designs are under way that enable landing larger payloads for the upcoming proposed Mars missions.
- The approach of using a subsonic parachute in combination with the existing Viking parachute design as a two-stage system builds on the proven design and extends the payload mass capabilities to a new generation of missions.
- The subsonic parachute must first be tested.

Test Program

- Three high altitude subsonic drop tests were conducted in the fall of 2004 from Ft. Sumner, NM. A 12 million cubic foot helium balloon used to raise the test article to 120,000 ft altitude was launched and operated by the National Science Balloon Test Facility (NSBF).

- The FPGA is used to receive, compress, format, and write to memory 10 hours of deployment, inflation, and inflated performance of the subsonic parachute.

Test Instrumentation



Requirements

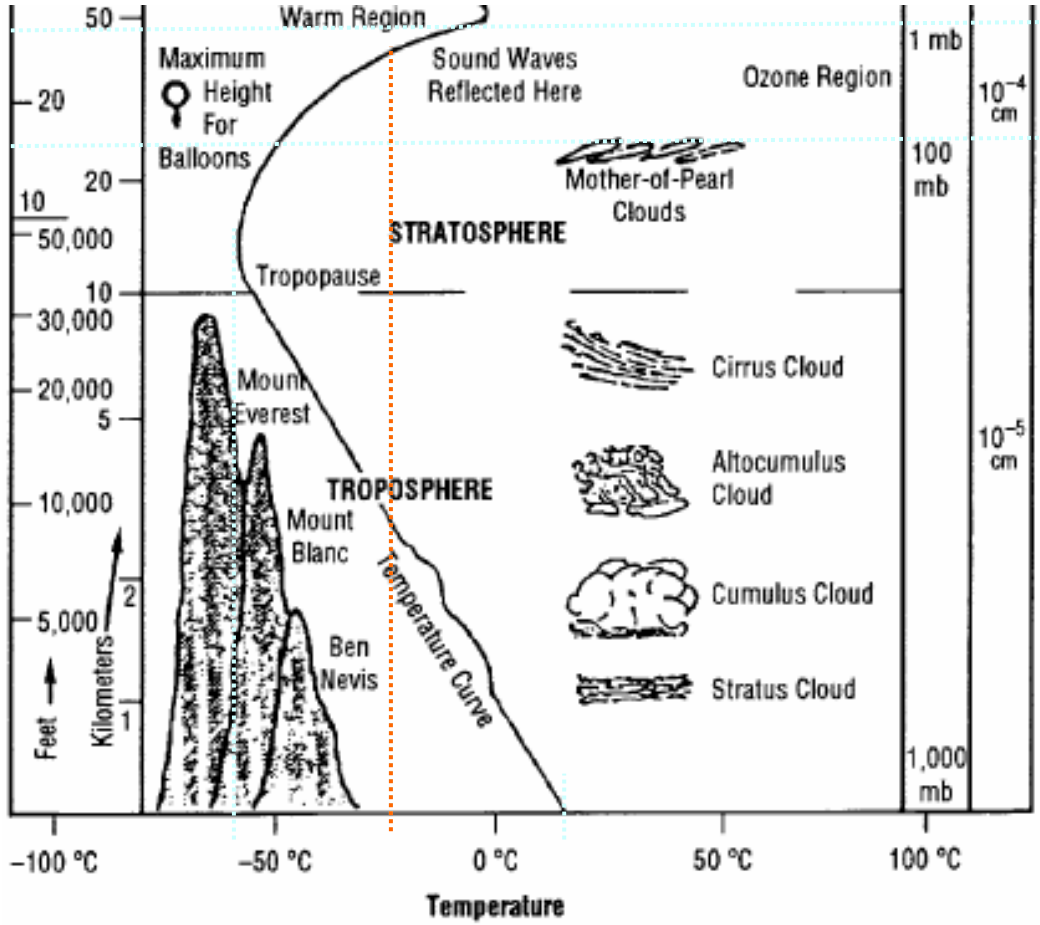
- Four months to deliver the FPGA (design and verification).
- Low mass, low power, Xilinx Virtex-E in PCMCIA form factor module.
- The memory storage is designed for 10-hours test duration Sufficient margin (100%) is included to account for possible delays in launch, or an atypical, prolonged period at the release altitude, total capacity 1GByte.
- The instrument set is designed and tested to operate and survive:
  - high altitude, low pressure environment extreme conditions
  - 1 day after touch down without data loss

Mission Profile / Thermal Environment

The instrumentation subsystem must operate over:

- **2.5 hour delay** launch pad
  - 20 deg. C (ground)
- **2 hour ascent**
  - **-54 deg. C (to 10, 000 ft)**
  - **-20 deg. C (120, 000 ft)**
- **4 hour drift at altitude**
  - **-20 deg. C (120, 000 ft)**
- **1 hour descent**
  - -20 (120, 000 ft)
  - -54 (10, 000 ft)
  - 38 deg. C (ground)

A total of **10 hours** from the last time it is accessed until ground impact.

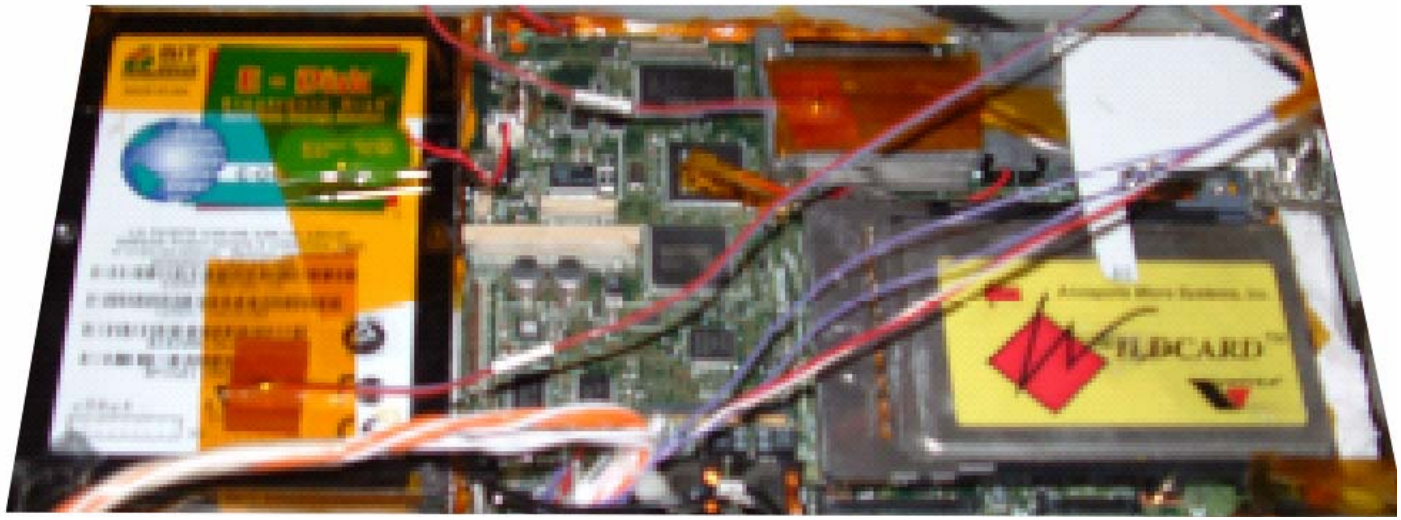


Adapted from: NASA Reference Publication 1350

The Natural Space Environment: Effects on Spacecraft, Nov. 1994

FPGA Implementation

- A COTs Xilinx Virtex-E FPGA embedded on a PCMCIA with a SRAM unit and PCI bus interface.
  - 26 Useable External I/Os
  - 52% Flipflops were utilized in this application
- Software on a SBC reads buffered SRAM using Direct Memory Access (DMA) to store the data in a flash disk.



Simulator / Synthesis Tools

- **ModelSim XE**
  - Version 5.6
  - Simulation and Verification
- **Visual C++ 6.0**
  - Used to compile host application
- **Xilinx Webpack 5.2i**
  - Place and Route
  - Maps design into target
- **Annapolis Microsystems Library**
  - Script Files
  - Cardbus bridge
  - Local Address and Data modules
- **Synplify Pro**
  - Version 7.2
  - Tried to use 7.5 and we had problems compiling
  - Synthesis: map of logic to FPGA technology
  - Generates EDIF File from Verilog and VHDL code

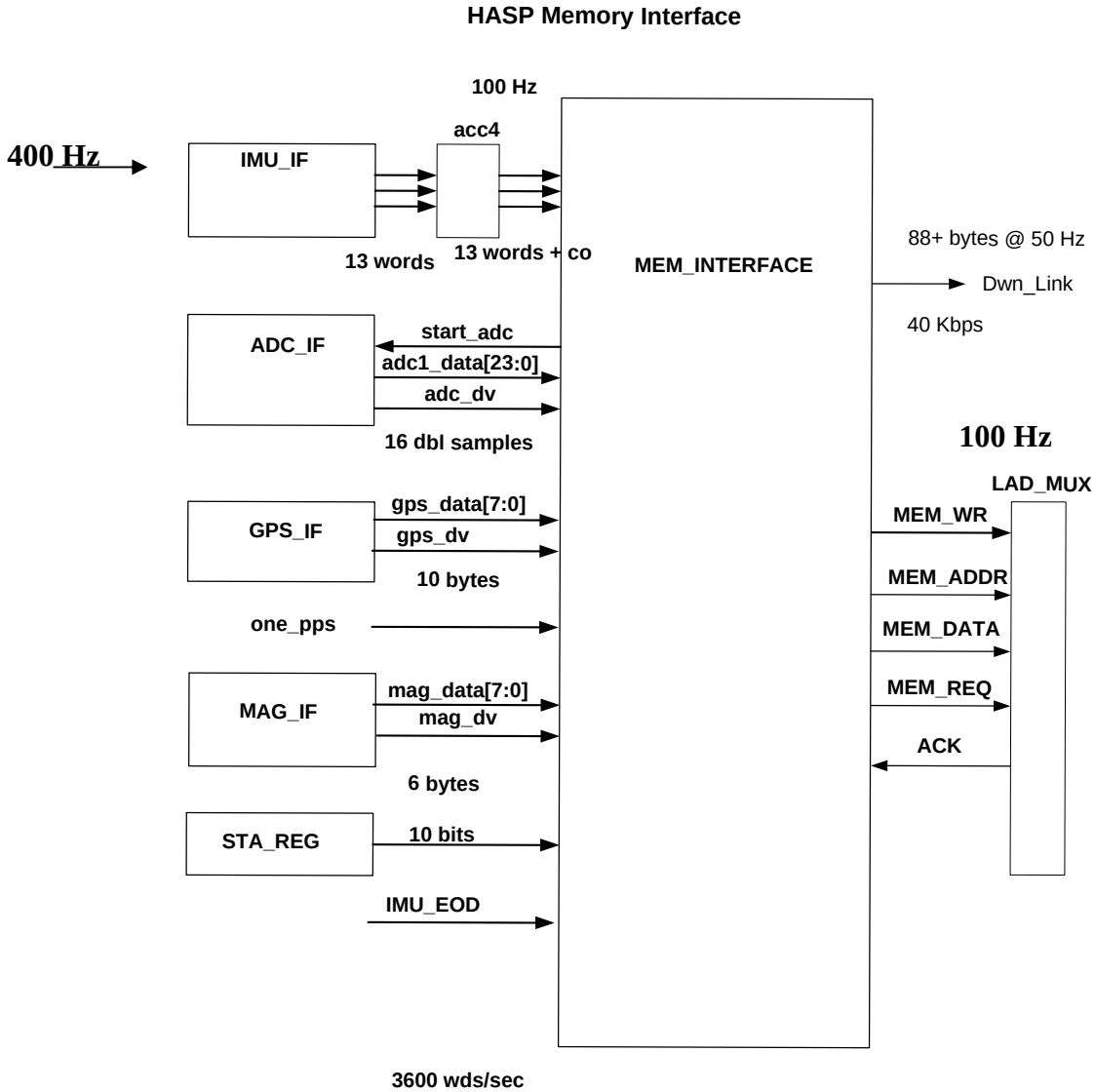
VHDL Wrapper

- **Developed using Annapolis Microsystems library**
  - **Control DMA word transfers to external flash disk**
  - **Control of Local Address Data bus**
  - **Mapped the external I/O pins**

Development Approach

- The FPGA design is guided by a spreadsheet of memory partitions based on data rates from each sensor.
- Accumulators are used to compress the high rate IMU data.
- A prioritized queue is used to control the servicing of received data from multiple sources.
- The memory transfer rate is high enough to allow single depth buffering.

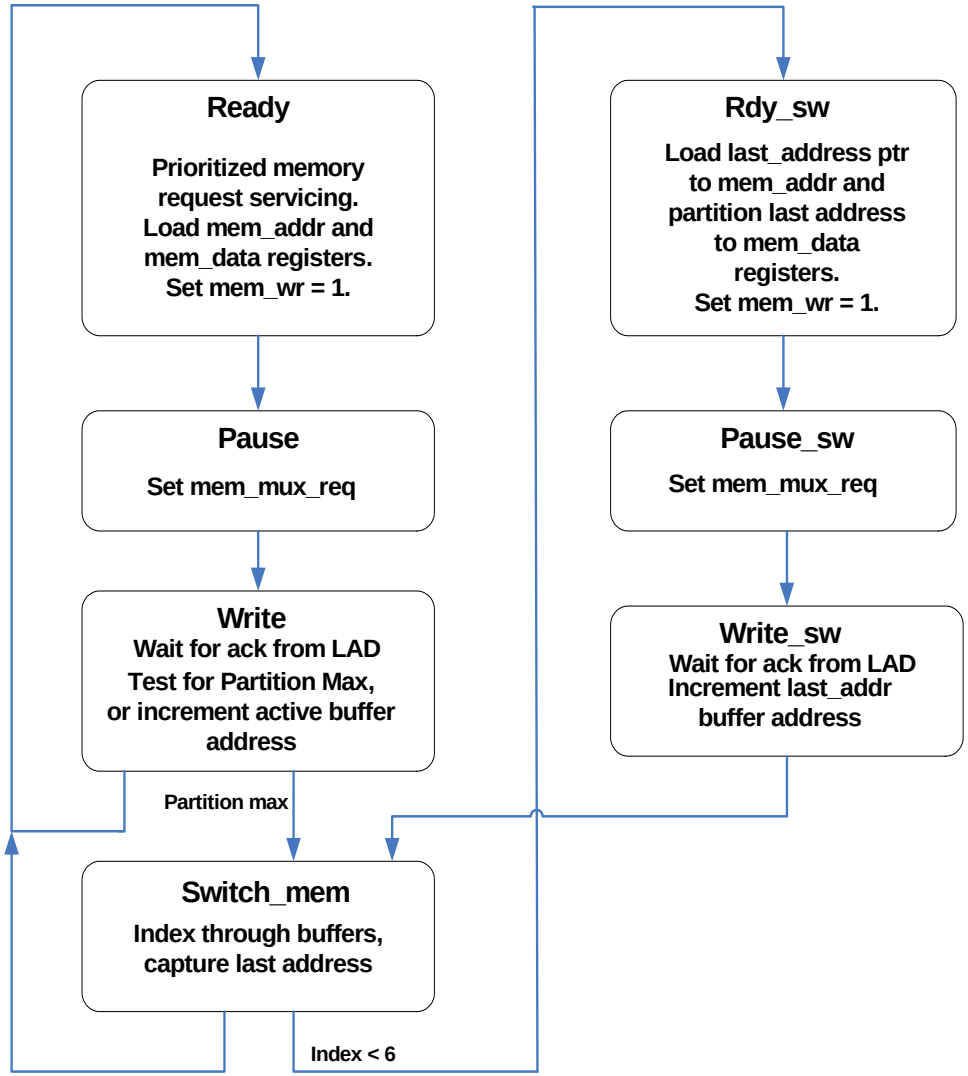
FPGA Core Organization



Rate-Based Memory Partition

		HASP Memory Partitioning						
	pkts	wds/pkt	partition size	start_dec	hex		end_dec	hex
	4440							
imu		5	22200	1	1	4	22200	56B8
adc		16	71040	22201	56B9	15AE4	93240	16C38
gps		2.5	11100	93241	16C39	5B0E4	104340	19794
mag		4	17760	104341	19795	65E54	122100	1DCF4
sta		2	8880	122101	1DCF5	773D4	130980	1FFA4
last_wr			6	130981	1FFA5	7FE94	130986	1FFAA

Memory Address State Machine



ADC Packet

HASP ADC DATA PACKET

word	mem_data[31:28]	mem_data[27:24]	mem_data[23:12]	mem_data[11:0]
1	pkt_cnt[3:0]	adc_addr[3:0]	adc.1. 0 [11:0],	adc.0. 0 [11:0]
2	pkt_cnt[3:0]	adc_addr[3:0]	adc.1. 1 [11:0],	adc.0. 1 [11:0]
3	pkt_cnt[3:0]	adc_addr[3:0]	adc.1. 2 [11:0],	adc.0. 2 [11:0]
4	pkt_cnt[3:0]	adc_addr[3:0]	adc.1. 3 [11:0],	adc.0. 3 [11:0]
5	pkt_cnt[3:0]	adc_addr[3:0]	adc.1. 4 [11:0],	adc.0. 4 [11:0]
6	pkt_cnt[3:0]	adc_addr[3:0]	adc.1. 5 [11:0],	adc.0. 5 [11:0]
7	pkt_cnt[3:0]	adc_addr[3:0]	adc.1. 6 [11:0],	adc.0. 6 [11:0]
8	pkt_cnt[3:0]	adc_addr[3:0]	adc.1. 7 [11:0],	adc.0. 7 [11:0]
9	pkt_cnt[3:0]	adc_addr[3:0]	adc.1. 8 [11:0],	adc.0. 8 [11:0]
10	pkt_cnt[3:0]	adc_addr[3:0]	adc.1. 9 [11:0],	adc.0. 9 [11:0]
11	pkt_cnt[3:0]	adc_addr[3:0]	adc.1. 10 [11:0],	adc.0. 10 [11:0]
12	pkt_cnt[3:0]	adc_addr[3:0]	adc.1. 11 [11:0],	adc.0. 11 [11:0]
13	pkt_cnt[3:0]	adc_addr[3:0]	adc.1. 12 [11:0],	adc.0. 12 [11:0]
14	pkt_cnt[3:0]	adc_addr[3:0]	adc.1. 13 [11:0],	adc.0. 13 [11:0]
15	pkt_cnt[3:0]	adc_addr[3:0]	adc.1. 14 [11:0],	adc.0. 14 [11:0]
16	pkt_cnt[3:0]	adc_addr[3:0]	adc.1. 15 [11:0],	adc.0. 15 [11:0]

pkt_cnt : increments, will have the same value for all 16 words in packet.

J. Kowalski
7/9/2004

IMU Packet

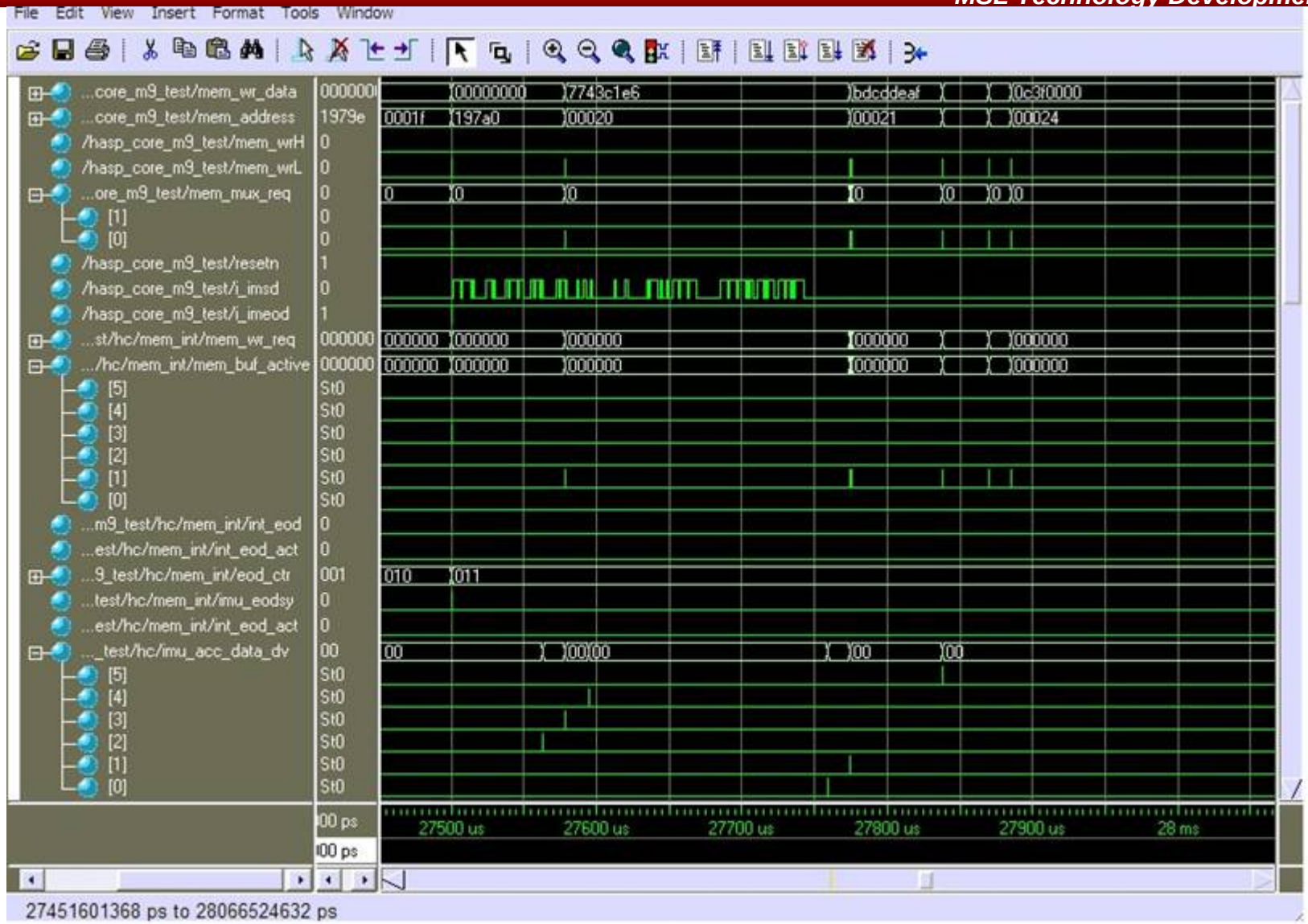
1		Y DELTA VELOCITY imu_data1[15:0]		X DELTA VELOCITY imu_data0[15:0]				
2		X DELTA ANGLE imu_data3[15:0]		Z DELTA VELOCITY imu_data2[15:0]				
3		Z DELTA ANGLE imu_data5[15:0]		Y DELTA ANGLE imu_data4[15:0]				
4		MODE BIT/MUX ID imu_data7[15:0]		IMU STATUS SUMMARY WD imu_data6[15:0]				
5		co4sum		MULTIPLEXED DATA WD imu_data8[15:0]				

FPGA Verification

Verification Tools & Methodology

- Hierarchical Verilog Simulation.
- Synplify and Xilinx Static Timing Analysis.
- Development Hardware Interface Testing: IMU, GPS, and ADC.
- Flight Model Integration and “End to End” Test at JPL.

FPGA Simulation – IMU write

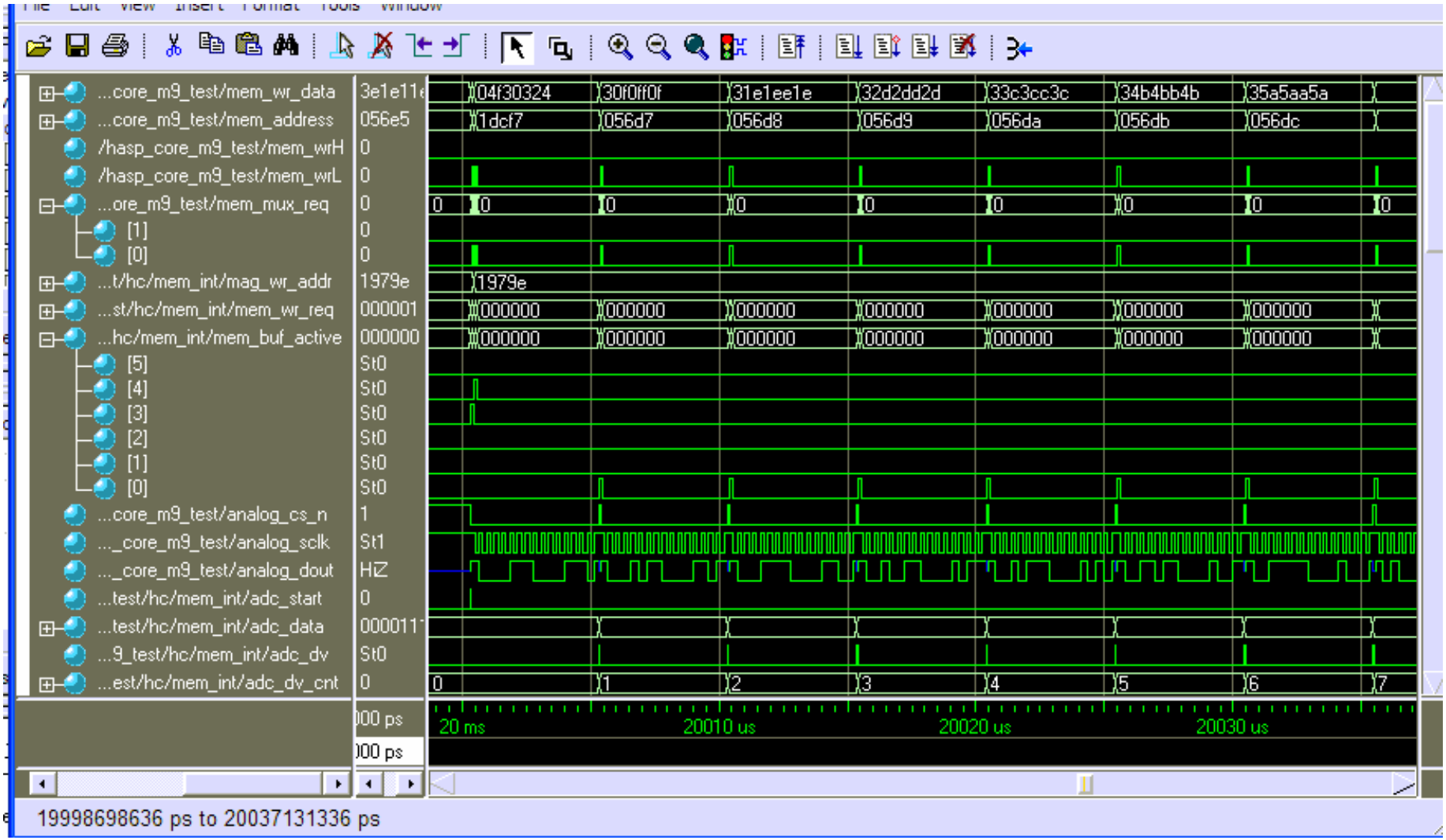


FPGA Utilization Statistics

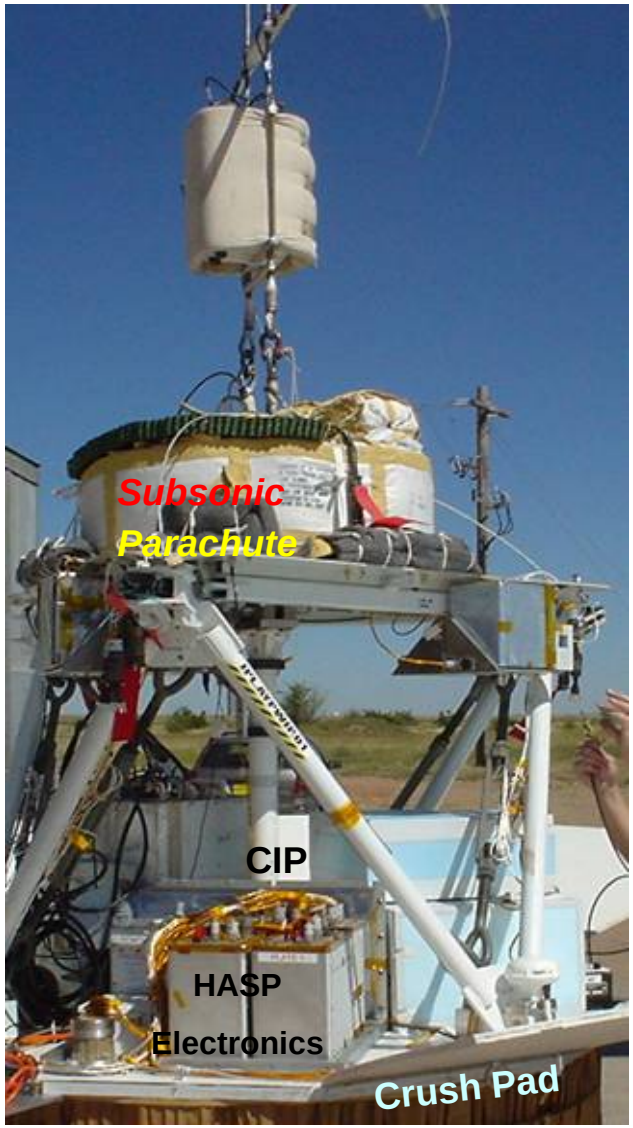
Logic Utilization	Used	Available	
• Number of Slice Flip Flops:	3,214	6,144	52%
• Number of 4 input LUTs:	3,510	6,144	57%
Logic Distribution			
• Number of Occupied Slices	2,824	3,072	91%
• # Slices w only related logic	2,824	2,824	100%
• Total Number 4 input LUTs	3,808	6,144	61%
• # Slices w unrelated logic	0	2,824	0%
• # used as logic:	3,510		
• # used as a route-thru:	264		
• # used as Shift registers:	34		
• # of bonded IOBs:	200	260	76%
• # of Tbufs:	1	3,200	1%
• # of Block RAMs:	10	32	31%
• # of GCLKs:	3	4	75%
• I/O Register bits:	0		

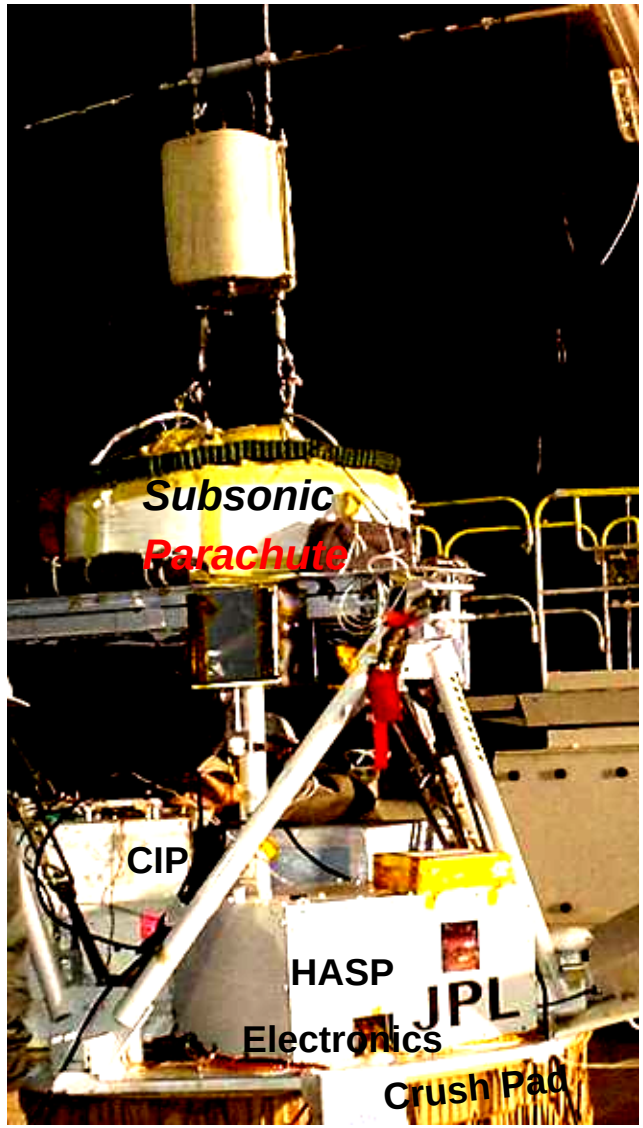
Table 2. From Xilinx Mapping Report

Analog Data Write



PAYLOAD DIAGRAM





Test Results

- Ten hours of the data was retrieved from solid state memory to aid post flight analysis and reconstruction of events.
- The rapid development of this FPGA was vital in obtaining massive amounts of data used in understanding critical facets of the mission:
  - the physical environment of deployment
  - Parachute inflation
  - inflated performance of the parachute

MSL Focused Technology Sig Event

MSL Focused Technology Significant Events: Aug. 2004
Subsonic Parachute Development

JPL-led Subsonic Parachute Development team has successfully completed the first of three high altitude drop tests of a 110 ft. diameter ringsail parachute designed and built by Pioneer Aerospace in order to characterize and demonstrate performance at representative Mars conditions. Test setup is a standard National Scientific Balloon Facility (NSBF) setup involving 11.87 Million cu. ft. balloon launch from 120,000 ft altitude.

http://marstech.jpl.nasa.gov/news/paraDev.cfm

Conclusion

- **Use of COTS Annapolis Wildcard and Re-use of existing Verilog module (IMU interface, RS422 interface) enabled quick design turnaround.**

- **Memory Partition Spreadsheet enabled quick design modifications as data sizes and rate requirements evolved.**

Acknowlgements

- HASP Instrument Task Lead – Edward Konefat
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- Research Assistant – Marc Helou

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Related Publications

1. **Opportunities and limitations in low earth subsonic testing for qualification of extraterrestrial supersonic parachute designs**
   A. Steltzner, J. Cruz, R. Bruno, Dr. R. Mitcheltree
   NASA Jet Propulsion Laboratory
   AIAA Aerodynamic Decelerators Conference , May 20-22, 2003
   Parachutes for Mars and other planetary missions often need to operate at supersonic speeds in very low density atmospheres. Flight testing of such parachutes at appropriate conditions in the Earth's atmosphere is possible at high altitudes.
   http://techreports.jpl.nasa.gov/2003/03-1289.pdf
   Updated/Added to NTRS: 2004-08-20

2. **Mars Science Laboratory: entry, descent and landing system overview**
   J. W. Umland, A. Chen, E. Wong, T. Rivellini, Dr. B. Mitcheltree, A. Johnson, B. Pollard, M. Lockwood, C. Graves, E. Venkataphy
   NASA Jet Propulsion Laboratory
   2004 IEEE Aerospace Conference , March 6-13, 2004

   http://techreports.jpl.nasa.gov/2003/03-2088.pdf
   Updated/Added to NTRS: 2004-09-03

3. **High Altitude Test Program for a Mars Subsonic Parachute**
   R. Mitcheltree,PhD., R. Bruno, E. Slimko, C. Baffes, and E. Konefat, NASA Jet Propulsion Laboratory; and A. Witkowski, Pioneer Aerospace Corporation, South Windsor, CT
   AIAA-2005-1659
   18th AIAA Aerodynamic Decelerator Systems Technology Conference and Seminar, Munich, Germany, May 23-26, 2005