High Altitude Subsonic Parachute Field Programmable Gate Array

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Overview

This paper describes a rapid, top down requirements-driven design of an FPGA used in an Earth qualification test program for a new Mars subsonic parachute. The FPGA is used to process and store data from multiple sensors at multiple rates during launch, ascent, deployment and descent phases of the subsonic parachute test.
The Mission

• The current Mars (Viking-heritage) supersonic parachute system was qualified in and used since 1972.

• New designs are under way that enable landing larger payloads for the upcoming proposed Mars missions.

• The approach of using a subsonic parachute in combination with the existing Viking parachute design as a two-stage system builds on the proven design and extends the payload mass capabilities to a new generation of missions.

• The subsonic parachute must first be tested.
Test Program

- Three high altitude subsonic drop tests were conducted in the fall of 2004 from Ft. Sumner, NM. A 12 million cubic foot helium balloon used to raise the test article to 120,000 ft altitude was launched and operated by the National Science Balloon Test Facility (NSBF).

- The FPGA is used to receive, compress, format, and write to memory 10 hours of deployment, inflation, and inflated performance of the subsonic parachute.
Test Instrumentation

30 V / 30 Amp-Hour Battery

Discrete Signals:
• POR
• Camera Turn on
• Low/High speed record
• Release trigger

Digital PCU

GPS

IMU

ANT

Driver / Receiver Board

RS422 RCV

RS422 RCV

RS422 RCV

+ 5 V

+ 15 V

- 15 V

+ 12 V

+ 5 V

RS232 RCV

RS422 RCV

OC

OC

OC

ISO RS422

2 x Analog Board(s)

Signal Cond.

Signal Cond.

Signal Cond.

Signal Cond.

Signal Cond.

Signal Cond.

ADC

AMUX

30 V

16.0 V

CPU

Computer

Card Bus

Solid State Flash

PCMCIA FPGA 1/F

Digital

Digital

• FUNCTIONAL ONLY
• No Assumptions on Grounding or Isolation should be inferred from this diagram

KOWALSKI 5

MAPLD05/F154

30 V

PCU

+ 5 V

+ 15 V

- 15 V

+ 5 V

+ 15 V

- 15 V
Requirements

- Four months to deliver the FPGA (design and verification).

- Low mass, low power, Xilinx Virtex-E in PCMCIA form factor module.

- The memory storage is designed for 10-hours test duration. Sufficient margin (100%) is included to account for possible delays in launch, or an atypical, prolonged period at the release altitude, total capacity 1GByte.

- The instrument set is designed and tested to operate and survive:
  - high altitude, low pressure environment extreme conditions
  - 1 day after touch down without data loss
The instrumentation subsystem must operate over:

- **2.5 hour delay** launch pad
  - 20 deg. C (ground)

- **2 hour ascent**
  - -54 deg. C (to 10,000 ft)
  - -20 deg. C (120,000 ft)

- **4 hour drift at altitude**
  - -20 deg. C (120,000 ft)

- **1 hour descent**
  - -20 (120,000 ft)
  - -54 (10,000 ft)
  - 38 deg. C (ground)

A total of **10 hours** from the last time it is accessed until ground impact.

Adapted from: NASA Reference Publication 1350

The Natural Space Environment: Effects on Spacecraft, Nov. 1994
FPGA Implementation

• A COTS Xilinx Virtex-E FPGA embedded on a PCMCIA with a SRAM unit and PCI bus interface.
  – 26 Useable External I/Os
  – 52% Flipflops were utilized in this application
• Software on a SBC reads buffered SRAM using Direct Memory Access (DMA) to store the data in a flash disk.
Simulator / Synthesis Tools

- **ModelSim XE**
  - Version 5.6
  - Simulation and Verification
- **Visual C++ 6.0**
  - Used to compile host application
- **Xilinx Webpack 5.2i**
  - Place and Route
  - Maps design into target
- **Annapolis Microsystems Library**
  - Script Files
  - Cardbus bridge
  - Local Address and Data modules
- **Synplify Pro**
  - Version 7.2
  - Tried to use 7.5 and we had problems compiling
  - Synthesis: map of logic to FPGA technology
  - Generates EDIF File from Verilog and VHDL code
VHDL Wrapper

- Developed using Annapolis Microsystems library
  - Control DMA word transfers to external flash disk
  - Control of Local Address Data bus
  - Mapped the external I/O pins
Development Approach

• The FPGA design is guided by a spreadsheet of memory partitions based on data rates from each sensor.

• Accumulators are used to compress the high rate IMU data.

• A prioritized queue is used to control the servicing of received data from multiple sources.

• The memory transfer rate is high enough to allow single depth buffering.
FPGA Core Organization

HASP Memory Interface

100 Hz
acc4

100 Hz

MEM_INTERFACE

400 Hz

IMU_IF

13 words
13 words + co

ADC_IF

start_adc
adc1_data[23:0]
adc_dv

16 dbl samples

GPS_IF

gps_data[7:0]
gps_dv

one_pps

10 bytes

MAG_IF

mag_data[7:0]
mag_dv

6 bytes

STA_REG

IMU_EOD

100 Hz

LAD_MUX

MEM_WR

MEM_ADDR

MEM_DATA

MEM_REQ

ACK

Dwn_Link

40 Kbps

88+ bytes @ 50 Hz

3600 wds/sec

40 Kbps
## Rate-Based Memory Partition

### HASP Memory Partitioning

<table>
<thead>
<tr>
<th>pkts</th>
<th>wds/pkt</th>
<th>partition size</th>
<th>start_dec</th>
<th>hex</th>
<th>end_dec</th>
<th>hex</th>
</tr>
</thead>
<tbody>
<tr>
<td>4440</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>imu</td>
<td>5</td>
<td>22200</td>
<td>1</td>
<td>1</td>
<td>4</td>
<td>22200</td>
</tr>
<tr>
<td>adc</td>
<td>16</td>
<td>71040</td>
<td>22201</td>
<td>6B9</td>
<td>15AE4</td>
<td>93240</td>
</tr>
<tr>
<td>gps</td>
<td>2.5</td>
<td>11100</td>
<td>93241</td>
<td>1C39</td>
<td>5B0E4</td>
<td>104340</td>
</tr>
<tr>
<td>mag</td>
<td>4</td>
<td>17760</td>
<td>104341</td>
<td>19795</td>
<td>65E54</td>
<td>121200</td>
</tr>
<tr>
<td>sta</td>
<td>2</td>
<td>8880</td>
<td>122101</td>
<td>1DCF5</td>
<td>773D4</td>
<td>130980</td>
</tr>
<tr>
<td>last_wr</td>
<td>6</td>
<td>130981</td>
<td>1FFA5</td>
<td>7FE94</td>
<td>130986</td>
<td>1FFAA</td>
</tr>
</tbody>
</table>
Memory Address State Machine

- **Ready**
  - Prioritized memory request servicing.
  - Load `mem_addr` and `mem_data` registers.
  - Set `mem_wr = 1`.

- **Pause**
  - Set `mem_mux_req`.

- **Write**
  - Wait for ack from LAD
  - Test for Partition Max, or increment active buffer address

- **Switch_mem**
  - Index through buffers, capture last address

- **Rdy_sw**
  - Load `last_address ptr` to `mem_addr` and partition last address to `mem_data` registers.
  - Set `mem_wr = 1`.

- **Pause_sw**
  - Set `mem_mux_req`.

- **Write_sw**
  - Wait for ack from LAD
  - Increment `last_addr` buffer address

- Partition max
- Index < 6
ADC Packet

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>pkt_cnt[3:0]</td>
<td>adc_addr[3:0]</td>
<td>adc.1.0 [11:0]</td>
<td>adc.0.0 [11:0]</td>
</tr>
</tbody>
</table>

pkt_cnt : increments, will have the same value for all 16 words in packet.

J. Kowalski
7/9/2004
## IMU Packet

<table>
<thead>
<tr>
<th></th>
<th>Y DELTA VELOCITY</th>
<th>X DELTA VELOCITY</th>
<th>IMU Packet Data Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>imu_data1[15:0]</td>
<td>imu_data0[15:0]</td>
<td>1 Y DELTA VELOCITY imu_data1[15:0] X DELTA VELOCITY imu_data0[15:0]</td>
</tr>
<tr>
<td>2</td>
<td>X DELTA ANGLE</td>
<td>Z DELTA VELOCITY</td>
<td>2 X DELTA ANGLE imu_data3[15:0] Z DELTA VELOCITY imu_data2[15:0]</td>
</tr>
<tr>
<td>3</td>
<td>Z DELTA ANGLE</td>
<td>Y DELTA ANGLE</td>
<td>3 Z DELTA ANGLE imu_data5[15:0] Y DELTA ANGLE imu_data4[15:0]</td>
</tr>
<tr>
<td>4</td>
<td>MODE BIT/MUX ID</td>
<td>IMU STATUS SUMMARY WD</td>
<td>4 MODE BIT/MUX ID imu_data7[15:0] IMU STATUS SUMMARY WD imu_data6[15:0]</td>
</tr>
<tr>
<td>5</td>
<td>co4sum</td>
<td>MULTIPLEXED DATA WD</td>
<td>5 co4sum MULTIPLEXED DATA WD imu_data8[15:0]</td>
</tr>
</tbody>
</table>
FPGA Verification

Verification Tools & Methodology

- Hierarchical Verilog Simulation.
- Synplify and Xilinx Static Timing Analysis.
- Development Hardware Interface Testing: IMU, GPS, and ADC.
- Flight Model Integration and “End to End” Test at JPL.
FPGA Simulation – IMU write
## FPGA Utilization Statistics

### Logic Utilization

<table>
<thead>
<tr>
<th></th>
<th>Used</th>
<th>Available</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Number of Slice Flip Flops:</td>
<td>3,214</td>
<td>6,144</td>
<td>52%</td>
</tr>
<tr>
<td>Number of 4 input LUTs:</td>
<td>3,510</td>
<td>6,144</td>
<td>57%</td>
</tr>
</tbody>
</table>

### Logic Distribution

<p>| | | | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Number of Occupied Slices</td>
<td>2,824</td>
<td>3,072</td>
<td>91%</td>
</tr>
<tr>
<td># Slices w only related logic</td>
<td>2,824</td>
<td>2,824</td>
<td>100%</td>
</tr>
<tr>
<td>Total Number 4 input LUTs</td>
<td>3,808</td>
<td>6,144</td>
<td>61%</td>
</tr>
<tr>
<td># Slices w unrelated logic</td>
<td>0</td>
<td>2,824</td>
<td>0%</td>
</tr>
<tr>
<td># used as logic:</td>
<td>3,510</td>
<td></td>
<td></td>
</tr>
<tr>
<td># used as a route-thru:</td>
<td>264</td>
<td></td>
<td></td>
</tr>
<tr>
<td># used as Shift registers:</td>
<td>34</td>
<td></td>
<td></td>
</tr>
<tr>
<td># of bonded IOBs:</td>
<td>200</td>
<td>260</td>
<td>76%</td>
</tr>
<tr>
<td># of Tbufs:</td>
<td>1</td>
<td>3,200</td>
<td>1%</td>
</tr>
<tr>
<td># of Block RAMs:</td>
<td>10</td>
<td>32</td>
<td>31%</td>
</tr>
<tr>
<td># of GCLKs:</td>
<td>3</td>
<td>4</td>
<td>75%</td>
</tr>
<tr>
<td>I/O Register bits:</td>
<td>0</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Table 2. From Xilinx Mapping Report
Analog Data Write
Test Results

Ten hours of the data was retrieved from solid state memory to aid post flight analysis and reconstruction of events.

The rapid development of this FPGA was vital in obtaining massive amounts of data used in understanding critical facets of the mission:

- the physical environment of deployment
- Parachute inflation
- inflated performance of the parachute
JPL-led Subsonic Parachute Development team has successfully completed the first of three high altitude drop tests of a 110 ft. diameter ringsail parachute designed and built by Pioneer Aerospace in order to characterize and demonstrate performance at representative Mars conditions. Test setup is a standard National Scientific Balloon Facility (NSBF) setup involving 11.87 Million cu. ft. balloon launch from 120,000 ft altitude.

Conclusion

• Use of COTS Annapolis Wildcard and Re-use of existing Verilog module (IMU interface, RS422 interface) enabled quick design turnaround.

• Memory Partition Spreadsheet enabled quick design modifications as data sizes and rate requirements evolved.
Acknowledgements

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- HASP FPGA Design Lead - James E. Kowalski
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- SBC C++ HASP invocation and control – Dr. Konstantin Gromov
- HASP FPGA VHDL wrapper – Dr. Konstantin Gromov
- MER IMU interface module – Jason Gates
- HASP ADC interface – Keizo Ishikawa
- HASP Downlink Serial Transmit - Tsan-Huei Cheng
- HASP Principal Investigator – Robert Mitcheltree
- C++ Postprocessing Data formatter – James Kowalski
- Research Assistant – Marc Helou

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Related Publications

1. Opportunities and limitations in low earth subsonic testing for qualification of extraterrestrial supersonic parachute designs
   A. Steltzner, J. Cruz, R. Bruno, Dr. R. Mitcheltree
   NASA Jet Propulsion Laboratory
   Parachutes for Mars and other planetary missions often need to operate at supersonic speeds in very low density atmospheres. Flight testing of such parachutes at appropriate conditions in the Earth’s atmosphere is possible at high altitudes.
   Updated/Added to NTRS: 2004-08-20

2. Mars Science Laboratory: entry, descent and landing system overview
   J. W. Umland, A. Chen, E. Wong, T. Rivellini, Dr. B. Mitcheltree, A. Johnson, B. Pollard, M. Lockwood, C. Graves, E. Venkataphy
   NASA Jet Propulsion Laboratory
   2004 IEEE Aerospace Conference, March 6-13, 2004
   Updated/Added to NTRS: 2004-09-03

3. High Altitude Test Program for a Mars Subsonic Parachute
   R. Mitcheltree, PhD., R. Bruno, E. Slimko, C. Baffes, and E. Konefat, NASA Jet Propulsion Laboratory; and A. Witkowski, Pioneer Aerospace Corporation, South Windsor, CT
   AIAA-2005-1659
   18th AIAA Aerodynamic Decelerator Systems Technology Conference and Seminar, Munich, Germany, May 23-26, 2005