

# **X2000 Power System Electronics Development**

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## *Abstract—*

The X2000 Power System Electronics (PSE) is a Jet Propulsion Laboratory (JPL) task to develop a new generation of power system building blocks for potential use on future deep-space missions. The effort includes the development of electronic components and modules that can be used as building blocks in the design of generic spacecraft power systems. All X2000 avionics components and modules are designed for use in centralized or distributed spacecraft architectures. Specifically, the power system components are being developed for a low voltage (30V) power management and distribution system. The power system components are applicable on deep-space missions beyond Mars orbit that demand reliable long-life circuitry (usually greater than 10 years). Missions to Jupiter and its moons demand radiation tolerant components. These two combined challenges require improvements in the lifetime and radiation tolerance of electronic components and parts used in the design and fabrication of power-system modules. The current state-of-the-art, low-voltage, power-system components are limited to environments less than 300 Krad total ionizing dose. To create a power system capable of performing in an extreme radiation environment the X2000 PSE has taken the approach of developing a set of Application Specific Integrated Circuits (ASICs) that are radiation tolerant to >1 Mrad. JPL had teamed with Boeing (ASIC Design) and Honeywell (ASIC foundry) under the X2000 Integrated First Delivery Project. During that past effort the team developed an analog ASIC cell library to be used for future ASIC designs. By combining the analog library developed by Boeing and the digital circuit cells developed by Honeywell, mixed-signal ASICs for power applications can be designed and fabricated. Using mixed-signal ASICs for power-system design can reduce the number of components necessary for a system. By using components that are inherently radiation hard, less shielding is required and higher reliability is achieved, resulting in overall mass and volume reduction. This result is beneficial to power-system architects who are constrained by spacecraft volume and mass requirements.

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## I. Introduction

The X2000 Power System Electronics (PSE) Development is a Jet Propulsion Laboratory task developing a new generation of power system building blocks for potential use on future deep space missions<sup>1</sup>. The development approach has been to partition the power system architecture into functional building blocks that can be developed to meet the environmental requirements of deep space missions. Each building block is assessed on the criticality of the function and the number of times the function is repeated throughout the power system.

The X2000 PSE has been functionally partitioned into a power control function, power distribution function and house-keeping supply function. Each function has been subdivided into building blocks where the some of the common building blocks will be used across the functional boundaries. The functional elements are shown in Figure I-1.

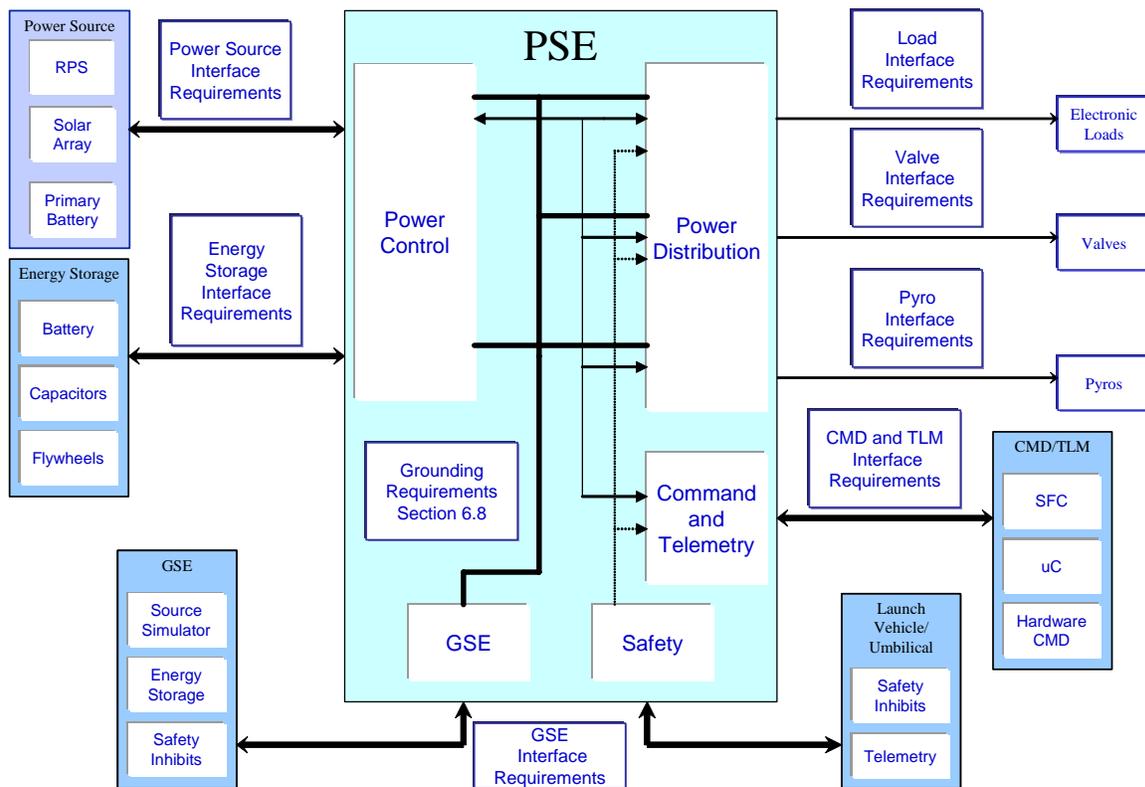


Figure I-1: PSE Functional Block Diagram

Based on the functional partitioning, some building blocks were identified and developed. Each building block would be available for the next higher level of integration. The different levels of building blocks are shown in Figure I-2. Products exist at all levels for use on multiple missions. The lowest level is the intellectual property level of library cells, and software code. A level above that is at the ASIC or module level where the complete part can be used in a function. The next level is the board level where the size of the board and overall functionality can be used depending on the packaging requirements of the mission. For example a probe might require custom packaging in order to reduce the overall system mass. Use at the assembly level will bring the most benefit to the mission by reducing cost and risk.

Each mission needs to assess at what level can inherit in order to meet the requirements. Mars mission might only use the intellectual property and implement the function in field programmable gate arrays due the shorter life and

lower radiation. On the other extreme, the Europa Orbiter mission might use the assembly level to take advantage of the radiation hardness and compact packaging.

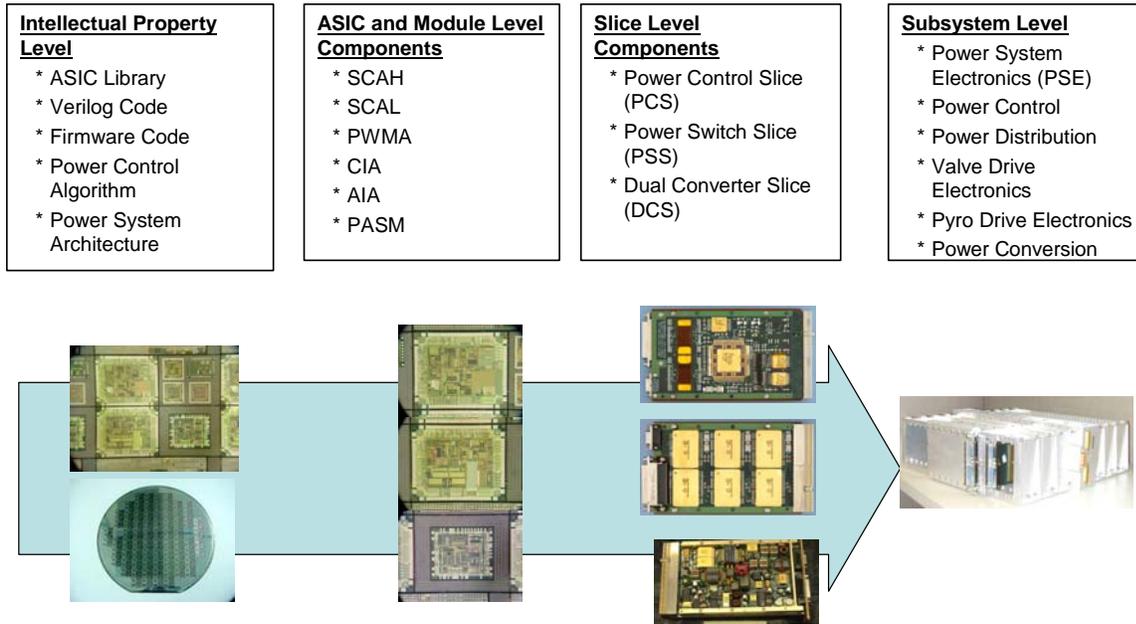


Figure I-2: X2000 PSE Development Approach

## II. Power System Architecture

There are several power system architectures that would apply to deep space missions. This paper will discuss two examples. The first is a direct energy transfer power system with a Radioisotope Thermoelectric Generator (RTG) power source and battery as energy storage. The system is single-fault tolerant with fault containment regions at the board level. An example of a possible Europa Orbiter power system architecture is in Figure II-1.

Europa Orbiter Power System Block Diagram

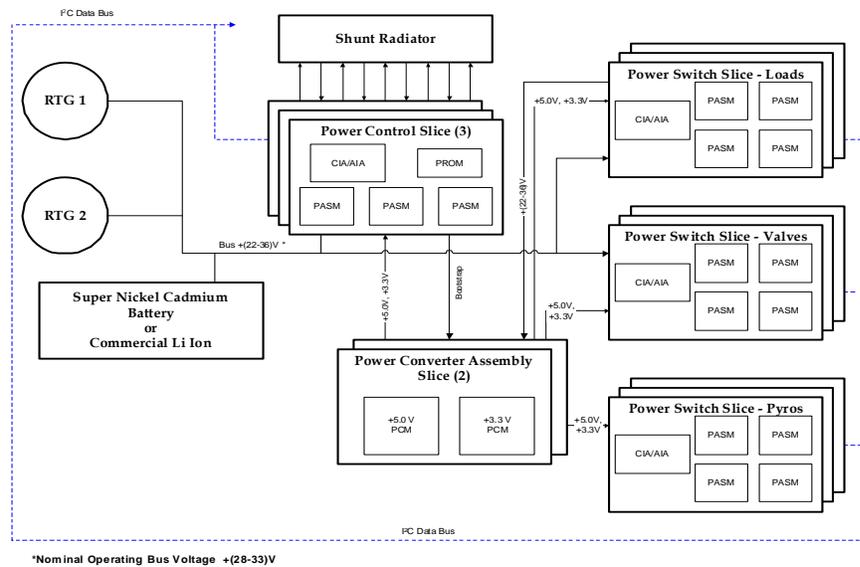
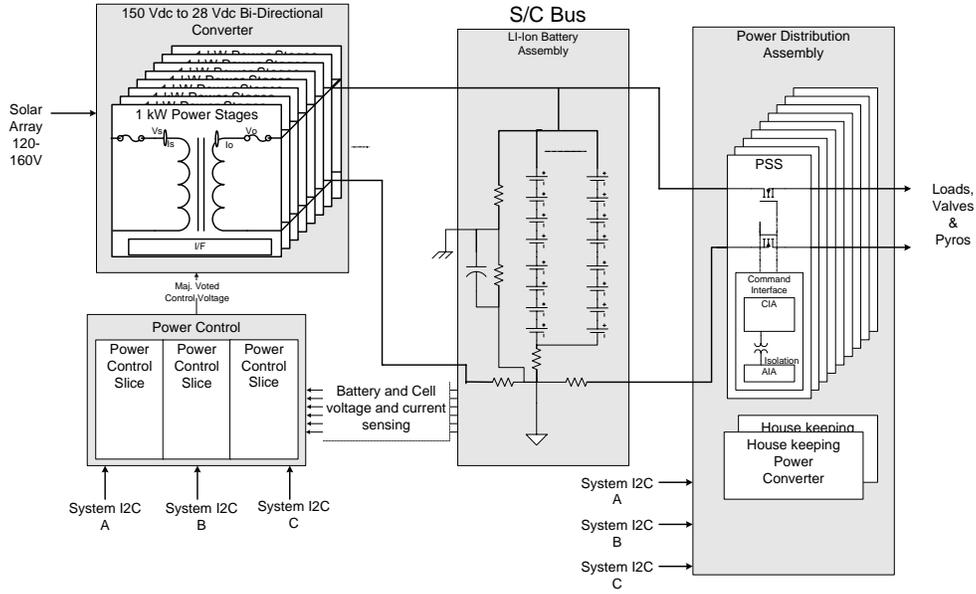


Figure II-1: Power System Architecture for the Europa Orbiter



**Figure II-2: Solar-Electric-Propulsion Power System Architecture**

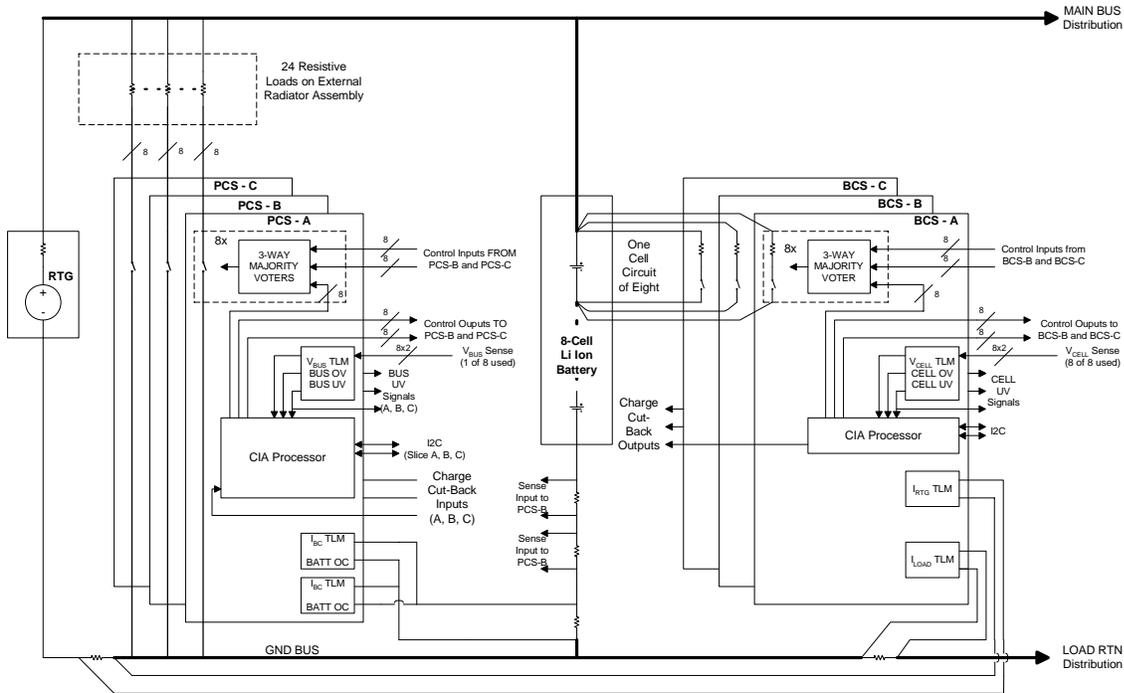
The next power system architecture, shown in Fig II-2, is for a Solar-Electric-Propulsion mission with a battery for energy storage. This architecture is single-fault tolerant at the system level and “N+K” redundant at the power-stage level, where “N” is the number of power stages required and “K” is the number of redundant power stages. This architectural approach is relevant for larger power missions where block redundancy incurs too much of a mass penalty and the reliability of the power stages is lower than the rest of the system components.

### A. Power Control Function

The power-control function provides the power-bus regulation, energy-storage charge and discharge control, and a command interface to the spacecraft C&DH. The power-control function will change based on the power-source and energy-storage technology selected for that mission. The key to this development was to reduce the amount of hardware changes and provide a method for software changes for updating to the control algorithm for a particular source or energy storage. The building blocks for power control were broken up into a command interface that can run different algorithms, a switch function that can switch shunts of a shunt regulator or switch strings of a solar array. Battery cell protection is required for a Li-Ion Battery and the same switching function is used to bypass the cell. The configuration of a power control slice and battery control slice are shown in Figure II-3.

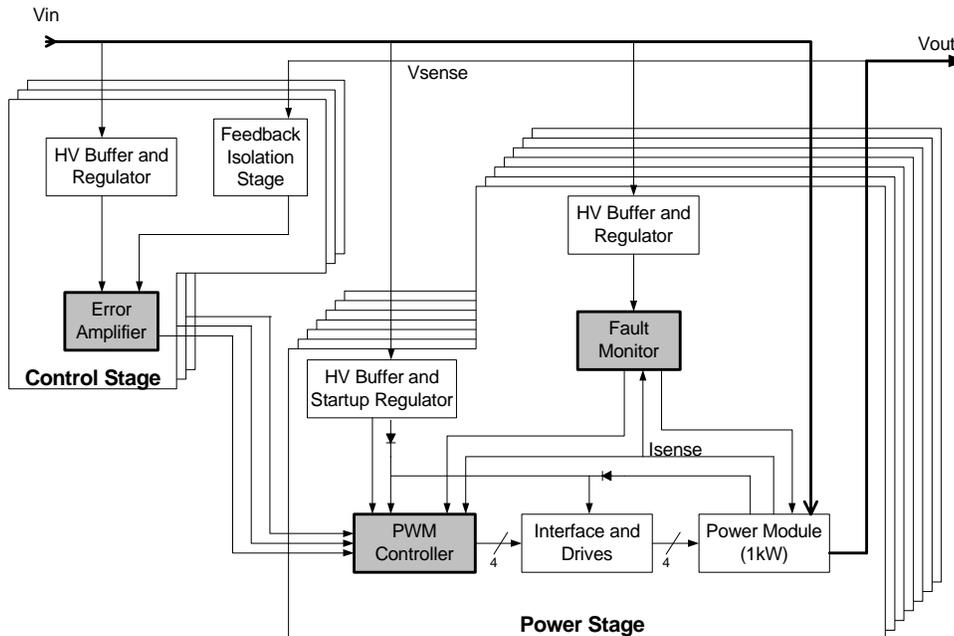
The algorithm for power control is contained in the command interface building block and can be changed from mission to mission based on the source and energy storage technology. Set-points for the shunt regulator, charge control and cell protection can be changed in flight depending on the limits defined in the algorithm.

The Power Control Slice (PCS) is developed to provide a fault tolerant shunt regulator or solar array switching function. A slight variation can be used to bypass battery cells for Li-Ion cell protection. Each function is designed to be single-fault tolerant.



**Figure II-3: Power Control Functional Block Diagram**

Power Control for the SEP power system requires a down converter in power control to step down the voltage because most of the power from the array is for the Electric Propulsion. The rest of the spacecraft does not require as much power. The down converter power stages are “N+K” redundant with the feedback control as single-fault tolerant.



**Figure II-4: SEP Power Control Functional Block Diagram**

## B. Power Distribution

Power distribution for the Europa and SEP power architecture is the same. The requirements for the power distribution function is to provide load switching, valve drivers, and pyro firing. The fault protection is driven by the load switching requirement. The command interface is driven by the valve drivers and pyro firing requirements. The safety interlocks are handled at the board level for the valve drivers and pyro firing circuits. The functional block diagram of the power switch slice is shown in Figure II-5.

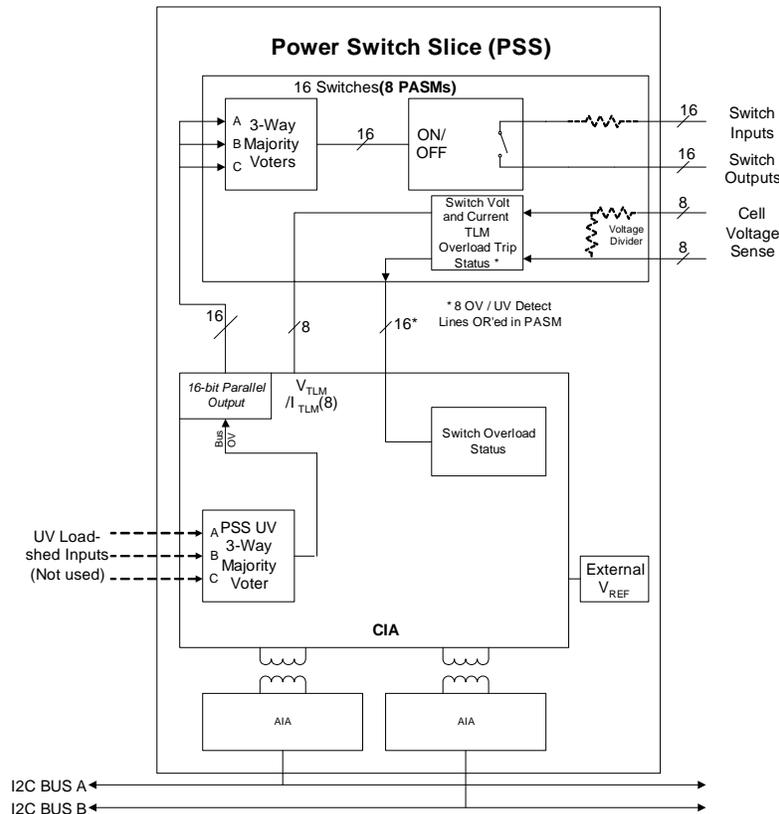


Figure II-5: Power Switch Slice Functional Block Diagram

## III. Power System Building Blocks

The previous section describes the functions required in two example power-system architectures. The building blocks that are used to provide these functions are described below. Five mixed-signal ASICs and one module provide the power system functions. Two mixed-signal ASICs, called Switch Control ASIC High (SCAH) and Low (SCAL), provide the power-switch control function. These ASICs are packaged in the Power Actuation and Switching Module (PASM). The PASM is used to provide all of the switching functions for the loads, valves, and pyro devices of the spacecraft.

Another building block is the command interface, which is provided by two mixed-signal ASICs, isolation transformers, an oscillator, and an external reference. The core of the command interface is in the Command Interface ASIC (CIA). This ASIC contains an embedded microcontroller programmed to provide the Inter-Integrated Circuit (I2C) data bus interface. All of the boards have the same command interface function. The Power

Control Function utilizes external memory to provide the power-control algorithms. Two Analog Interface ASICs are used to provide the physical I2C data bus interface.

The last building block is the Pulse-Width-Modulator ASIC (PWMA). The PWMA is a mixed-signal ASIC that provides the closed-loop control of a switching power converter. The PWMA is used in the housekeeping supplies to provide the required voltages: 3.3Vdc for digital, and 5.0 Vdc for analog functions. The PWMA also provides the fault protection and multiple control loops for the Step-Down Converter in the SEP power-system architecture.

### A. Switch Control ASICs (SCAH and SCAL)

The SCA-High and SCA-Low are designed as a chipset to control one solid-state switch for general switching purposes. Figure III-1 illustrates both ASICs connected to a power switch. The chipset is fabricated on the Honeywell foundry HX2000, 0.8 $\mu$ m, Silicon on Insulator (SOI) process and the first ASICs were completed in June 2003. The chipset has the capability to be powered by redundant 5V power supplies. Power-on-Reset (POR) circuitry was designed to keep the circuit in a known state during power on and power cycling. The ASICs have the capability of providing analog telemetry for switch current and switch voltage. Logic command inputs are compatible with 3.3V & 5.0V standard CMOS logic levels. Currently the chipset is designed to interface with a 100V MOSFET appropriate for use in most low voltage applications. However, with adequate isolation between the interfaces of the two chips it can be used in higher switch voltage applications.

The first pass of the SCAs were tested in PASM brassboards and prototype PASM. A few changes were identified and the changes were made to the metal layers of the wafers that were on hold at Honeywell. The set of modified ASICs has been verified and is currently in fabrication of the second pass of the PASM.

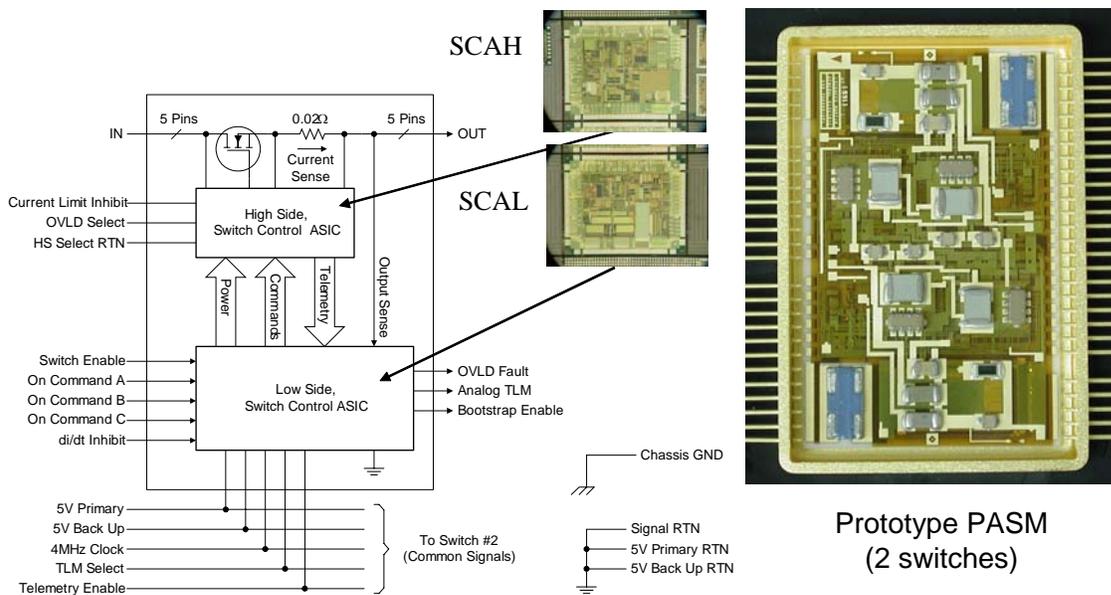


Figure III-1: Switch Control ASICs and PASM Building Blocks

### B. Power Actuation and Switching Module (PASM)

The PASM is a solid-state, general-purpose switching module. Each PASM has two independent MOSFET power switches that can be used in various configurations. Figure III-1 contains a picture of a prototype PASM. These switches can be used in a series or parallel configuration and as high-side or low-side connection to the load, thus, providing greater flexibility to the system architect when designing the power system. The PASM package design is based on a new technology that enables higher density packaging of electronic components when compared to chip-on-board or hybrid packaging techniques. JPL's industry partner Lockheed Martin – Commercial Space Systems (LM-CSS in Newtown, PA) designed the PASM. The Power High-Density-Interconnect (Power HDI) packaging technique developed by General Electric is being used to fabricate the PASM. Some of the key

features of the PASM are over-current trip, current limiting, soft start (closed-loop di/dt control), switch current and voltage telemetry, and back-EMF suppression for inductive loads. The over-current trip and current-limit capability of the PASM have high and low settings. Current will be limited to a maximum of 6.5A on the high setting and 2.5A on the low setting. The individual switches are command resettable once tripped. In addition switch status (on/off) and overload fault telemetry output is available. Nominal limit for di/dt control is 7.5 A/ms. The PASM is capable of driving regular loads (e.g., heaters, traveling-wave tube amplifiers, spacecraft computers), pyro devices, and inductive loads (thruster valves, motors). The SCA control circuitry allows each switch to be configured appropriately to match the needs of the load. For example, to configure a PASM switch to drive a pyro device one would disable the di/dt, set the current limit to 5.0A, and enable the over-current trip so that when switched on the pyro initiator is given a 6.5A pulse for a maximum of 31ms before the switch trips off.

Prototype HDI PASM were fabricated and tested the first half of 2004. The PASM package is 1.0 by 1.6 inches and contains two independent power switches. The tight package significantly reduced the noise sensitivity found during packaged SCA testing. The switches were tested with resistive loads at various bus voltage levels and various load values. Switched voltage and current waveforms were clean and followed the di/dt ramp as expected. Testing was performed with the switch configured as a high-side and low-side switch. When driven into a load greater than the current limit, the output current was held at the current-limit value until the switch tripped off. Pyro initiator switch testing with di/dt disabled performed perfectly. Switching into inductive or capacitive loads with di/dt control enabled performed as expected for the representative values that have been tested to date. Testing is ongoing at LM-CSS. Testing of the switch commands and telemetry performed as expected. The PASM current-limit levels and shut-down response times were as expected. Combining the PASM with the AIA and CIA on a single card is currently in progress..

### C. Analog Interface ASIC (AIA)

The AIA provides power-return isolation between the data buses and the power system electronics. The AIA receives and transmits commands to the CIA via two I<sup>2</sup>C transceivers. Figure III-2 exhibits the block diagram of the Command Interface. Transformers are used to isolate the signals between the AIA and the CIA. An internal 6.29 MHz clock is designed on chip with the capability of interfacing with an optional external clock. An on-chip oscillator watchdog forces the AIA into a fail-silent mode in the event of an oscillator failure. This chip is powered by redundant 3.3V power sources. A power-on-reset signal must be provided by an external source such as a power converter. Like the SCA, it is fabricated on the Honeywell HX2000 process, which makes the chip 1Mrad hard. The first ASICs were produced June 2003. Prototype ASICs were packaged and have been tested individually and with the Command Interface ASIC. The AIA passed all functional verification tests.

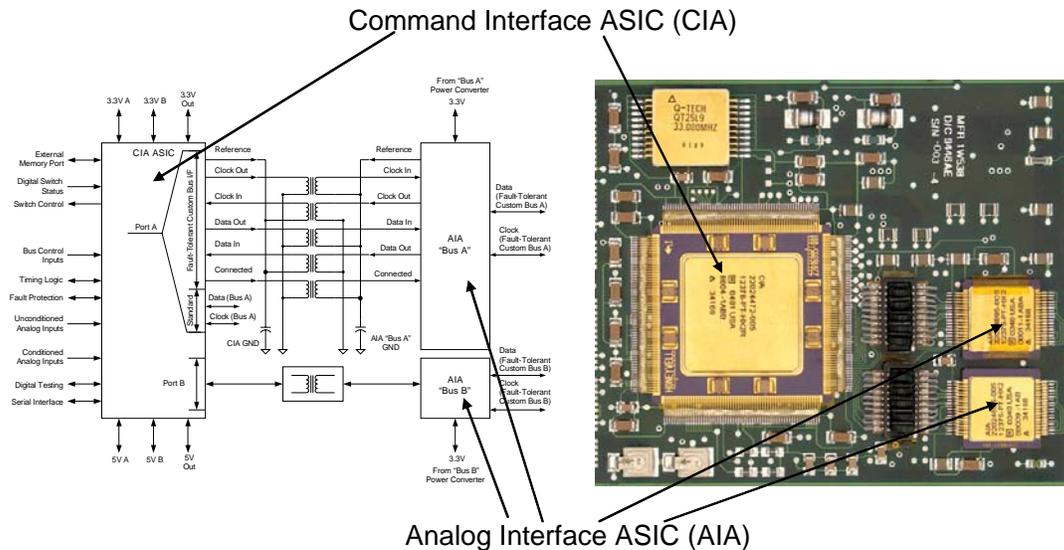


Figure III-2: Command Interface Building Block

#### D. Command Interface ASIC (CIA)

The CIA is a micro-controller that is based on a M8051 core processor with multi-frequency operation<sup>2</sup>. The CIA has been fabricated on the Honeywell HX3000 0.3 $\mu$ m, SOI process line. The CIA has two modes of operation, one at 16.5 MHz and another at 8.25 MHz. In addition it has a sleep mode for low power consumption. It can interface with the spacecraft computer via an I<sup>2</sup>C standard data bus. The design provides two I<sup>2</sup>C ports, which allow communication on primary and redundant data busses. There is 8KB and 12KB of program and data memory respectively available on chip. The CIA also has the capability to boot up from an external ROM and store data to a larger external memory device. The external ROM feature allows user specific programming of the micro-controller. The chip can be powered by two 5.0V sources for the analog circuitry and two 3.3V sources for the digital circuitry. Both voltages are then cross-strapped internally for redundancy. At least one of each voltage is needed for proper CIA functionality. Internal power-on-reset (POR) circuits are also designed to hold the circuit in a known state during initial power on and power cycling. The CIA is designed to work with the other building blocks of the power system, and as such contains a multiplexed 8-bit analog-to-digital converter, which processes the analog telemetry from the PASM. The CIA has the ability to measure bus voltage and current directly across an external resistor network and report this telemetry on the I<sup>2</sup>C bus. An internal watchdog timer in the design forces a fail silent state on the I<sup>2</sup>C bus in the event of a failure.

Prototype versions of the AIA and CIA have been tested at JPL. Functionality of each block of has been targeted by a series of tests. All blocks have successfully passed performance testing at ambient temperature. A simulated spacecraft computer was used to send I<sup>2</sup>C commands and receive telemetry back from the test card containing two AIAs and one CIA. Each time the automated test is run approximately 2.3 million I<sup>2</sup>C commands are sent and a telemetry status response is received for each command. Tests were run using primary and redundant I<sup>2</sup>C busses; all commands resulted in the expected telemetry and power-switch status indication. The fail-silent and power cross-strap functions of both ASICs performed as expected.

#### E. Pulse Width Modulator ASIC (PWMA)

The PWMA is currently in design<sup>3</sup>. The goal of this effort is to design a single ASIC that can be used as the PWM for a family of radiation-hardened power converters. Taking advantage of the analog cell library used in the design of the other ASICs along with the same design team and modeling tools, the PWMA design has a high likelihood for first-pass success. The ASIC will contain necessary functions for power conversion such as pulse-width modulation, synchronous rectification, voltage references, and FET drivers. As a dc-dc converter building block, the PWMA will accommodate isolated and non-isolated converter designs using spacecraft input bus voltages as large as 130V. The design of the ASIC is currently being performed by JPL, and fabrication is planned for late 2005.

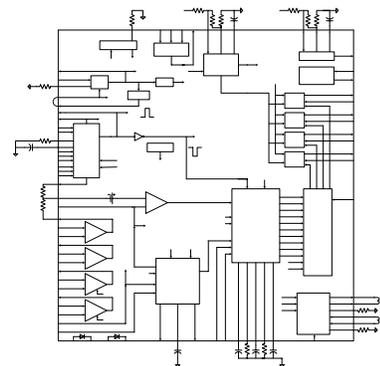


Figure III-3: PWMA Block Diagram

### IV. Summary

The X2000 PSE task is to develop electronic components that are highly reliable and radiation hard for future spacecraft power systems. These components can be used to architect a centralized or distributed power system for future long-life, deep-space missions, such as missions to Jupiter or Saturn. Using these components a power system can be designed to have a regulated or non-regulated power bus. In addition, a power system designer is not limited in the types of power sources and energy-storage devices that can be selected. These components have the flexibility to meet the needs of many power-system architectures. Commanding of the power system is achieved through an I<sup>2</sup>C data bus. Power distribution to a variety of loads such as heaters, pyros, and propulsion valves can be achieved by using the same generic building blocks being developed. The basis of the building blocks being developed is a set of five mixed-signal ASICs (AIA, CIA, SCAH, SCAL, and PWMA) and one power-switching module (PASM). To date four ASICs and a switching module have been designed, fabricated, and preliminary test results have been gathered.

## Acknowledgments

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## References

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<sup>2</sup> Ruiz, I., "Open-Systems Architecture of a Standardized Command Interface Chip-Set for Spacecraft Power Switching and Control," *2nd AIAA International Energy Conversion Engineering Conference*, Providence RI, 16-19 Aug 2004, Paper Number: AIAA-2004-5691.

<sup>3</sup> Wester, G., Carr, G., Deligiannis, F., Jones, L., Lam, B., Sauers, J., Haskell, R., Mulvey, J., "The Pulse-Width-Modulator ASIC Development for Deep Space Missions," *2nd AIAA International Energy Conversion Engineering Conference*, Providence RI, 16-19 Aug 2004, Paper Number: AIAA-2004-5694.