A Chip and Pixel Qualification Methodology on Imaging Sensors

Yuan Chen, Steven M. Guertin, Mihail Petkov, Duc N. Nguyen, Frank Novak² Jet Propulsion Laboratory, MS 303-230, 4800 Oak Grove Drive, Pasadena, CA 91109 ²NASA Langley Research Center, MS 468, 5 North Dryden St., Hampton, Virginia 23681

ABSTRACT

This paper presents a qualification methodology on imaging sensors. In addition to overall chip reliability characterization based on sensor's overall figure of merit, such as Dark Rate, Linearity, Dark Current Non-Uniformity, Fixed Pattern Noise and Photon Response Non-Uniformity, a simulation technique is proposed and used to project pixel reliability, which is directly related to imaging quality, and provide additional sensor reliability information and performance control. [Keywords: CMOS Active Pixel Sensors, PD-APS, Imaging Sensor Reliability, Pixel Reliability.]

INTRODUCTION

Imaging sensors of different varieties are widely used in commercial and scientific applications. Comparing to chargecoupled device (CCD) image sensors, CMOS active pixel sensor (APS) imagers are fabricated in standard CMOS processes and therefore make it possible to integrate the timing and control electronics, sensor array, signal processing electronics, analog-todigital converter (ADC) and full digital interface on one chip to achieve a cost-effective highly integrated and highly compact imaging system, i.e. camera-on-a-chip, by utilizing the same design techniques that have been developed over the years for low-power CMOS digital and analog circuits.

There have been extensive research efforts to enhance the performance of the CMOS APS imaging sensors by adopting more robust digital/analog circuit designs, sampling techniques, imaging processing technology and advanced semiconductor fabrication technologies [1-9].

On the other hand, few studies have been concentrated on the reliability or qualification of the imaging sensors. It is taken for granted that the reliability of the imaging sensors should be automatically guaranteed when the semiconductor process technologies fabricating the imaging devices have been qualified. However, unlike memory chips where failed bits can be detected by functional testing and easily recognized as bad bits, pixels of the imaging sensors can be either uniformly degraded or becoming "hot" pixels. In both cases, these will cause imaging problems or decrease imaging quality.

In the effort of qualifying a photodiode-type (PD) CMOS APS imaging device for one of our space mission applications, we have developed a qualification procedure and reliability analysis approach for imaging sensors. It should be noted that the environmental, mechanical and packaging evaluation procedures and tests are also part of the qualification plan and practice, but are not addressed here. In addition, the results of the radiation impact, including Gamma, proton and heavy ion radiation studies on the imagers were presented in [10].

In this paper, a qualification methodology on imaging sensors is presented. The experimental details of the accelerated life

testing will be described first, along with the reliability characterizations on the imaging sensors. Then, the projection for overall chip reliability and a simulation approach developed to correlate the pixel reliability to image quality will be presented, followed by discussion and summary.

EXPERIMENTAL DETAILS

The image sensor is photodiode-type CMOS active pixel sensor imaging system on chip, designed by Jet Propulsion Laboratory and manufactured by a standard commercial CMOS production line. The imager is a 512 by 512 photodiode pixel array, which can randomly access any window in the array from 1 pixel by 1 pixel all the way to 512 pixels by 512 pixels in any rectangular shape. Figure 1 gives a schematic of the active pixel sensor cell.



Figure 1. Schematic of the photodiode-type active pixel sensor cell.

Light into the photo-diode generates a small current proportional to the light intensity and photo-diode area. Due to this small photo current, the nMOS transistor (M1) operates in weak inversion. In this region, the gate to source voltage depends logarithmically on the drain current with a constant slope independent on the technology and being equal to kT/q, as shown in the following simplified expression for the gate-source voltage for a transistor working in its weak inversion region [3-4,11]:

$$V_{gs} = \frac{kT}{q} \ln(\frac{L}{W} \frac{I_d}{I_{d0}}) + V_{ih}$$

where V_{gs} is the gate-source voltage, I_d is the drain current or the photo current, I_{d0} is the I_d at the on-set of weak inversion, W and L are the width and length of the channel of the transistor, T, k are the temperature and the Bolzmann constant, respectively. Therefore, the pixel structure yields a continuous signal that is proportional to the instantaneous light intensity.

Because of the characteristic deviation of the active transistor M1 in the pixel cell, non-uniformity among pixels is expected and therefore the following parameters are some important figures of merit for imaging sensors. Fixed pattern noise (FPN) is the variation from pixel to pixel when the imager operated as normal with no light input. The FPN is typically measured using the full array. Photon Response Non-Uniformity (PRNU) is the gain difference between pixels and it is typically taken with a field at approximately 50% of full well. Dark Current is the thermally generated electrons discharging the pixel just as if a photon had hit the pixel. Dark Current Non-Uniformity (DCNU) is the leakage difference between pixels with a dark field over a long integration time. All those parameters are functions of temperature and measured during the accelerated testing. Also, Dark Rate and Linearity, defined as the mV/s from Dark Current and PRNU measurements, respectively, were also monitored.

The accelerated testing was performed on the image sensors at elevated bias and temperature levels to accelerate thermally activated failure mechanisms. It is very important to ensure that the highest stress temperature cannot exceed the glass transition temperature for the die attach material of the packages, in our case, 117°C. At the same time, the highest stress voltage at each stress temperature should be within the range when the sensor is still framing and functional. The highest voltage that can be applied on the imager when it is still framing was simulated as 6.8V and later confirmed by experiment.

Following this procedure, the stress conditions were determined as 6.5V at 85°C, 6.5V at 45°C, and 6.0V at 85°C to estimate voltage acceleration factor and activation energy. The limited number of stress conditions in our case results from cost restraints. More bias stress conditions should be used to obtain more accurate bias and temperature acceleration factor estimations.

Shown in Figure 2, the accelerated testing was fully controlled by LabView software running on the personal computer. The image sensors were stressed in parallel and stopped in a pre-set time interval to be monitored one by one for Dark Rate, Linearity, Dark Current Non-Uniformity (DCNU), Fixed Pattern Noise (FPN) and Photon Response Non-Uniformity (PRNU).

During the accelerated testing, the sensors were running at 5 MHz with the clock pulse matching the stress voltage applied on the chips. An LED with color of green carefully designed and tuned on each testing board was served as the light source within the chamber for Linearity and Photon Response Non-Uniformity measurements.

The imagers were tested under each temperature condition and the integration time was chosen for the imagers to reach saturation region during DCNU, FPN and PRNU measurements for a full characterization of the imaging response.



Figure 2. Schematic of the accelerated testing set-up.

CHIP RELIABILITY PROJECTION

For overall VIDI APS chip reliability, Linearity and Dark Rate are the two parameters to be considered since they reflect the overall parametric shift or change on the imaging chips.

Figure 3 shows the linearity characteristics for the worst case/chip as a function of stress time. The black symbol indicates the response at time zero while the white symbol at the end of stress testing. The characteristics trend is representative for all imaging chips under all stress conditions. The plot indicates that it took a longer integration time to achieve saturation when the device was degrading with the stress time.



Figure 3. Linearity changes with stress time, black symbol indicates time zero while white symbol at the end of stress.

This information can be also presented by the slope of the linearity curves before the saturation points. This information is plotted in Figure 4, showing almost linear increasing Linearity slope versus stress time in a log-log scale.



Figure 4. Linearity slope change with stress time.

The behavior of the dark rate is similar to that of Linearity but with smaller degradation rate. Figure 5 shows a representative change of the dark rate slope as a function of stress time in a log-log scale.



Figure 5. Dark rate slope change with stress time.

Since the Dark Rate and Linearity can indicate the overall sensor performance, the sensor's overall chip reliability can be projected based on the Dark Rate and Linearity degradation.

Assuming the Arrhenius model [12]

$$t_{\rm N_o} \sim e^{\beta V_o} e^{\frac{E_a}{kT_o}}$$

where t_{56} is the chip life time at certain failure fraction and is determined to be 0.1% in our case; β , V_{or} , E_{ar} , k and T_o are the voltage acceleration factor, operating voltage, activation energy, Boltzmann's constant and operating temperature in Kelvin, respectively.

The voltage acceleration factor and activation energy were estimated as 0.73 dec/volt and 0.7eV, respectively, for worst case imaging chips. Using 10% degradation for Linearity as the chip failure criterion, the chip life time at 3.3V, 27°C is over 112 years at 0.1% failure fraction with average failure rate of 1 FIT. Life and failure rate can be also generated by using a percentage degradation of Dark Rate as well.

It should be noted that the "failure" criteria used in this reliability projection is defined as a certain level of parametric shifting. Even though this parametric shifting does indicate some performance degradation of the imagers, but it is worthwhile to know that the imagers still frame and function very well when the Dark Rate and/or Linearity reaches 10% parametric degradation. In order to estimate life and failure rate associated with the "imaging failures", pixel reliability needs to be projected.

PIXEL RELIABILITY PROJECTION

In the previous section, chip reliability projection gives reliability indication for a sensor's overall performance as a function of operation time, but it is difficult to relate it to image quality. Therefore, pixel reliability needs to be considered and projected as well.

The Dark Current Non-Uniformity, Fixed Pattern Noise and Photon Response Non-Uniformity measurements during the accelerated testing recorded the distributions of the photodiode reference voltage for each pixel as a function of stress time, in order to calculate the time-dependent DCNU, FPN and PRNU values.

Figure 6 shows an example of the distributions of pixel responses during FPN measurements with FPN suppression function enable at 27°C.



Figure 6. Pixel response during FPN measurement at 27°C.

During the accelerated testing, some of the pixels get "hotter", i.e. more leakier than nominal pixels. In addition, the standard deviation of the pixel distribution becomes a little bit larger with worst case of 2% change and the median of the distribution shifts eventually.

Based on our sample size of 20 CMOS active pixel sensors with 512 by 512 pixels on each imager, we found that the "hot" pixels tend to be randomly distributed across the pixel array and no signature of the pattern can be found. This may indicate that the imaging chips do not have evident process-related defects or stress-induced weak-link pixels. The hot pixel generation rate is slow at the accelerated stress levels. Based on the limited data, the estimated hot pixel generation rate is approximately one and half pixel per decade at 6V 85°C, which gives a rather long projected imager life, assuming a few hot pixels do not have severe impact on imaging quality. Hot pixels do not seem to induce neighboring pixel to degrade faster. While hot pixels can cause image problems but with proper refreshing scheme, the impact of hot pixel on imaging quality can be significantly reduced.

The change of standard deviation of the pixel distribution seems to increase faster at the beginning of the accelerated stress conditions and then saturate at about 2% to 3% change. However, due to the limited data set and small sample size in our study, no further conclusion can be made on the behavior of the standard deviation change.

When the pixel distributions under DCNU, FPN and PRNU measurements have shifted and/or the standard deviations have changed, it indicates the changes of black-white scale for imaging. Therefore, by scaling the time-dependent pixel distribution against the initial pixel distribution, images can be generated either by real pixel distribution data or by projected pixel distributions. The pixel distributions for DCNU, FPN and PRNU did not have significant shift during our accelerated testing and, therefore, the projected distributions based on the trend of pixel degradation can be generated to simulate the image quality.

Figure 7 shows an original image of Saturn. Figure 8, 9 and 10 are the simulated images with 10%, 15% and 20% median pixel degradation, respectively. The degradation on the imaging quality can be seen very clearly from those Figures and so a socalled "imaging failure" can be decided based on the series of images. For example, if Figure 8 is regarded as a imaging fail, a 10% median pixel degradation is then chosen as the failure criterion. In this case, the imager life is at least an order of magnitude longer than the projected imager life using 10% Linearity degradation.



Figure 7. Original image of Saturn



Figure 8. Image with pixel degradation (Median percentage change is 10%).



Figure 9. Image with pixel degradation (Median percentage change is 15%).



Figure 10. Image with pixel degradation (Median percentage change is 20%).

Figure 7-10. Imaging quality simulation with different level of pixel degradation.

Another failure mechanism results from the read-out or I/O circuitry. It happens rather suddenly when the imager stops functional totally. Competing with the pixel degradation, which is a relatively slower process, periphery circuitry failure may be much more severe since it will cause hard failure of the imager.

The pixel reliability is a function of acceptable image quality level and depends on the pixel responses to darkness and light. Acceptable image quality can be chosen based on the same experimental data or simulation results using small degradation percentage increase. It should be noted that the reliability projection based on the worst case parameter degradation, i.e. linearity degradation, gives a much shorter lifetime prediction compared to the pixel projection. Therefore, pixel reliability cannot be overlooked during imaging sensor qualification.

SUMMARY

A reliability study on a CMOS active pixel sensor imaging system is presented. While reliability projection based on imaging sensor's overall parametric performance may provide some insight on the imager performance degradation, pixel reliability projection, either by experimental or by predicted pixel distributions, has to be performed, which can be directly related to imaging quality and can provide additional sensor performance information.

REFERENCES

- E. R. Fossum, "CMOS Image Sensors: Electronic Cameraon-a-Chip", *IEEE Transactions on Electron Devices*, Vol. 44, No. 10, pp. 1689-1697, October, 1997.
- J. Janesick, "Lux transfer: Complementary metal oxide semiconductors versus charge-coupled devices", *Opt. Eng.* 41(6), 1203-1215, June, 2002.
- F. Pardo, et al, "CMOS Foveated Image Sensor: Signal Scaling and Small Geometry Effects", *IEEE Transactions* on *Electron Devices*, Vol. 44, No. 10, pp. 1731-1737, October, 1997.
- 4. D. Scheffer, et al, "Random Addressable 2048 X 2048 Active Pixel Image Sensor", *IEEE Transactions on*

Electron Devices, Vol. 44, No. 10, pp. 1716-1720, October, 1997.

- S. Mendis, et al, "CMOS Active Pixel Image Sensor", *IEEE Transactions on Electron Devices*, Vol. 41, No. 3, pp. 452-453, March, 1997.
- 6. G. Deptuch, et al, "Design and Testing of Monolithic Active Pixel Sensor for Charged Particle Tracking", *IEEE Transactions on Nuclear Science*, Vol 49, No. 2, p601-610, 2002.
- J. Nakamura, et al, "On-focal-plane signal processing for current-mode active pixel sensors", *IEEE Transactions on Electron Devices*, Vol 44, pp. 1747-1758, 1997.
- R.H. Nixon, et al, "128 X 128 CMOS photodiode-type active Pixel Sensor with on-chip Timing Control and Signal Chain Electronics", *Charge-Coupled Devices and* Solid-State Optical Sensors V, Proceedings of SPIE, Vol. 2415, pp. 117-123, 1995.
- 9. O. Yadid-Petch and E.R. Fossum, "Wide Intrascene Dynamic Range CMOS APS Using Dual Sampling",

IEEE Transactions on Electron Devices, Vol 44, pp. 1721-1723, 1997.

- 10. L. Scheick, F. Novak, "Hot Pixel Generation in Active Pixel Sensors: Domeimetric and Microdosimetric Response", *Radiation and its Effects on Component and Systems*, Noorwikj, Netherlands, September, 2003.
- 11. N. Ricquier and B. Dierickx, "Pixel Structure with Logarithmic Response for Intelligent and Flexible Imager Architectures", *Microelectron. Eng.*, Vol. 19, pp. 631-634, 1992.
- 12. W. Nelson, "Accelerated Testing", John Wiley & Sons, New York, 1990.

ACKNOWLEDGEMENTS

This work was carried out at Jet Propulsion Laboratory, California Institute of Technology, under a contract with the National Aeronautics and Space Administration. The authors also would like to thank Dr. Bedabrata Pain and Chris Wrigley for helpful technical discussions.