

Evidence for Reduction of Noise and Radiation Effects in G^4 -FET Depletion-All-Around Operation

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Abstract:

The low noise and radiation-hard operation of the SOI Four-Gate transistor (G^4 -FET) is experimentally demonstrated. When operated in depletion-all-around (DAA) mode, the G^4 -FET drain current flows in the middle of the silicon film, far from the interfaces. The influence of oxide and interface traps on the conduction channel is suppressed by biasing the front and back gates in depletion or, even better, in inversion. Systematic data show a significant reduction of low-frequency noise as well as a quasi-insensitivity to total-dose radiation effects, up to 10 Mrad. These features come along with superior static characteristics in DAA mode and are attractive for G^4 -FET-based analog circuits.

1. Introduction

CMOS is the technology of choice for advanced ULSI circuits. However for low-noise and radiation-hard applications, the MOS transistor may be inadequate as it involves surface conduction that is very sensitive to interface defects. These defects can capture and release the conducting channel carriers and generate excess noise. If the defect concentration increases during operation as a consequence of exposure to ionizing radiation, they give rise to a change in device parameters, *i.e.*, threshold voltage shift, subthreshold swing and transconductance degradation. The situation is aggravated in SOI MOSFETs due to the existence of the buried oxide. Among the bulk-channel transistors, JFETs are competitive for low-noise and radiation hardness but their integration density is poor. On the other hand, buried-channel MOSFETs have inadequate transconductance.

The four-gate transistor (G^4 -FET), proposed recently, combines the advantages of MOSFETs and JFETs. In particular, it can be operated in volume (DAA, Depletion-All-Around) mode which is free from the influence of interface and oxide defects. In ESSDERC'04, we have demonstrated excellent static characteristics (transconductance, subthreshold swing and g_m/I_D ratio) for DAA operation [1]. As the interface defects can be 'erased' in DAA mode, the noise performance and the radiation

hardness are expected to improve. This is the aspect systematically documented in the present work.

2. G^4 -FET Structure and DAA Operation

An n-channel G^4 -FET is fabricated with the standard partially-depleted SOI CMOS technology and actually uses the same layout as a p-channel inversion-mode MOSFET with the two body contacts on each side of the channel (Fig. 1). The current is due to majority carriers (electrons) and flows from one body contact to the other, which play the roles of drain and source. There are four *independent* gates [2] that provide an unchallenged functional flexibility and enable the adjustment of the conducting channel position within the body. This attribute is exploited in this paper to optimize the noise and total-dose performance. The original source and drain of the p-MOSFET are used, in G^4 -FETs, as two extra lateral gates: the junction gates, JG1 and JG2, are reverse-biased with respect to the channel to provide a JFET-like control. The vertical front-gate (G1) can induce accumulation, depletion or inversion at the top interface according to the mode of operation. The substrate *emulates* a back-gate (G2) and is used to modulate the back surface potential and conducting channel location.

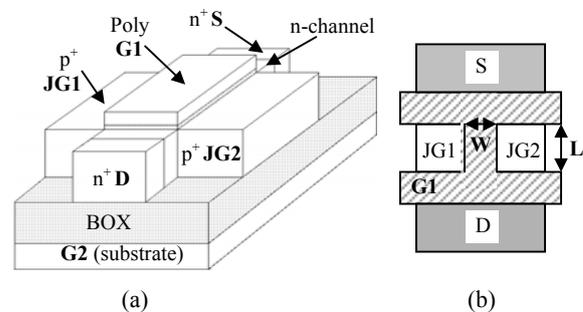


Fig. 1. (a) N-channel G^4 -FET structure, (b) H-gate G^4 -FET layout.

In depletion-all-around operation [1], the G^4 -FET is driven by the junction-gates, which are tied together ($V_{JG1} = V_{JG2} = V_{JG}$, Fig. 2a). Front and back gate are biased to a constant voltage, inducing depletion or inver-

sion at the interfaces. Drain current flows in the middle of the silicon film and the conducting channel is surrounded by the depletion regions (Fig. 2a).

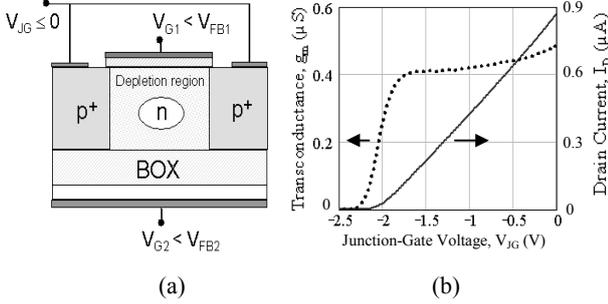


Fig. 2. N-channel G^4 -FET operating in Depletion-All-Around mode: (a) cross-section (drain current flows perpendicular to the figure), (b) drain current and transconductance as a function of the junction-gate voltage. Interfaces are depleted with $V_{G1} = V_{G2} = 0$ V ($V_D = 50$ mV, $W = 0.35$ μm , $L = 1.2$ μm).

The current and transconductance characteristics of an n-channel G^4 -FET operating in DAA mode are shown in Fig. 2b. For $V_{JG} = -2.5$ V, the channel is pinched-off by the junction-gates and current and transconductance ($g_m = \partial I_D / \partial V_{JG}$) are zero. As V_{JG} approaches zero, the lateral depletion regions shrink and allow first the onset of the conduction channel and then its gradual widening in the middle of the body. This is reflected by the increase of both g_m and I_D with V_{JG} . The operation principle and the resulting characteristics are here similar to those of a JFET.

In DAA mode, if the front and/or back interfaces are in inversion, the inversion layers are of the same type as the junction gates (p-type in an n-channel G^4 -FET). They are naturally biased to V_{JG} and behave as vertical junction gates. This provides an enhanced control over the volume channel, which means an improvement of the transconductance, subthreshold swing and transconductance-to-current ratio [1]. Furthermore, the Early Voltage of the H-gate G^4 -FETs (Fig. 1b) is very high in DAA mode especially when the interfaces are in inversion (3 kV at $V_D = 3.5$ V for $L = 1.2$ μm). This is basically due to the relative insensitivity of the channel cross-section, enclosed by the junction-gates, to drain voltage variations. High g_m/I_D ratio and Early Voltage provide an extremely high intrinsic DC gain in G^4 -FETs operating in DAA mode.

3. Low-Frequency Noise

N-channel, encapsulated G^4 -FETs, fabricated in a conventional 0.35 μm partially-depleted SOI process are used for the low-frequency noise measurements. The transistors were 0.35 μm wide and 3.4 μm long, with 20 channels in parallel to get a relatively high drive current. Channel doping was in the 10^{17} cm^{-3} range. The silicon film, front-gate oxide and buried-oxide thicknesses were 150 nm, 8 nm and 350 nm, respectively. Drain-to-source voltage was 50 mV for all measurements. We first monitored the difference between the noise levels of the

surface channel and the volume channel of the transistor: the G^4 -FET was biased with a constant V_{JG} and V_{G2} , while V_{G1} was swept to drive the front-surface from depletion to strong accumulation. In Fig. 3 the resulting drain current noise power S_I , at 10 Hz, is shown as a function of the drain current. Related current-voltage characteristics in semilogarithmic scale are given in the inset of Fig. 3. For $V_{G1} = -2$ V, transistor is in the off-state because the depletion regions induced by the front, back and the junction-gates fully deplete the body. Until the flatband condition is reached, *i.e.*, for -2 V $< V_{G1} < 0.56$ V, the front-depletion region shrinks gradually and enables *volume* conduction, far from the front interface. In this region the noise power increases with the current as the number of carriers increases (more fluctuations). Around the onset of accumulation at the front-surface (flatband condition), for $I_D = 0.5$ μA , a very abrupt kink is observed in the noise amplitude. This kink is as large as *one order of magnitude*, and is due to the excess 1/f noise generated at the surface. This excess noise is due to the dynamic capture/release of the carriers by the oxide traps located in the vicinity of the interface [3]. The opening of the surface accumulation channel is clearly confirmed by the visible change in subthreshold slope (inset of Fig. 3).

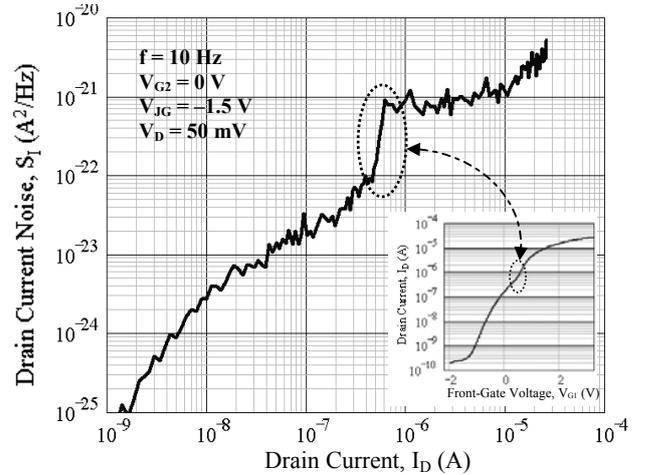


Fig. 3. Drain current noise of the n-channel G^4 -FET. The kink corresponds to the onset of the front accumulation current added to a bulk component. Inset: related current voltage characteristics.

The noise characteristics in DAA mode are presented in Fig. 4 (solid curves). In Fig. 4a, the variation of the normalized drain current noise, S_I/I_D^2 is shown as a function of drain current for different front-gate voltages; I_D is varied by sweeping V_{JG} . For comparison, the dotted curve labeled “surface mode” is obtained by sweeping V_{G1} and shows the noise level related to a front accumulation current. From Fig. 4a it is noted that the normalized noise amplitude gradually decreases as the front interface goes from depletion ($V_{G1} = 0$ V) to strong inversion ($V_{G1} = -2$ V), moving the conducting channel away from the front-interface. When the front-surface is in strong inversion, the noise amplitude is minimum for a given drain current because the minority carriers (holes)

shield the interface, preventing the exchange between the channel electrons and the oxide traps [4]. The noise is lowered, especially at low current, by two orders of magnitude. Note also that the surface noise magnitude (dotted line) is higher than that related to the volume over the whole bias range.

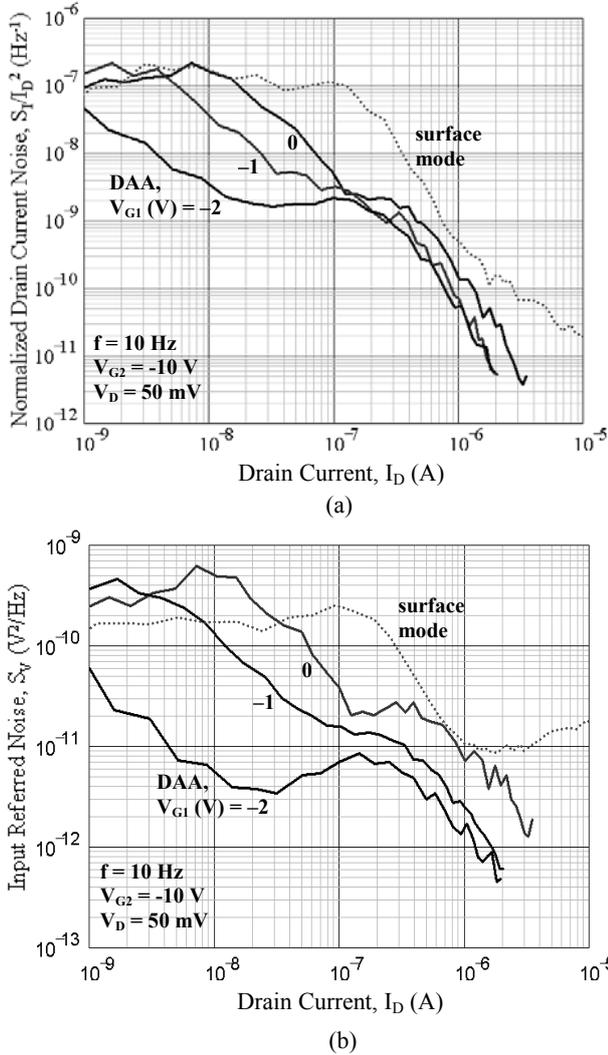


Fig. 4. N-channel G^4 -FET operated in DAA mode (solid curves): (a) Normalized drain current noise, (b) input referred noise as a function of drain current. The noise related to front surface accumulation is also shown for comparison (dotted curves, $V_{JG} = -3$ V).

The input referred noise is considered as the figure of merit for low-noise design. It allows the circuit designer to simultaneously take into account the noise level *and* the gain of a device or circuit. In Fig. 4b, the variation of the noise referred to input ($S_V = S_I/g_m^2$) is shown as a function of drain current. The characteristics originate from the same measurements as in Fig. 4a, but are normalized with respect to the transconductance, seen by the junction gates (in DAA mode) or by the front gate (in surface mode). It is essential to note again that the DAA mode with front interface in inversion provides the lower noise operation from low to high currents. The performance is now even better than for DAA with depleted front-interface, due to a higher transconductance.

4. Total-Dose Radiation Hardness

The most significant consequences of ionizing radiation are the positive charge build-up in the oxides and the interface state generation, giving rise to a shift in transistor parameters [5]. The problem is acute in SOI MOSFETs where the buried oxide is thick and accumulates more charges. Therefore the total dose response of a transistor depends essentially on the sensitivity to this charge build-up. The advantage of DAA operation is straightforward: the presence of inversion layers, ensured by appropriately biasing V_{G1} and V_{G2} , blocks the surface potentials. Thus the transistor characteristics become insensitive to the degradation of the oxides and interfaces.

In Fig. 5, simulated G^4 -FET DAA characteristics are compared with those of partially-depleted floating-body n-channel MOSFETs. Same structural parameters (doping, dimensions) are used in the simulations (Silvaco Atlas 3D/2D). The effects of the ionizing irradiation are emulated by gradually increasing the oxide (N_{ot}) or interface (N_{it}) trapped charge density. It is seen from Fig. 5a that the G^4 -FET in DAA mode with both interfaces in inversion is insensitive to oxide or interface charge build-up. By contrast, in the n-MOSFETs, the threshold voltage shifts significantly for oxide trapped or interface trapped charge densities above 10^{11} cm^{-2} (interface traps are assumed to be of acceptor type, uniformly distributed in the upper half of the bandgap).

Figure 5b shows the subthreshold swing variation. In partially-depleted MOSFETs, the subthreshold swing deteriorates dramatically from 90 to 200 mV/dec as the density of interface traps increases. The G^4 -FET DAA features two remarkable properties: (i) the swing is almost ideal (62 mV/dec), which is unusual for partially-depleted devices [1,2], and (ii) it stays constant with increased interface charge density.

It is important to note that in MOSFETs the threshold shift and subthreshold swing variation with the total dose depend on the gate oxide thickness ($t_{ox1} = 10$ nm is used for simulations in Fig. 5). In G^4 -FET DAA, if there is any change in V_T or swing with the radiation dose, it is *independent* of the front and back gate oxide thickness as long as V_{G1} and V_{G2} keep the interfaces in strong inversion for the whole V_{JG} range.

The experimental variations of the threshold voltage and subthreshold swing in a p-channel G^4 -FET in DAA mode with both interfaces in inversion are shown in Fig. 6a as a function of total dose. 10 keV X-rays were used to irradiate the transistor up to 10 Mrad(SiO_2) at a dose-rate of 31 krad(SiO_2)/min. A single-channel device with $L = 1.2$ μm was used. Figure 6a points out that the change in subthreshold swing is negligible and an excellent value of 70 mV/dec is still available after 10 Mrad irradiation. The threshold shift is below 100 mV for 1 Mrad and reaches 350 mV for 10 Mrad. This shift may be related to damage induced in the body, resulting in a lowering of the channel free carrier density; although X-rays do not induce significant damage in Si at typical dose levels, the dose considered here is very high.

Figure 6b shows the g_m/I_D ratio as a function of the nor-

malized drain current for different total-dose values. Both interfaces are in inversion and therefore DAA provides improved transconductance for a reduced drain current (as compared to the case where interfaces are depleted). The resulting g_m/I_D ratio in the subthreshold region (35 V^{-1}) is close to the theoretical maximum [1]. After 10 Mrad total dose, the peak value of g_m/I_D is degraded to 28 V^{-1} , which is still a high value. As a matter of fact, for relatively high drain currents the g_m/I_D ratio does not deteriorate at all with total dose (superimposed curves in Fig. 6b).

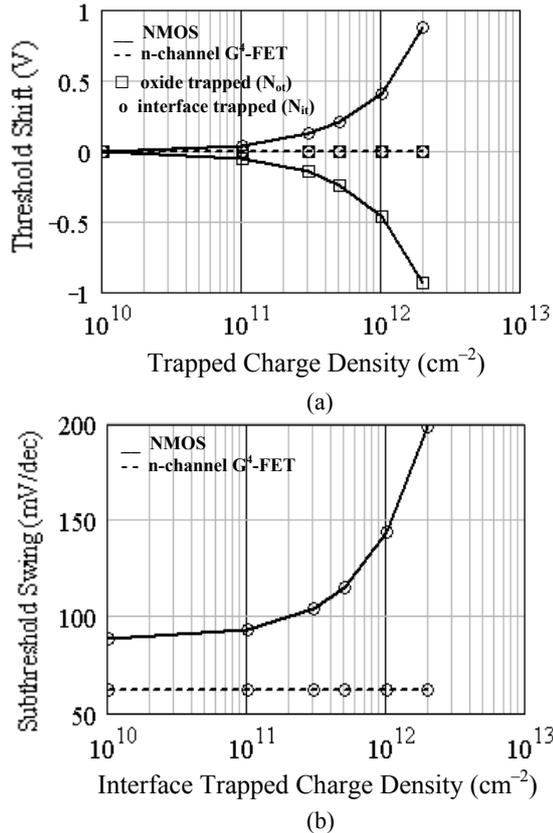


Fig. 5. Comparison of the NMOSFET and n-channel G^4 -FET (operating in DAA mode with both interfaces in inversion) simulated threshold voltage shift (a) and simulated subthreshold swing (b) as a function of the trapped charge density ($W = 0.35 \mu\text{m}$, $L = 1 \mu\text{m}$, $t_{\text{ox}1} = t_{\text{ox}2} = 10 \text{ nm}$, $t_{\text{Si}} = 200 \text{ nm}$, $N_{A,D} = 2 \cdot 10^{17} \text{ cm}^{-3}$).

The G^4 -FET radiation-hard concept demonstrated here needs further investigation. The characteristics shown in Fig. 6 were measured by applying 80 V to the substrate in order to induce inversion at the back interface. Such a high voltage is impractical for circuit applications. The solution is to use the G^4 -FETs with thinner buried oxides or with a double-gate configuration.

5. Conclusion

The low-frequency noise and total-dose performance of the G^4 -FET operating in DAA mode was measured and analyzed. It was found that when both interfaces are in inversion, the drain current sensitivity to surface and oxide defects is minimized. The low-frequency noise is

reduced by one to two orders of magnitude and radiation-hard operation is achieved up to 10 Mrad.

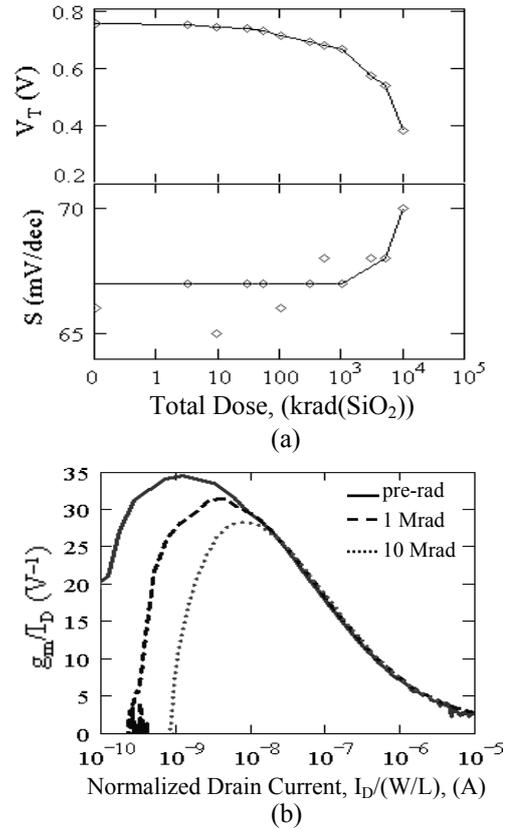


Fig. 6. Measured total-dose characteristics of the p-channel G^4 -FET operating in DAA mode with both interfaces in inversion ($V_{G1} = 3.3 \text{ V}$, $V_{G2} = 80 \text{ V}$): (a) Variation of the threshold voltage and subthreshold swing as a function of the total dose ($V_D = -50 \text{ mV}$), (b) g_m/I_D ratio as a function of normalized drain current for the different total-dose values ($V_D = -2.5 \text{ V}$). During irradiation, all terminals were grounded except in (b) where $V_{G1} = 3.3 \text{ V}$.

References:

- [1] K. Akarvardar, S. Cristoloveanu, P. Gentil, B. J. Blalock, B. Dufrene and M. M. Mojarradi, "Depletion-All-Around in SOI G^4 -FETs: a Conduction Mechanism with High Performance," ESSDERC Proceedings, 217, (2004).
- [2] B. Dufrene, K. Akarvardar, S. Cristoloveanu, B. J. Blalock, P. Gentil, E. Kolawa and M. M. Mojarradi, "Investigation of the Four-Gate Action in G^4 -FETs," IEEE Trans. Electron Devices, **51**, 1931, (2004).
- [3] S. Cristoloveanu and S. Li, Electrical Characterization of Silicon-On-Insulator Materials and Devices, Kluwer Academic Publishers (1995).
- [4] T. Elewa, B. Boukriss, H. S. Haddara, A. Chovet and S. Cristoloveanu, "Low-Frequency Noise in Depletion-Mode SIMOX Transistors," IEEE Trans. Electron Devices, **38**, 323, (1991).
- [5] J. A. Felix, J. R. Schwank, C. R. Cirba, R. D. Schrimpf, M. R. Shaneyfelt, D. M. Fleetwood and P. E. Dodd, "Influence of Total-Dose Radiation on the Electrical Characteristics of MOSFETs," Microelectronic Engineering, **72**, 332, (2004).