A Novel Four-Quadrant Analog Multiplier Using SOI Four-Gate Transistors (G^4-FETs)

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Abstract:

A novel analog multiplier using SOI four-gate transistors (G^4-FETs) is presented. Thanks to the multiple inputs of the G^4-FET that may be biased independently, the number of transistors in the proposed circuit is dramatically reduced, compared to conventional single-gate MOSFET based multipliers. Only four G^4-FETs are needed to build the multiplier core. The circuit is feasible with a standard SOI CMOS process. Two different configurations, both based on the linear modulation of the front-gate threshold voltage by the junction-gates, are presented. This paper addresses the theoretical analysis as well as the preliminary measurement results.

1. Introduction

The G^4-FET is a novel SOI transistor offering high functionality thanks to its independently biased multiple inputs [1]. It has the same structure (Fig. 1) as that of a partially-depleted SOI MOSFET with two independent body contacts, one on each side of the channel. The drain current is comprised of majority carriers flowing from one body contact to the other (*i.e.,* the body contacts of the MOSFET are used as drain and source for the G^4-FET). The source and drain of the regular MOSFET are promoted as two extra gates (junction gates, JG1 and JG2), which squeeze the channel via the reverse-biased junctions as in a JFET. The role of the polysilicon top gate (G1) is the same as in an accumulation-mode MOSFET. The substrate *emulates* a fourth MOS gate (G2).

The G^4-FET offers exciting options to the analog designer, when it is driven either from one gate (while the remaining gates are held at a constant voltage) or from multiple gates simultaneously. In the former case, the conduction parameters (*i.e.*, threshold voltage, transconductance, noise performance, radiation hardness etc.) related to the control gate may be adjusted and optimized by the biases on the remaining gates. Such an approach was used in [2] to build a temperature compensated voltage reference. In the latter case, the G^4-FET provides the opportunity to build multiple input circuits with much reduced transistor count compared to their CMOS counterparts. This strategy is used in this paper to design an analog multiplier.

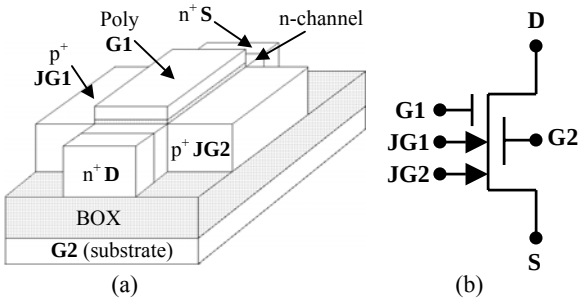


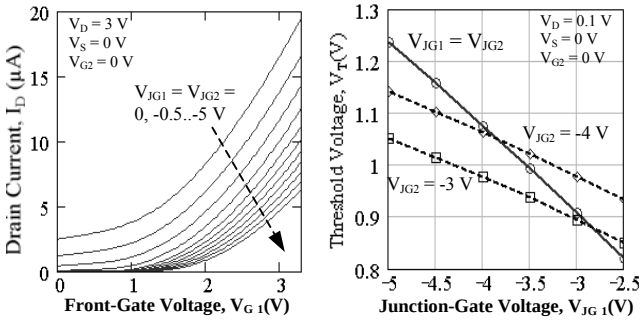
Fig. 1. N-channel G^4-FET: (a) structure, (b) schematic.

2. G^4-FET Operation and Model

The G^4-FET can basically be seen as an accumulation-mode MOSFET but with two junction-gates, one on each side of the channel. The junction-gates operate as in a JFET and alter the potential distribution within the body via the lateral depletion regions they induce. On a partially-depleted body, if the reverse bias on the junction-gates is sufficiently high, they can switch the G^4-FET from normally-on to normally-off mode. Further increase of $|V_{JG}|$ modulates the threshold voltage related to the front gate (G1).

In Fig. 2a, the saturated drain current of an n-channel G^4-FET is shown as a function of the front-gate voltage for different junction-gate voltages. For $V_{JG} = 0$ V, transistor is normally-on because the electron concentration within the body, determined by the doping level, enables the conduction even when $V_{G1} = 0$ V. As V_{JG} is decreased from 0 V to –1.5 V, depletion regions induced by the junction-gates gradually widen and suppress the volume component of the current. At $V_{JG} = –2$ V, G^4-FET becomes normally-off: the channel is fully-depleted for $V_{G1} = 0$ V and drain current depends only on the electrons accumulated near the front-interface by the increase of V_{G1}. For $V_{JG} < –2$ V the body potential is further lowered and due to the charge coupling between the front-gate and junction-gates it becomes harder for the front-gate to accumulate carriers at the front-interface, which means an increase of the threshold voltage.

In normally-off operation, the saturated drain current of the G^4-FET is expressed as for the accumulation-mode MOSFETs [3] by including the threshold voltage modulation by the junction-gates:



(a) (b)

Fig. 2. N-channel partially-depleted G⁴-FET: (a) Measured variation of drain current in saturation as a function of the front-gate voltage for different junction-gate voltages (V_{JG1} = V_{JG2}), (b) Threshold voltage as a function of V_{JG1} for constant V_{JG2} (dashed lines) and for V_{JG2} = V_{JG1} (solid line), (W = 0.35 μm, L = 5 μm).

$$I_D = \frac{K_n}{2}\left[V_{G1S} - V_T(V_{JG1S}, V_{JG2S})\right]^2 \qquad (1)$$

K_n is the transconductance parameter given by:

$$K_n = \frac{W_{eff}}{L} C_{ox1} \mu_{neff} \qquad (2)$$

C_{ox1} is the front-gate oxide capacitance, μ_{neff} is the effective mobility and W_{eff} is the effective channel width, which is about half of the distance between the two junctions due to the squeezing effect of the junction-gates. V_T is the threshold voltage of the G⁴-FET corresponding to the flatband condition at the front interface. For V_{JG1S} = V_{JG2S} = V_{JGS} (junction gate to source voltage), $V_T(V_{JGS})$ dependency in fully-depleted mode is modeled in [4] for the different conditions at the back interface. When the back-gate is grounded, the back surface is slightly-depleted and the threshold voltage

$$V_T(V_{JGS}) = V_{T0} + \xi V_{JGS} \qquad (3)$$

varies linearly with V_{JGS}. The coupling factor ξ is a strong function of the device width, W, and depends weakly on silicon film thickness, t_{Si}. It is independent of the channel doping as long as the film is fully-depleted. V_{T0} and ξ are defined in Table 1.

ξ	$(\gamma - \alpha)\left(\frac{C_J}{C_{ox1}} + \frac{\gamma C_J^2}{C_{ox1}(C_{ox2} + \alpha C_J)}\right)$		
V_{T0}	$V_{FB1} + \frac{\gamma C_J C_{ox2}}{C_{ox1}(C_{ox2} + \alpha C_J)} V_{FB2} - \xi V_P$		
V_P	$\Phi_b - \frac{qN_D W^2}{8\varepsilon_{Si}}$		
γ	$\frac{2\sqrt{2}}{\sinh(2\sqrt{2}\, t_{Si}/W)}$	α	$\frac{2\sqrt{2}}{\tanh(2\sqrt{2}\, t_{Si}/W)}$
C_J	$\frac{\varepsilon_{Si}}{W}$	$C_{ox1,2}$	$\frac{\varepsilon_{ox}}{t_{ox1,2}}$

Table 1. Definition of the G⁴-FET parameters [4].

Systematic measurements suggest that for $V_{JG1} \neq V_{JG2}$:

$$V_T(V_{JG1S}, V_{JG2S}) = V_{T0} + \frac{\xi}{2}(V_{JG1S} + V_{JG2S}) \qquad (4)$$

The measured variation of V_T with V_{JG1} in fully-depleted mode is shown In Fig. 2b. As V_{JG1} becomes more negative, threshold voltage increases linearly. For V_{JG2} = V_{JG1} (solid line), the slope is double (ξ = – 0.16) that obtained for constant V_{JG2} (dashed lines), as predicted by equations (3) and (4).

3. Analog Multiplier

The two configurations of the analog multiplier are shown in Figs. 3a and 3b. In both cases, the multiplier core is constructed by four G⁴-FETs biased by a constant current sink and loaded by two identically sized resistors, R_L, which are used to convert the differential output current to a differential output voltage.

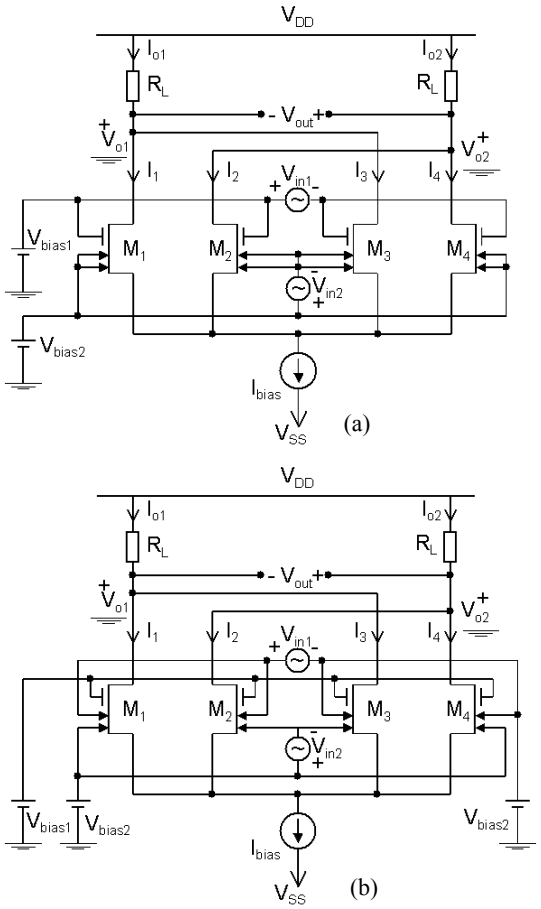


Fig. 3. The G⁴-FET analog multiplier circuits. (a) Configuration 1: V_{in1} = V_{G1}, V_{in2} = V_{JG1} = V_{JG2}, (b) Configuration 2: V_{in1} = V_{JG1}, V_{in2} = V_{JG2} and a constant voltage, V_{bias1}, is applied to the front-gate of the G⁴-FETs. In both configurations V_{bias2} is used to DC bias the junction gates. (V_{G2} = 0, not shown to simplify the schematics).

The difference between the two circuits stems from their input configurations: in the first case, the differential input voltages are applied to the front-gate and to the junction-gates (which are tied together for each

transistor, Fig. 3a). In the second configuration, the inputs are applied to JG1 and JG2 while the front-gate is biased to a constant voltage. In both cases the differential output voltage, V_{out}, is given by:

$$V_{out} = V_{o2} - V_{o1} = \left[(I_1 + I_3) - (I_2 + I_4)\right]R_L \quad (5)$$

The drain currents I_1 to I_4 are expressed by substituting (3) or (4) into (1) and then writing V_{G1}, V_{JG1} and V_{JG2} in terms of the bias and differential input voltages. For example, the drain current of M1 in the first configuration is expressed as:

$$I_{1(1)} = \frac{K_n}{2}\left[V_{bias1} + V_{in1} - V_S - V_{T0} - \xi(V_{bias2} + V_{in2})\right]^2 \quad (6)$$

Using similar relations for I_2, I_3 and I_4, then substituting into (5) yields:

$$V_{out(1)} = -4K_n\xi R_L V_{in1}V_{in2} \quad (7)$$

indicating that in Configuration 1 (Fig. 3a), the differential output voltage is a linear function of the product of the differential input voltages.
For the second configuration, $I_{1(2)}$ is written as:

$$I_{1(2)} = \frac{K_n}{2}\left[V_{bias1} - V_S - V_{T0} - \frac{\xi}{2}(2V_{bias2} + V_{in1} + V_{in2})\right]^2 \quad (8)$$

and the output voltage becomes:

$$V_{out(2)} = K_n\xi^2 R_L V_{in1}V_{in2} \quad (9)$$

demonstrating that a linear multiplication of the input voltages is also achieved in Configuration 2 (Fig. 3b). Note that the multiplier gain is different for the two configurations. It can be shown that for single-ended inputs the output voltages expressed by (7) and (9) are reduced by a factor of 4.

4. Input Range

The circuits given in Fig. 3a and 3b function as a multiplier as long as drain current of the G^4-FETs can be expressed using (1). This imposes the following requirements over the n-channel G^4-FET bias:

1. Cut-off prevention: $V_{G1S} > V_T(V_{JG1S}, V_{JG2S})$.
2. Drain current saturation: $V_{G1D} \le V_T(V_{JG1S}, V_{JG2S})$.
3. Reverse-bias on junction-gates with respect to the source: $V_{JG1S} \le 0$, $V_{JG2S} \le 0$.

V_{G1S} and V_{G1D} are front-gate to source and front-gate to drain voltages, respectively. The third condition is valid if the body is fully-depleted. If the body is partially-depleted, the requirement is more strict: $V_{JG1,2S}$ should be sufficiently negative to keep the body fully-depleted during operation.
Writing the bias current, I_{bias}, as the sum of four drain currents, the common source voltage in the configuration 1 and 2 is expressed respectively as:

$$V_{S(1)} = V_{bias1} - \xi V_{bias2} - V_{T0} - \sqrt{\frac{I_{bias}}{2K_n} - \left(V_{in1}^2 + \xi^2 V_{in2}^2\right)} \quad (10a)$$

$$V_{S(2)} = V_{bias1} - \xi V_{bias2} - V_{T0} - \sqrt{\frac{I_{bias}}{2K_n} - \frac{\xi^2}{4}\left(V_{in1}^2 + V_{in2}^2\right)} \quad (10b)$$

Drain voltages are calculated starting from I_{o1} and I_{o2}, which are written as the sum of two drain currents. The replacement of (10a) or (10b) for V_S in drain current equations yields:

$$V_{o1,2(1)} = V_{DD} - \frac{I_{bias}R_L}{2} \pm 2K_n R_L \xi V_{in1}V_{in2} \quad (11a)$$

$$V_{o1,2(2)} = V_{DD} - \frac{I_{bias}R_L}{2} \mp \frac{K_n R_L \xi^2}{2} V_{in1}V_{in2} \quad (11b)$$

To find the input range, the G^4-FET terminal voltages V_{G1}, V_{JG}, V_S (Eq. 10) and V_D (Eq. 11), expressed as a function of the differential input voltages, have to be applied in conditions 1 through 3 mentioned above. An example of the input range for both configurations is given in Figs. 4a and 4b, respectively. The input-range is shown by the intersection of the areas determined by the requirements 1 to 3 (in Config. 2, the first restriction is much more relaxed than the others and therefore it is not shown on Fig. 2b). The circuits are intended to operate under ± 3.3 V supply voltage. Body of the G^4-FETs is assumed to be fully-depleted for $V_{JG1,2S} = 0$ V.

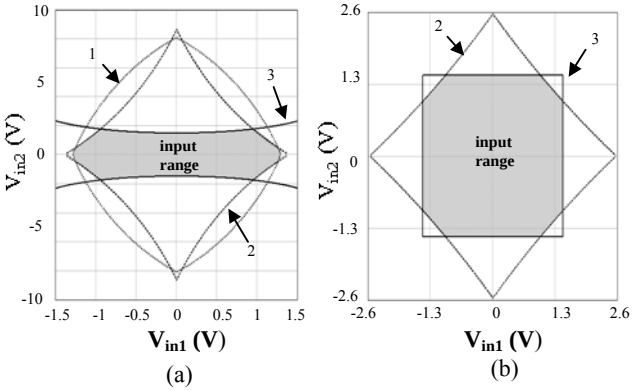


Fig. 4. Input range of the multiplier (grey area): (a) Config. 1 (W = 0.35 μm, L = 5 μm, V_{DD} = 3.3 V, I_{bias} = 20 μA, K_n = 3 μA/V^2, ξ = -0.16, V_{T0} = 0.4 V, V_{bias1} = 2 V, V_{bias2} = -2 V, R_L = 65 kΩ), (b) Config. 2 (Same parameters as (a) except R_L = 190 kΩ).

In general, if the same circuit and device parameters are used, the second configuration allows to a higher input range than the first one as both of the inputs are multiplied by the coupling factor ξ, which is typically between –1 and 0. On the other hand for the same input range, the first configuration provides a larger output swing as can be noticed by comparing (7) with (9). Depending on the specifications of input and output range for a given application, one topology may be preferred over the other.

5. Experimental Results

The preliminary measured results obtained from circuits constructed with discrete transistors (fabricated with a conventional 0.35 µm partially-depleted SOI technology) are presented in Fig. 5 and Fig. 6. Despite the poor matching between the discrete G^4-FETs on separate chips, the operation of both configurations as a multiplier is validated. In Fig. 5, transfer characteristics are shown. For single-ended input voltages varying between ± 1.5 V, 0.8 V and 0.4 V peak-to-peak variation of the differential output voltage is obtained in configuration 1 and 2, respectively.

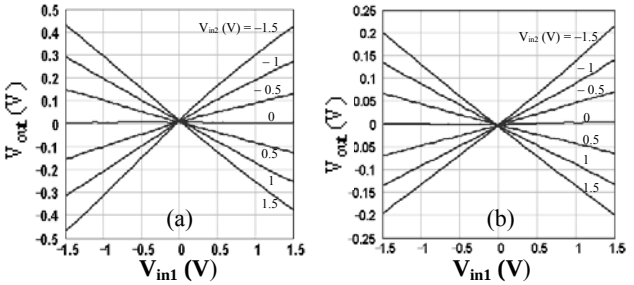


Fig. 5. Measured DC transfer characteristics (single-ended inputs). (a) Config. 1 (W = 0.35 μm, L = 10 μm, V_{DD} = 10 V, I_{bias} = 15 μA, V_{bias1} = 1.7 V, V_{bias2} = -1.8 V, R_L = 500 kΩ), (b) Config. 2 (W = 0.35 μm, L = 5 μm, V_{DD} = 5 V, I_{bias} = 10 μA, V_{bias1} = 0 V, V_{bias2} = -3 V, R_L = 500 kΩ).

The product of a square-wave with a sinusoidal signal (Config. 1) and with a triangular-wave (Config. 2) are shown in Figs. 6. For single-ended inputs, high gain in the first configuration and large input swing (close to supply voltage) in Config. 2 are noticed.

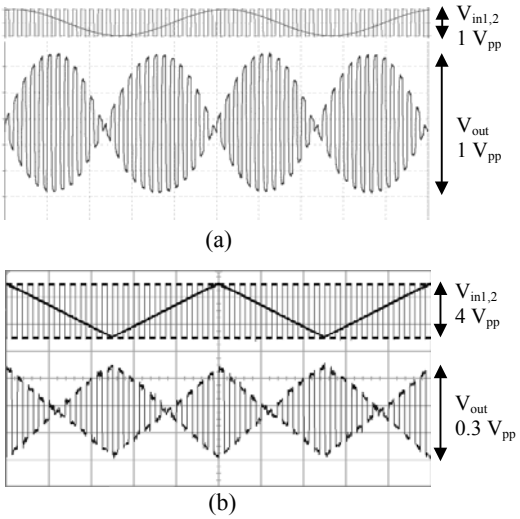


Fig. 6. Measured waveforms (single-ended inputs). (a) product of a 20 Hz, 1 V_{pp} sinusoidal-wave with 500 Hz, 1 V_{pp} square-wave (W = 0.3 μm x 10, L = 2.4 μm, V_{DD} = 3.5 V, V_{SS} = -3.5 V, I_{bias} = 35 μA, V_{bias1} = 2 V, V_{bias2} = -2.5 V, R_L = 100 kΩ), (b) Config. 2, product of a 10 Hz, 4 V_{pp} triangular-wave with 200 Hz, 4 V_{pp} square-wave (W = 0.35 μm, L = 5 μm, V_{DD} = 5 V, I_{bias} = 15 μA, V_{bias1} = 0 V, V_{bias2} = -3.5 V, R_L = 200 kΩ).

The DC linearity of the first configuration for single-ended inputs is measured. The multiplier is configured as a variable gain-amplifier and a 20 Hz 1.6 V peak to peak ramp is applied as V_{in2}. Then, the differential output amplitude is adjusted to get V_{out}/V_{in2} = 1 while V_{in1} amplitude was 0.6 V. The linearity error is given by the difference between V_{out} and V_{in2} and measured as 3 %. Interchanging the inputs results in 4.5 % error between V_{out} and V_{in1}. The linearity should be considerably better in a fully integrated implementation with improved device matching. But already, our experimental results validate the four-quadrant behavior of the circuit.

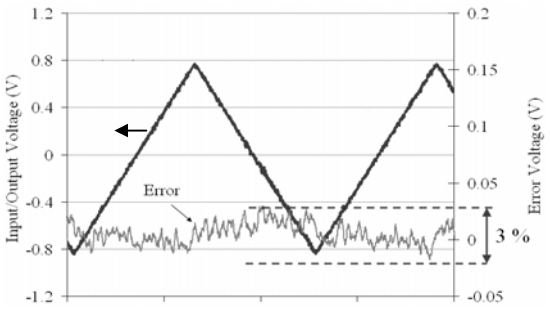


Fig. 7. Config.1 DC linearity error (V_{in2} = V_{out}, f = 20 Hz, V_{in1} = 0.6 V, W = 0.3 μm x 10, L = 2.4 μm, V_{DD} = 6 V, V_{SS} = -2 V, I_{bias} = 35 μA, V_{bias1} = 2 V, V_{bias2} = -3.3 V, R_L = 100 kΩ).

6. Conclusions

The operation of a novel four-quadrant analog multiplier designed with SOI four-gate transistors is theoretically and experimentally demonstrated. The circuit is feasible on a standard SOI process and requires only four G^4-FETs and a current source. Its functionality is based on the linear control of the front-gate threshold voltage by the junction-gates. We believe that the design strategy and experimental results exposed in this paper promote the design of other G^4-FET based multiple-input circuits.

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