# Ka-Band Wide-Bandgap Solid-State Power Amplifier Task

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**WBG SSPA Program Status Review**
**Aerospace Corp. El Segundo, California**
**September 1, 2004**

# Task Overview

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## Program Goal

Determine feasibility of a 120–150 W Ka-band SSPA based on WBG semiconductor with an EM build in 3–5 years and FM in 7–8 years to replace TWTAs for space telecommunication

## JPL investigating three architectures providing 2X to > 90X combining with target combining loss < 1 dB

- W/G Binary, W/G Radial, Parallel-Plate Radial

## Deliverables

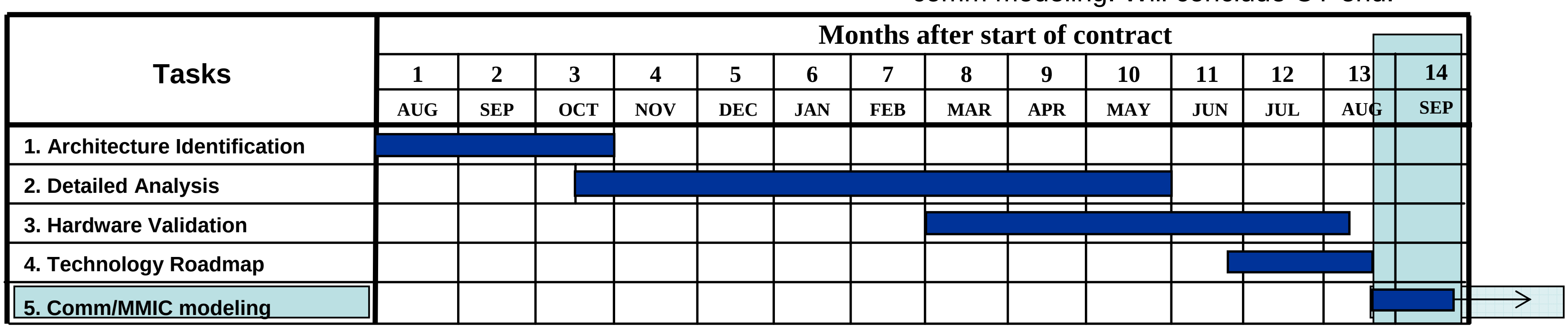
- SSPA architecture design and recommendations
- MMIC performance guidelines
- Independent assessment of GaN technology status
- Technology development roadmap through flight qualification

## Progress Since Monterey Review:

- Hardware Validation of key components
  - Binary Septum combiner fabricated and measured
  - Mode transducer (for Radial) fabricated and measured
    - Radial Base nearing completion
  - Parallel Plate isolation hardware TBD
- Linearity comm architecture examination started
- MMIC packaging initiated
- Rock Systems on contract for GaN reliability
- New MMIC assy facility on schedule for end of 2004

## Financial Status:

- First year funding (9 mo’s) concluded May
- Balance funding (3 mo’s) turned-on mid-July via GRC using second year funding
  - Will round out 12 month effort by FY end
  - Official second-year follow-on will support comm modeling. Will conclude CY end.



# Power Combiners Studied

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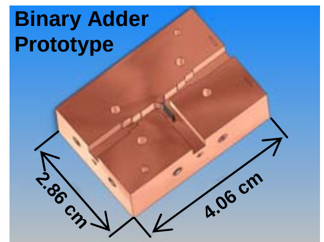
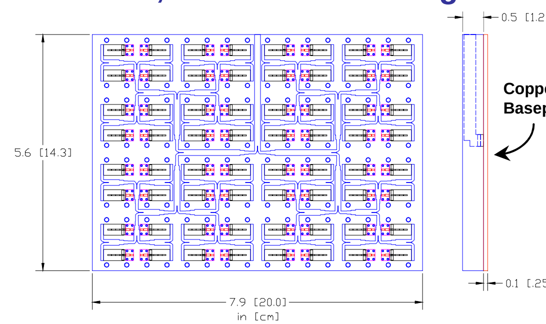
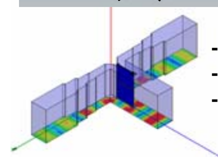
- **Defined trade space and subsystem requirements**
- **Selected combining architectures for detailed study**
  - W/G Binary, WG Radial & Parallel-Plate Radial (JPL)
- **Continuing detailed electrical design**
  - Prototype hardware in development
  - Target combining efficiency > 80% (< 1 dB loss)
- **Defined preliminary MMIC requirements**
  - 1-10 W per MMIC, > 10 dB gain, and 45%-55% PAE
- **Established subcontract to evaluate WBG reliability status, identify critical path, and develop a roadmap for insertion into high-reliability applications**
  - Completed technology survey

## 64-Way W/G Binary Combiner, 140 W SSPA Design




Copper Baseplate

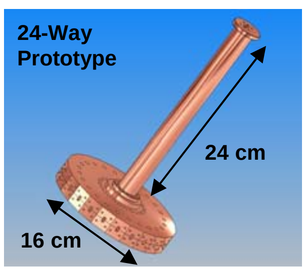


**-0.04 dB I.L.**
**-25 dB R.L.**
**-30 dB Isolation**

**-0.9 dB total loss from MMIC to WR28 output flange including 30% margin**

**Estimated Mass 1.7 kg**

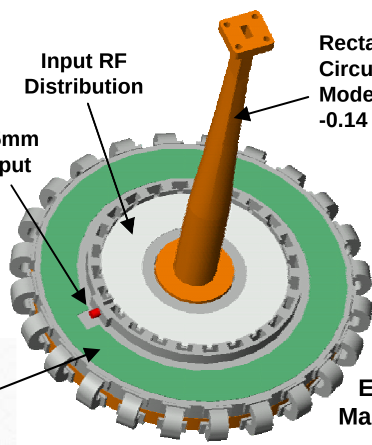
## 96-Way W/G Radial Combiner, 150 W SSPA Design

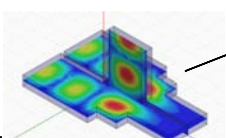



**Input RF Distribution**

**3.5mm Input**

**Rectangular to Circular WG Mode Converter -0.14 db I.L.**



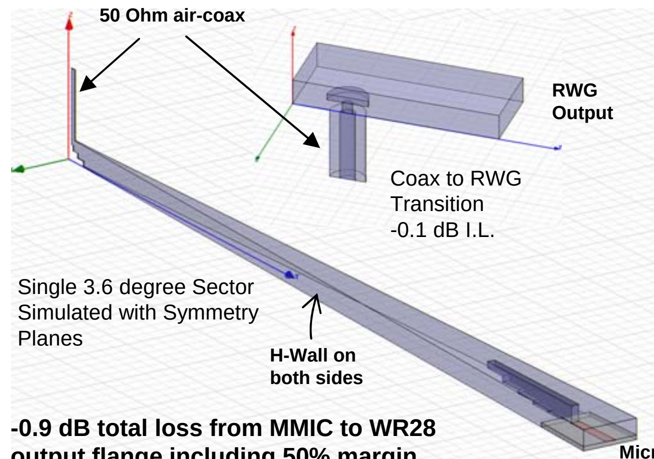


**Hybrid-Tee Combiners Inside Base**
**-0.2 dB I.L.**
**-23 dB Isolation**

**Estimated Mass 1.5 kg**

**-1.0 dB total loss from MMIC to WR28 output flange including 30% margin**

## 100-Way Parallel-Plate Combiner




**-0.9 dB total loss from MMIC to WR28 output flange including 50% margin**

**Microstrip Input**

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# Hardware Validations

# Hardware Validation: Binary Combiner

## Fabricated and Measured Prototype Septum Binary Combiner

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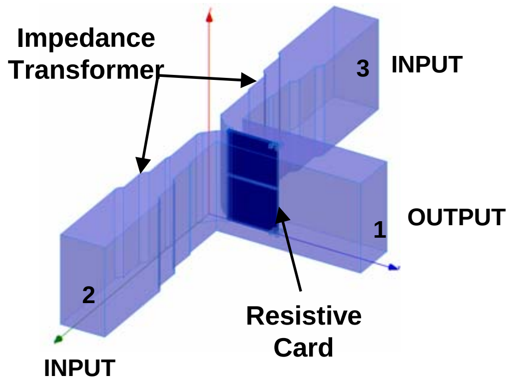
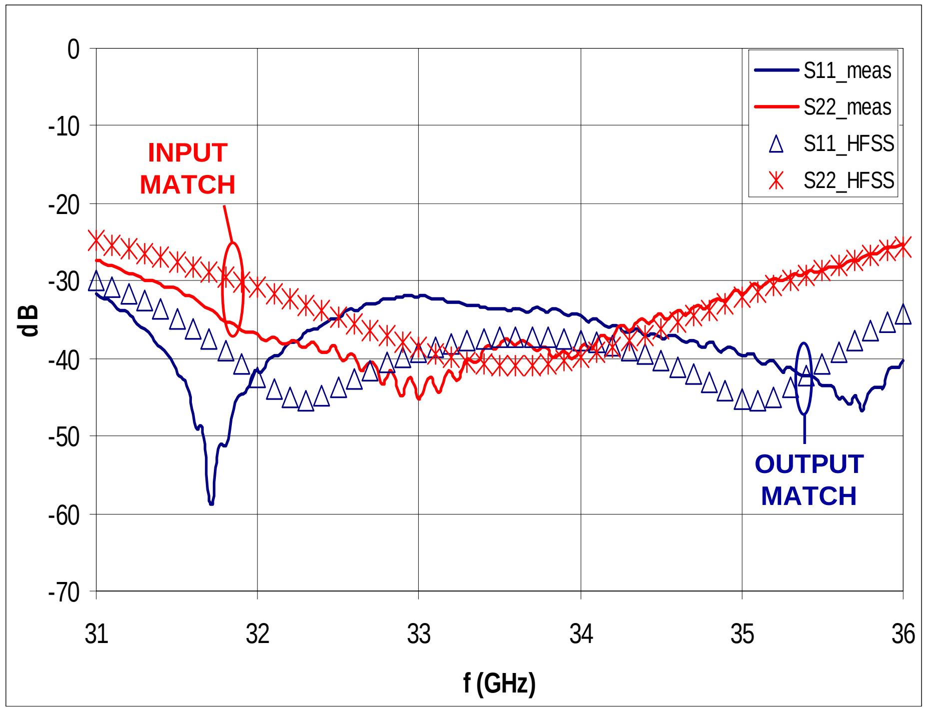



| | Match, dB | | | Coupling, dB | | Isolation, dB | Ampl. Bal., dB | Ph. Bal., deg |
|---|---|---|---|---|---|---|---|---|
| S/N | s11 | s22 | s33 | s12 | s13 | s23 | s12-s13 | phS12-phS13 |
| 1 | -31 | -25 | -25 | -3.055 | -3.060 | -27 | 0.005 | 0.75 |
| 2 | -31 | -25 | -25 | -3.030 | -3.095 | -27 | 0.065 | 0.2 |
| 3 | -31 | -25 | -25 | -3.045 | -3.060 | -27 | 0.015 | 0.49 |
| 4 | -31 | -25 | -25 | -3.047 | -3.044 | -27 | 0.003 | 0.27 |
| **Average:** | **-31** | **-25** | **-25** | **-3.044** | **-3.065** | **-27** | **0.022** | **0.43** |

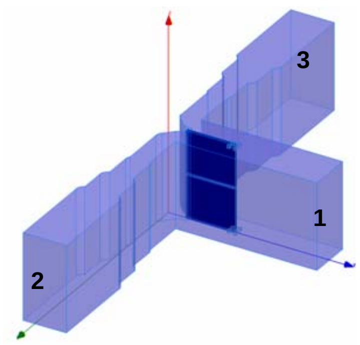
Split Block Design

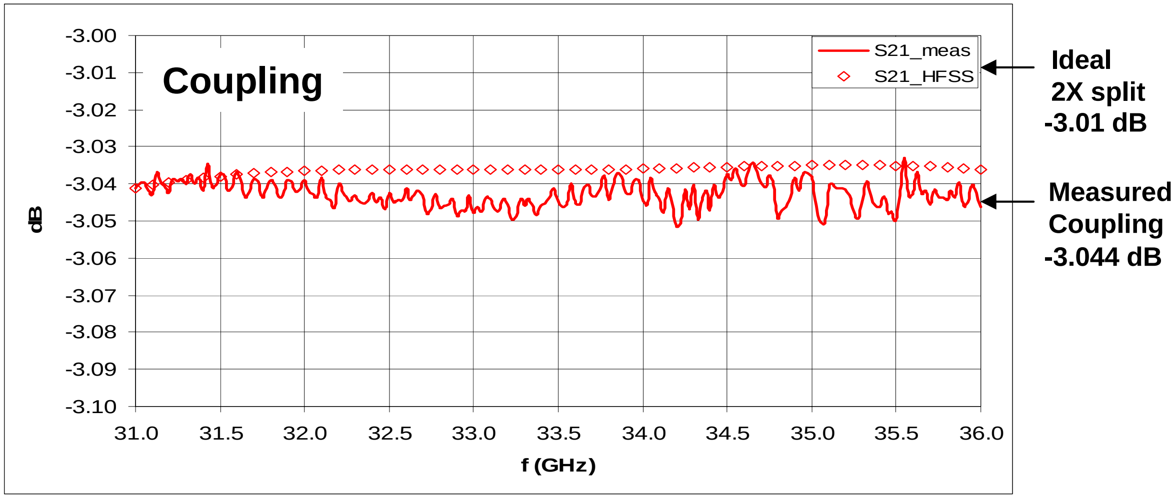
**<u>Four</u> 2X combiner prototype units were fabricated and measured**



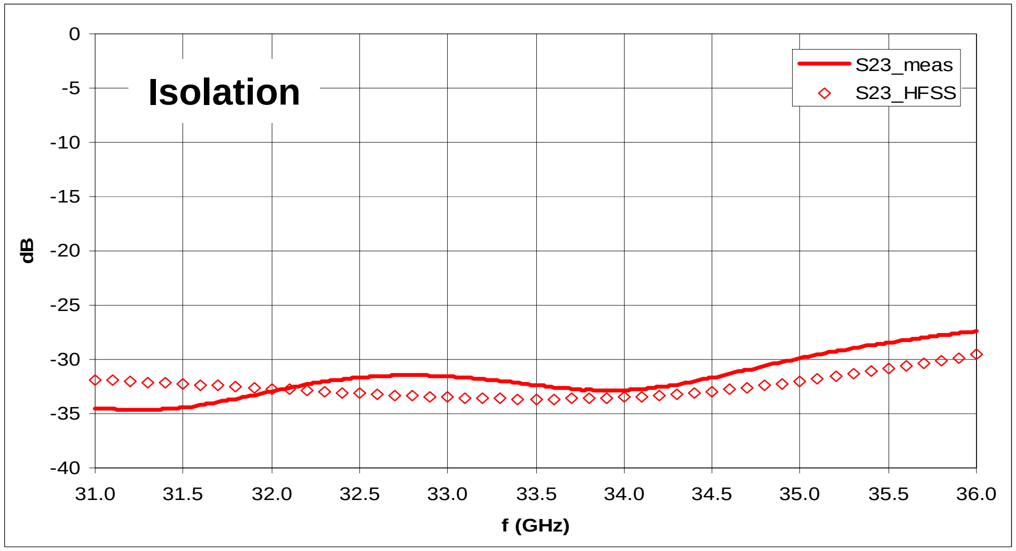

- Broadband match (>15% bandwidth)
  - Input match >25 dB
  - Output match >30 dB
- Excellent amplitude and phase balance
- Excellent unit-unit uniformity
- Good agreement with HFSS analysis
  - Differences well within fabrication tolerances

# Measured Coupling and Isolation




***Breakthrough feature: Extremely low insertion loss with high isolation over a broad bandwidth.***




- Measured insertion loss less than 0.05 dB (worst case)
- Measured isolation >27 dB
- Good agreement with HFSS analysis.



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# Hardware Validation: Binary Combiner
# Septum Combiner Benefits

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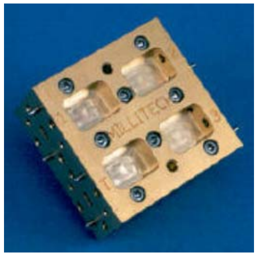
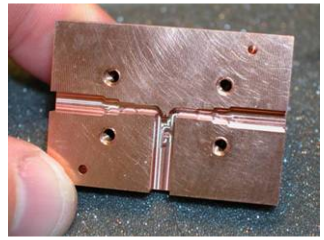
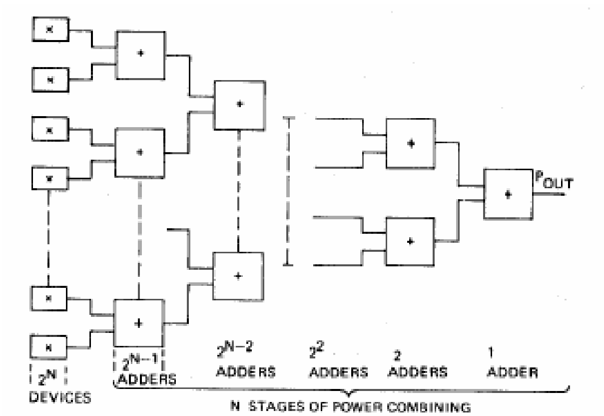


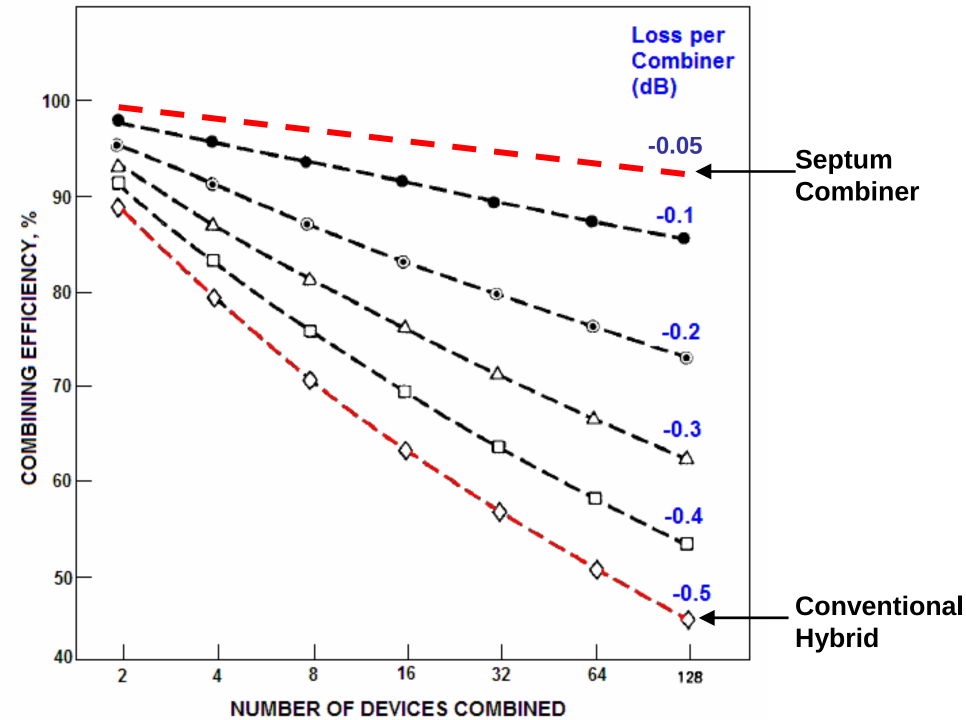
**Millitech CSS-28 Hybrid Coupler**
5% Bandwidth for equal power division
0.5 dB max insertion loss
20 dB isolation typical w/ external load



**Prototype Septum Combiner**
>15% Bandwidth *(>3X improvement)*
0.05 dB max insertion loss *(10X improvement)*
27 dB isolation min (30-35 dB typical)
More compact and easier layout
*(Enables compact, higher-order combining)*

**Corporate Binary Combining**

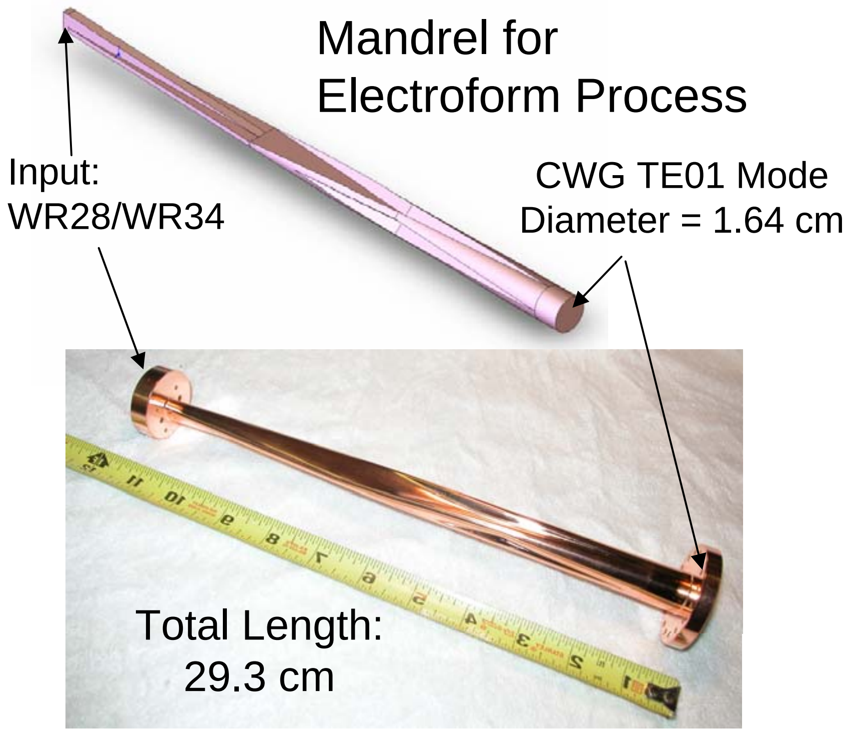


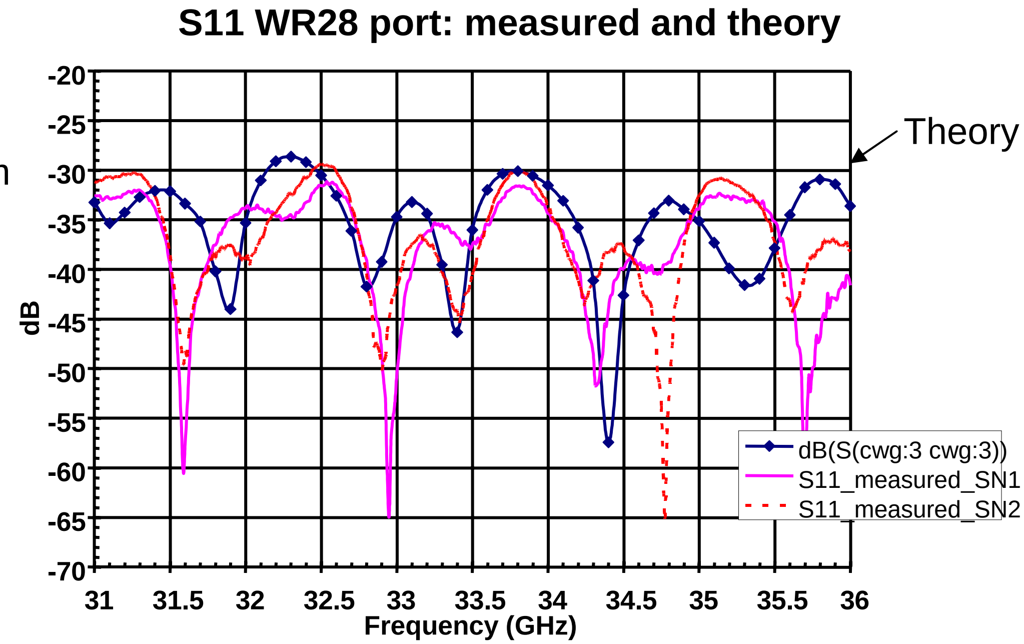




From: Russell, K.J., "Microwave power combining techniques," *IEEE Trans. Microwave Theory Tech.*, vol. 27, pp. 472-478, May 1979.

***32X combining efficiency:***
***94% with septum combiner***
***56% with conventional hybrid***

# Hardware Validation: Radial Combiner Fabricated and Measured Mode Transducer



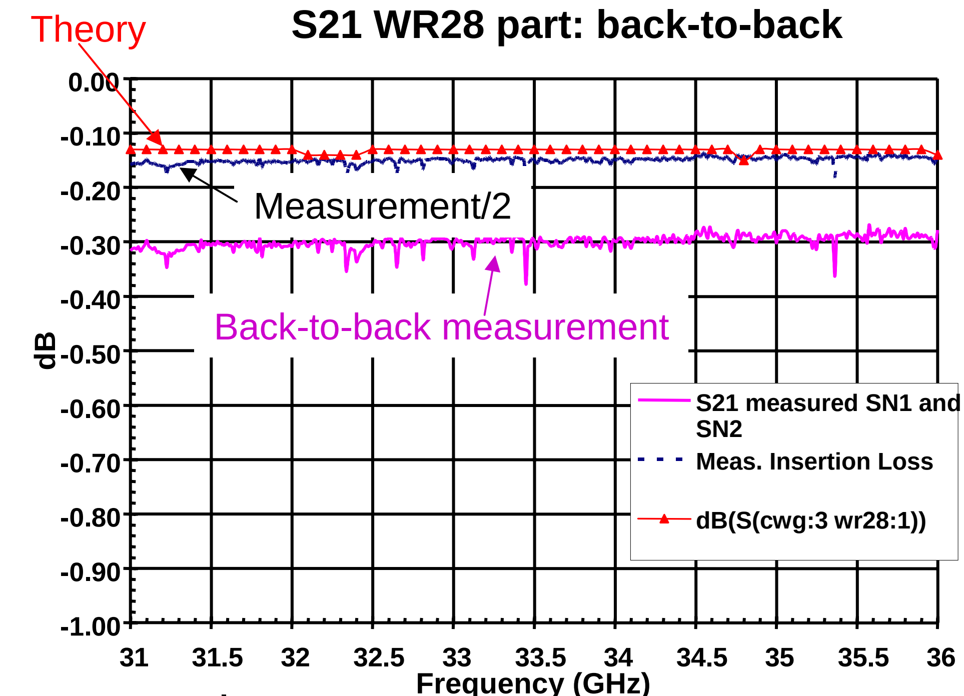

Four Marie Transducers Fabricated

- 2 x WR28 RWG input for 31 - 36 GHz
- 2 x WR34 RWG input parts for *Jupiter Icy Moons Orbiter* (JIMO) Mission Development (TWTAs radially power combined)
    - Technology transfer benefit to NASA
    - JIMO order decreased our WR28 part cost

Key Results:

- SN1 Match < -31.2 dB
- SN2 Match < -29.4 dB
- Good agreement for over-moded part
- Exceeds bandwidth needs

# Hardware Validation: Radial Combiner
## Insertion Loss Measurements of Mode Transducer

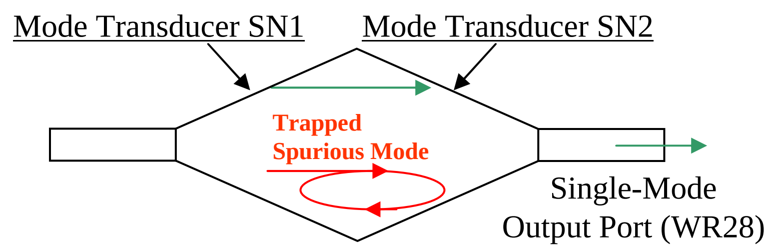



Key Results:

- Low Loss Transition < 0.19 dB
- 0.055 dB Ripple for single Mode Transducer
  - Worst Case (~ no loss)
  - Within .005 dB of requirements

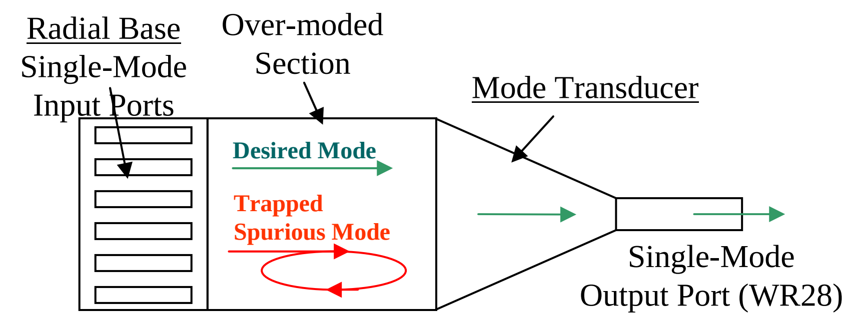
➢ Measurement with Radial Base planned for final validation of gain ripple and mode purity

### *Back-to-Back Mode Transducer Measurement*




- Recall effect of trapped modes:

### *Mode Transducer w/ Radial Base*




- Trapped modes cause gain and phase ripple in the output
- Assuming *0.25 dB* attenuation of the trapped mode by the radial base, 3deg phase ripple requires spurious modes be < -25 dB relative to the desired mode

# Hardware Validation Summary

- **Validated waveguide conductor loss versus plating types onto Aluminum**
  - **WR28 loss with silver plating (0.19 dB/ft) was ~20% lower compared to loss with gold plating (0.24 dB/ft).**
  - **Chemical polishing of metal surface prior to plating reduced loss by an additional 5%.**
  - ➢ **Allows low mass construction from Aluminum**

- **Validated septum combiner design for waveguide binary architecture**
  - **Good agreement between analysis and measurement**

- **Completed fabrication of circular to rectangular waveguide to circular waveguide mode transducer for radial architecture**
  - **Exceeded bandwidth requirements**

- **Fabrication of Radial Base nearly complete**
  - **Measurements will determine phase ripple**

- **Completed electrical design of a novel port-to-port isolation structure for parallel-plate radial architecture**
  - **Hardware validation TBD**

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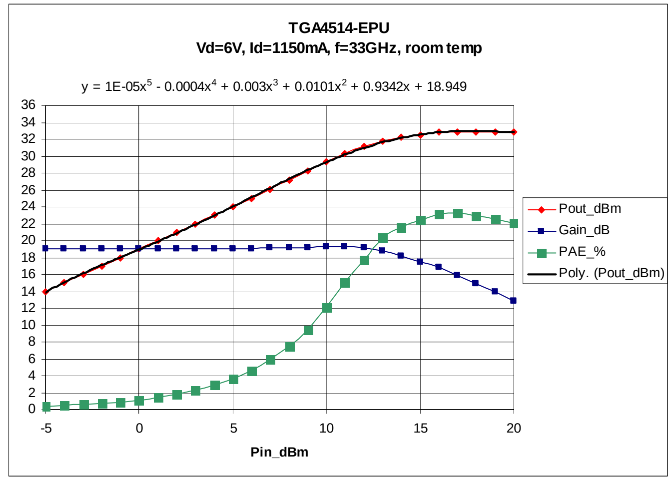
# MMIC Data for Linearity Study

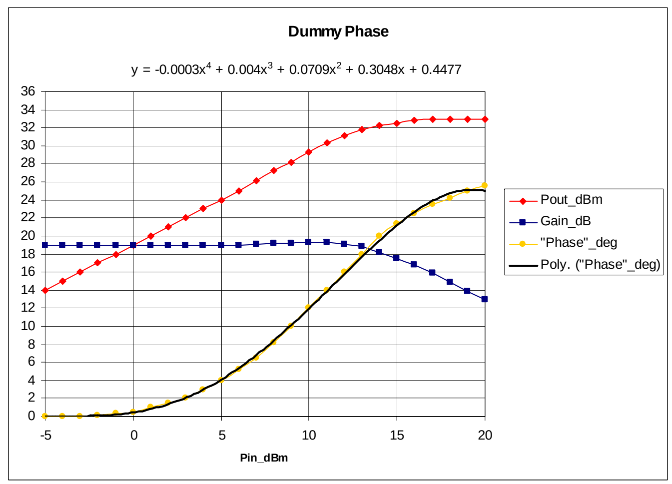
# Comm Marching Orders

- Will combine multiple power MMICs
- May need 2-3 driver/gain stages to achieve 50 dB gain
- Customer desires “advanced digital modulation,” e.g. QAM, but cannot backoff significantly to operate in linear regime; efficiency is King.
- We may be able to provide candidate MMIC performance, expected combiner performance, etc.
- What linearization technique best at Ka-band? Should we just use existing digital predistorters (e.g., Lintech)? Bias modulation?
- How will amplitude/phase balance, # stages, etc., affect
  - Linearity
  - AM/PM conversion
  - Link performance?

# Commercial MMIC Eval

- Examined commercial Tri-Quint device for modeling of linearity
  - Don’t have measured GaN MMIC data, yet
- Used preliminary data/assumptions for doing linearity simulations:
  - Amplitude response from data sheet
    - 5th order poly fit coefficients included in plot below
  - Phase response from SSPA extrapolation
    - 4th order poly fit coefficients included in plot
  - Frequency response: flat over 31-36 GHz 3dB BW
- Comm system folks used data for a first look, and as leg stretcher.



# Preliminary Evaluation of Higher Order Modulations in the Presence of Non-Linearities

# Modulation Types Under Investigation

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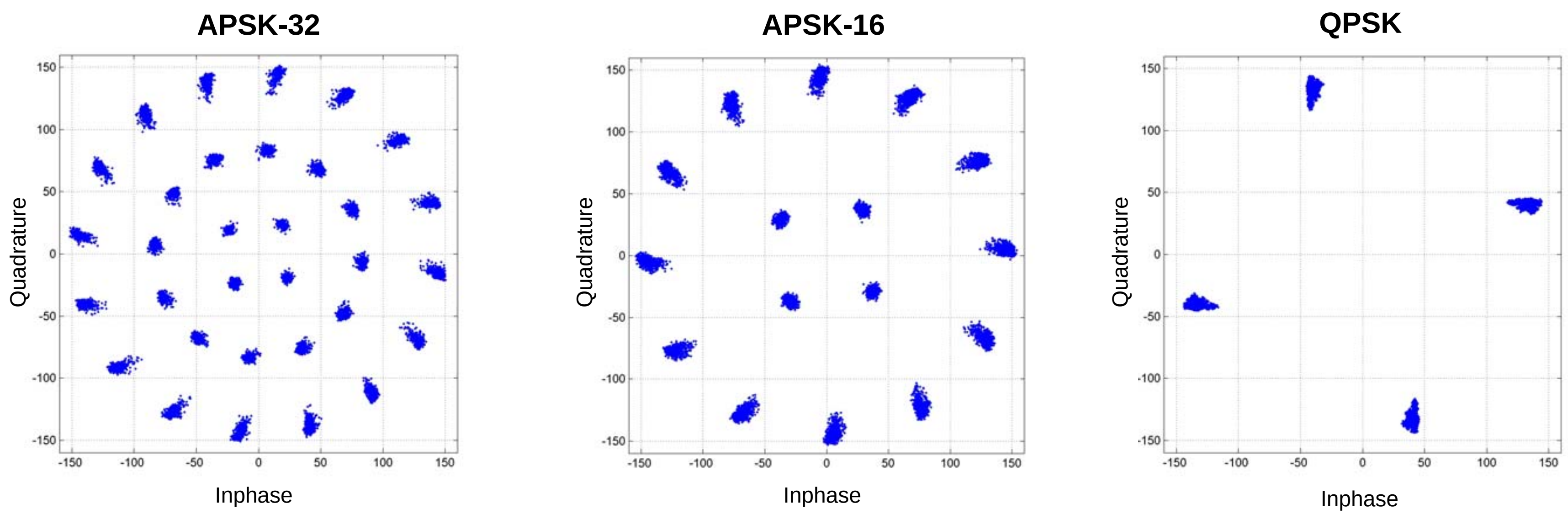
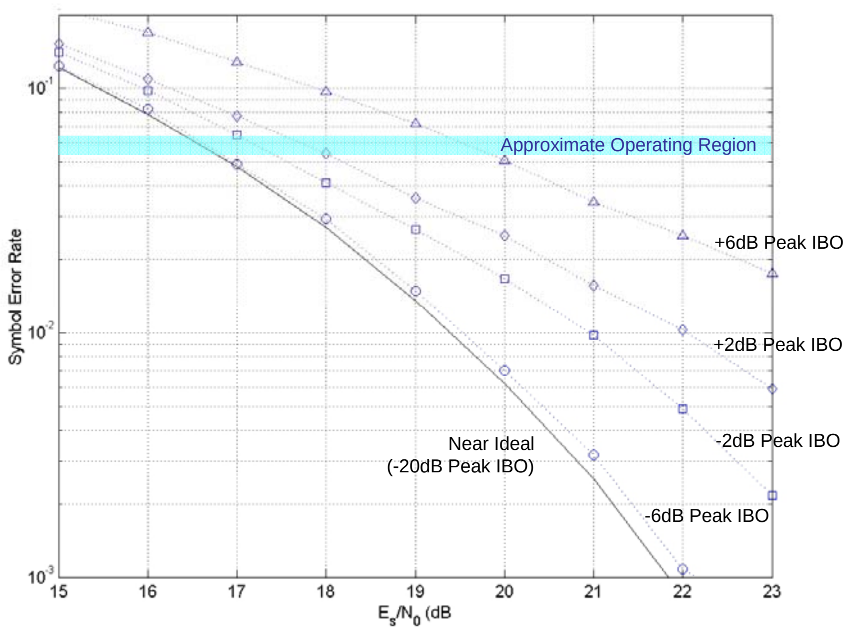


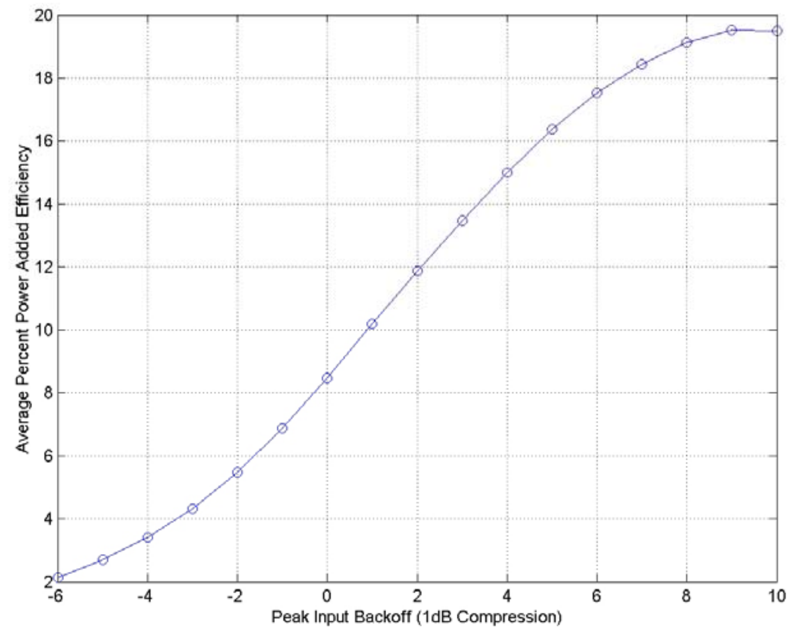

- Examined two higher order QAM-like modulations for performance under instantaneous non-linearities
  - APSK-16 (12/4 QAM)
  - APSK-32 (16/12/4 QAM)
  - Modulation descriptions based upon DVB S2 proposed standard
- Examined performance of QPSK for baseline performance validation
- Constellations represent noiseless matched filter outputs of 35% excess bandwidth square root raised cosine pulse shaping filters passed through MMIC memoryless nonlinearities (AM-AM, AM-PM)
- Waveform peak is approximately 2 dB above 1 dB compression point
- Pulse shape distortion and AM-PM effects noticeable



1. Characterization based on Triquint TGA4514-EPU

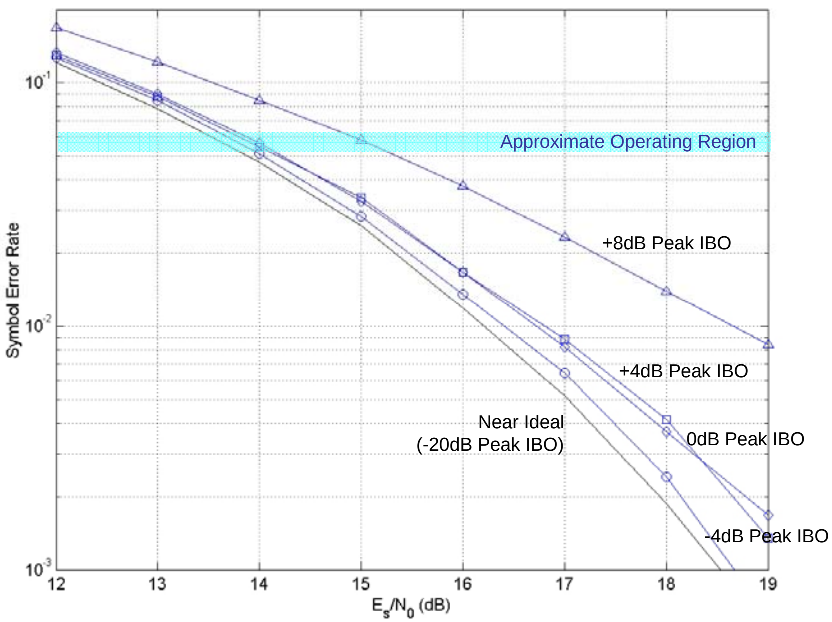
# APSK-32 Performance

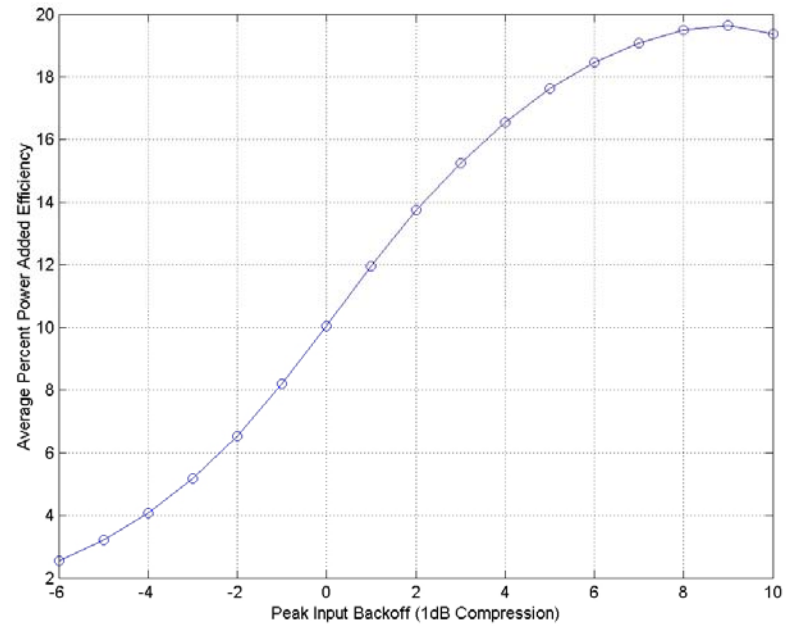



- Degradation limited to approximately 1 dB compared to ideal waveform detection for an average PAE of 12% and lower
- Phase and amplitude distortion of outer constellation ring likely cause of increasing losses under higher gain compression
- Statistical (e.g. histogram) analysis of symbol error distribution may localize main error contributions
- Possible mitigation techniques include “simple” linearization in amplitude and/or phase

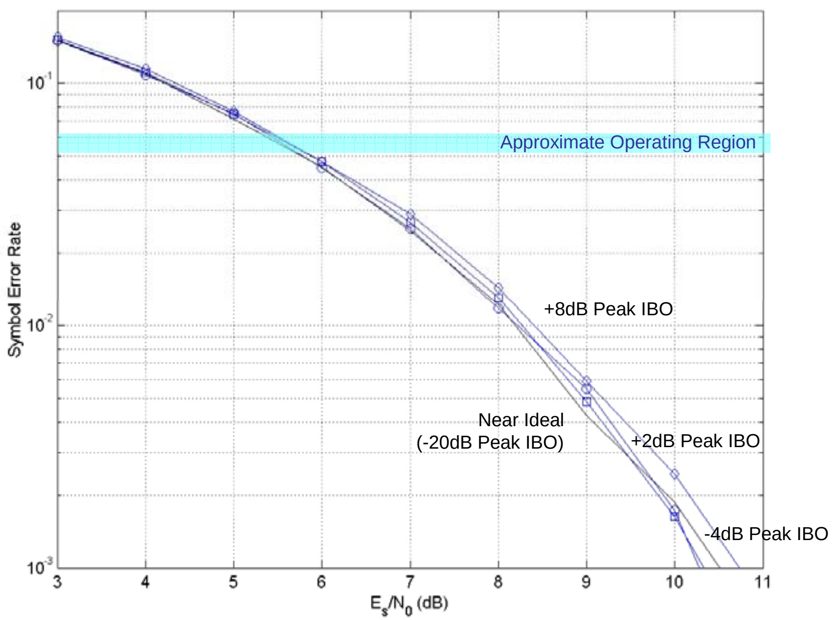
# APSK-16 Performance

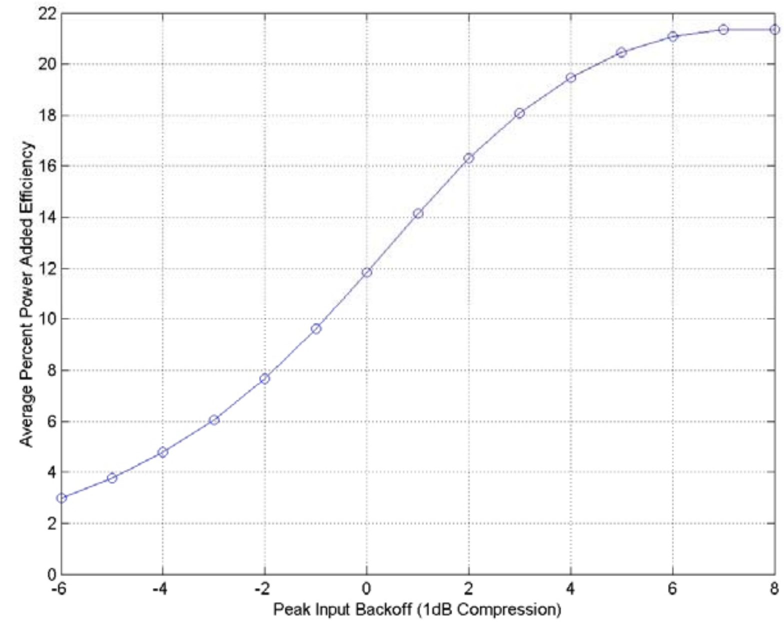



- At maximum MMIC amplifier efficiency (peak IBO approx. +8 dB), performance degradation is slightly above 1 dB
- PAE improvement at peak IBO of +8 dB is offset by performance degradation relative to peak IBO of +4 dB operating point

# QPSK Performance




- QPSK exhibits negligible loss when operating in saturation regime of the MMIC amplifier

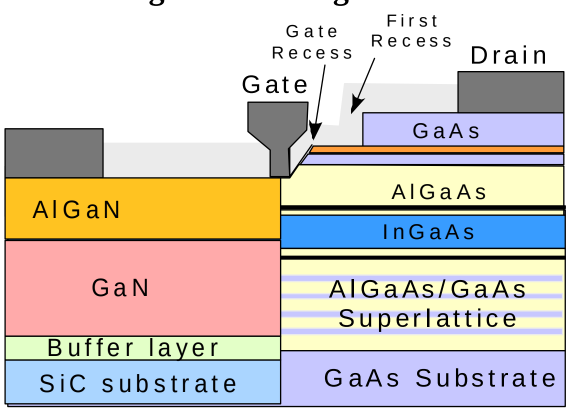
# Possible Next Steps

- Increased fidelity performance characterization
  - Uncoded bit error rate
  - Modulation integrated with high performance forward error correction (FEC)
- Incorporate modular architecture to non-linearity performance analysis
  - Model as *N* equally combined amplifiers
  - Introduce parametric errors to amplifier gain and phase curves
  - Characterize errors via statistical distributions
- Assess output spectral regrowth for regulatory/non-interference compliance
  - Spectral mask compliance
  - Adjacent/Co-channel interference analysis
- Examine fixed and adaptive non-linear compensation techniques
  - Single input “average” compensation
  - Multiple input (not necessarily *N*) “tailored” compensation
- Incorporate any needed frequency selective modeling and compensation
  - Transmitter
  - Receiver

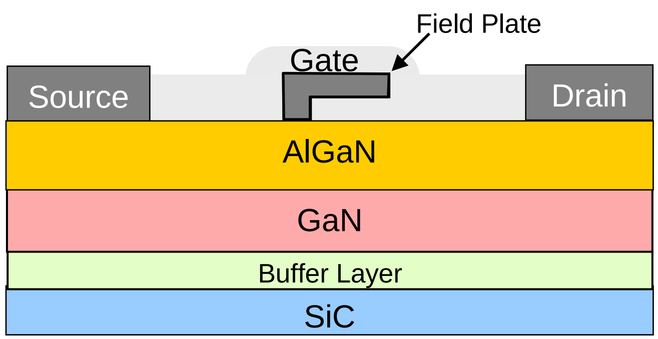
# RELIABILITY DRIVERS

| Performance area under investigation | Parameter / Method to Affect Change in Performance |
|---|---|
| Gate Leakage Current | • Adjust metallization material or barrier layer material<br>• Improve dislocations in substrate interface or adjust nucleation layer. |
| Drain Leakage Current | • Improve material quality |
| Electric-Field degradation (dispersion) | • Create a layered structure in the gate-drain region<br>• Recess gate<br>• Add a field-plate at the gate<br>• Add a p-doped cap layer between the gate and drain |
| Channel Temperature | • Optimize efficiency of device versus power density<br>• Optimize geometry of device periphery layout (fingers and spacing) |

**Incorporate Recess-Topology Structures to reduce leakage-current degradation effect**




**Addition of a Field-Plate to reduce Electric-Field degradation affect**



# Reliability Test Methodology and Metrics

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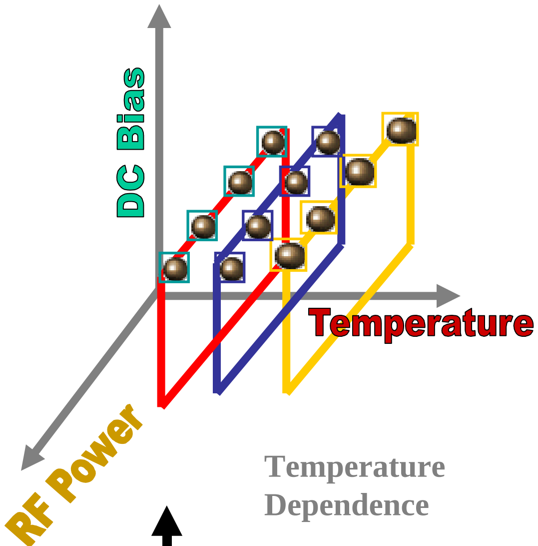
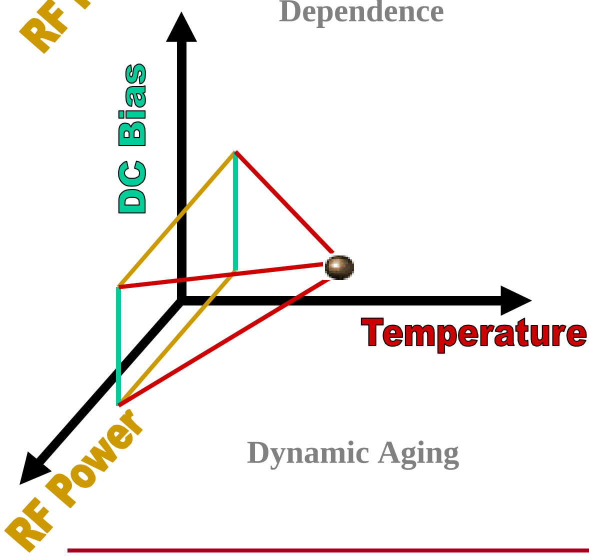
## Accelerated Life-Test Paradigms




Temperature Dependence




Dynamic Aging

| Parameter | Methodology | Characterization Test Level |
|---|---|---|
| Ohmic-contact Resistance | Temperature Dependence | Intrinsic |
| Leakage-Current | Temperature Dependence | Intrinsic |
| Transconductance | Temperature Dependence | Intrinsic |
| Forward-Voltage Turn-On | Temperature Dependence | Intrinsic |
| Reverse-Bias Breakdown-Voltage | Temperature Dependence | Intrinsic |
| Metal Migration | Static Aging | Intrinsic |
| Forward-Voltage Turn-On | Dynamic Aging | Device |
| Specific-On Resistance | Dynamic Aging | Device |
| DC & RF Transconductance | Dynamic Aging | Device |
| Reverse-Bias Breakdown Voltage | Dynamic Aging | Device |
| Saturated RF Output Power | Dynamic Aging | Device |

# ROADMAP ISSUES

# Roadmap Considerations

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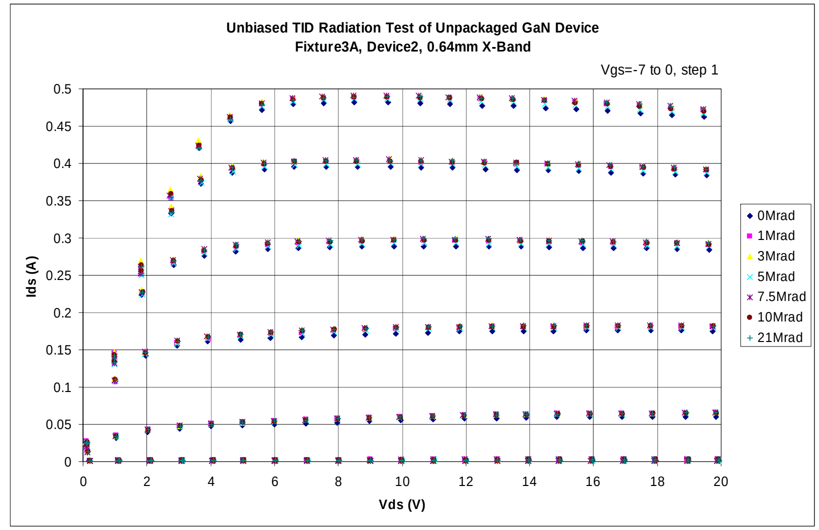
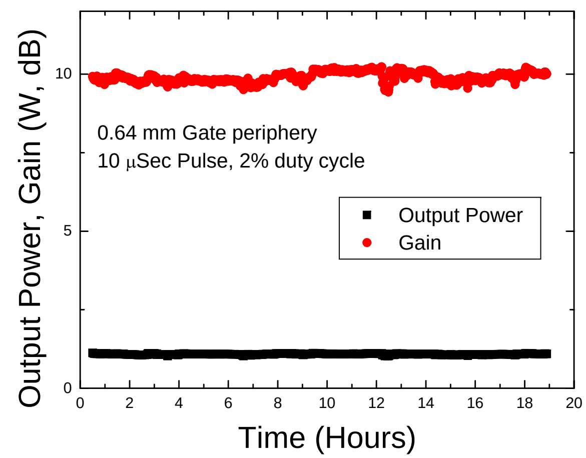
MAJOR FOCUS AREAS

- JPL Report Construct
  - Challenges
  - Requirements levied on tech dev
  - Cross-cutting issues
  - Potential solutions & pathways
- Materials & Device Performance
- MMIC Development Critical
  - Supporting developments not quite there
  - Production level reliability yields needed
- Reliability & Space Qual
  - Some promising early data
  - Need to learn from GaAs evolution
- Follow-on Proof-of-Concepts
- Performance Trials
- TRL Maturation

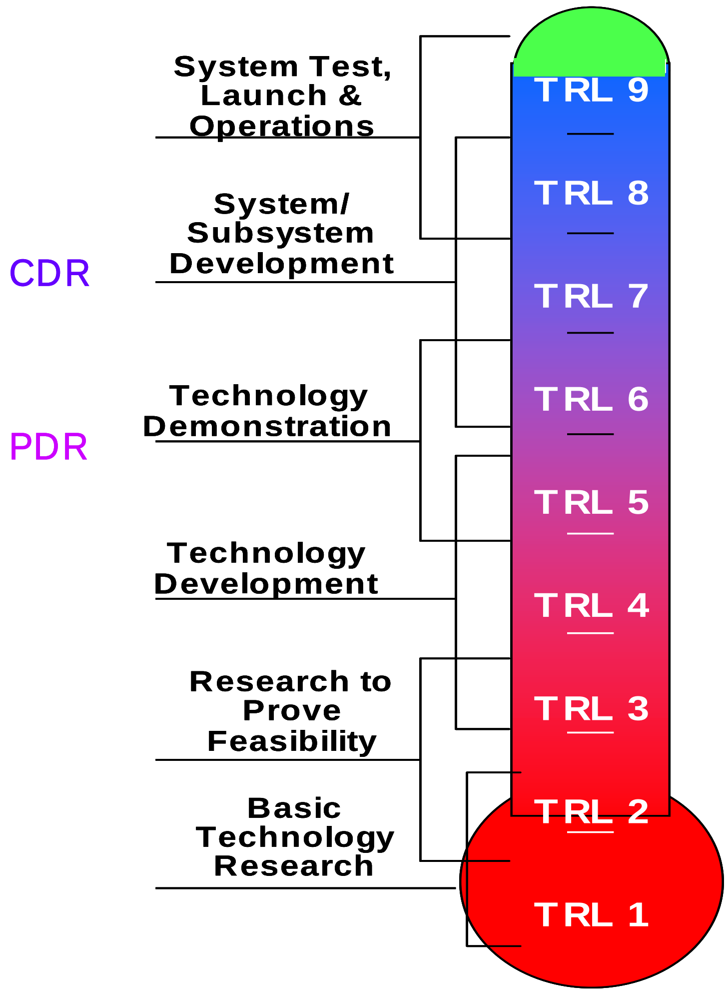


# Critical Technological Issues

- Materials
  - Processing cost
  - Reproducibility and large scale production
  - Lower microscopic defect density
- Device Processing
  - Ohmics
  - Low electro-migration metals. High-current and temperature devices.
  - Gate recess process (or lack of)
  - Via process through substrate difficult
  - Reproducibility across the wafer
  - Wafer to wafer reproducibility
- Device Performance and RF Amplifier Issues
  - Reliability. Some degrade with DC biasing alone; others show no degradation even under DC, RF and temperature stressing. Reasons for the differences are unknown.
  - Lower gain devices. Power densities pushing towards multi stage designs/hybrids possibly with GaAs based drivers (~25 dB).

# GaN Technology – TRL View




- Materials (wafer size & uniformity, yield - GaN on SiC)
  - TRL: 2-4
- Discrete Devices (including Reliability)
  - TRL: 3- 4
- MMIC designs
  - TRL: 4
- Thermal Management
  - TRL: 4-5

# GaN Insertion @ JPL

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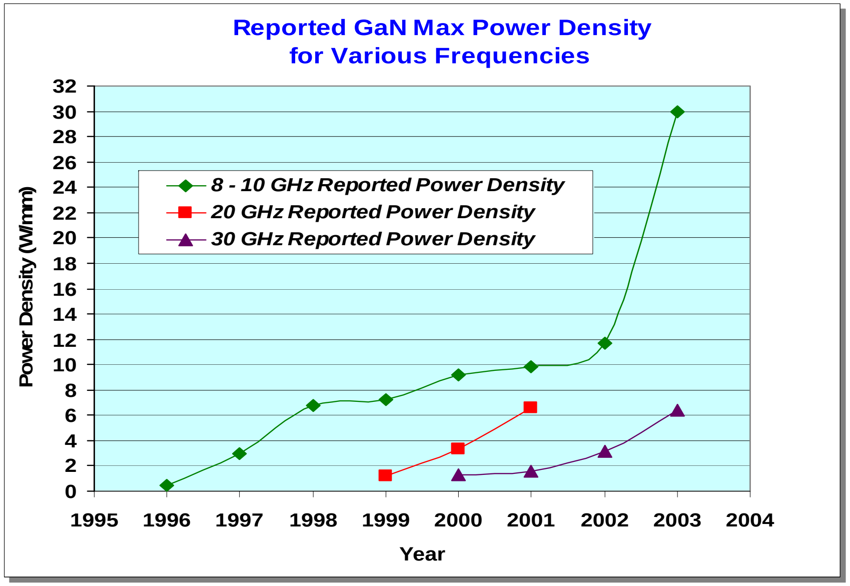
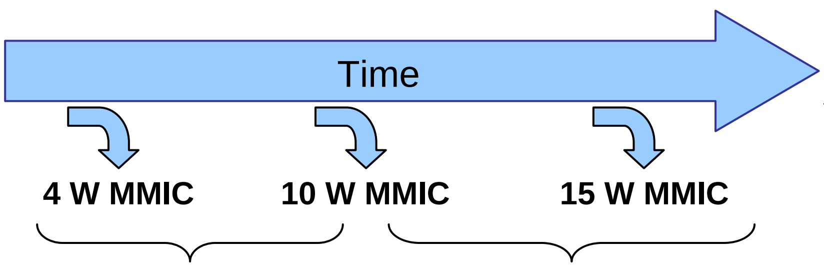



- **JPL PA architectures can accommodate a large range of MMIC powers and meet SSPA performance targets**
  - **Can evolve with device technology**
  - **Flexibility to drive up the timeline**
  - **Govt. roadmap synergistic**
- **Selection of N driven by:**
  - **MMIC availability**
  - **Insertion schedule(s)**
- **NASA insertions possible**
  - **Prometheus, Code T, Mars Technology, New Frontiers, DSN, Discovery Class**




**Early Insertion**
- **Larger number of MMICs**
- **More complex**
- **SSPA target achievable**

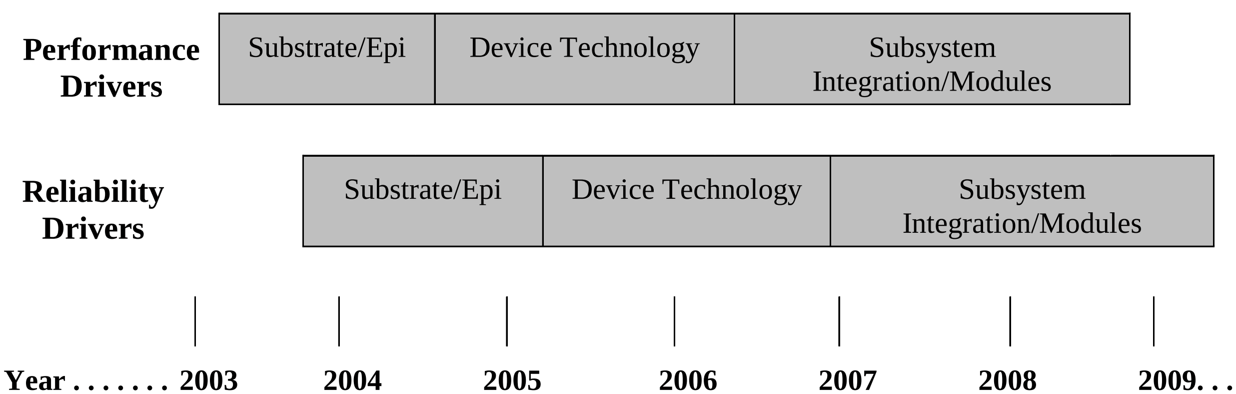
**Later Insertion**
- **More compact**
- **Better reliability**

## MMIC Summary

| Architecture | N | MMIC Power | MMIC Efficiency |
|---|---|---|---|
| Parallel Plate | 18 | 9 W | 45% |
| | 40 | 4 W | 46% |
| | 80 | 2 W | 47% |
| Waveguide Radial | 24 | 7 W | 47% |
| | 48 | 4 W | 49% |
| | 96 | 2 W | 50% |
| Waveguide Binary | 16 | 11 W | 49% |
| | 32 | 6 W | 50% |
| | 64 | 3 W | 52% |

# GaN Assessment Roadmap

- **GaN technology insertion will be successful with . . . . .**
  - **•Device performance maturation**
  - ***•Device reliability demonstration (intrinsic reliability)***
  - **•Sub - System performance maturation**
  - ***•Sub - System reliability demonstration (performance degradation with age)***




**** For NASA Missions our goal is to aggressively meet or beat this roadmap!***

**<u>Time-Lag of GaN Reliability Assessment to Technology Development</u>**

# Concluding Summary

- JPL completing hardware validations
- Roadmap report also in work
- Linearity studies and modeling ramping up
  - Need relevant measured GaN data
- Significant issues remain at the MMIC and sub-MMIC level
- Trial SSPA's at system/subsystem are feasible if:
  - We fully leverage advanced architectures
  - Accept interim performance on the road to higher compliance performers
- Benefits are:
  - Earlier assessments of broad spectrum of issues at the various level of integration
  - Performance characterizations & model development
  - Earlier mission infusion (ground and space)
  - Flexible alignment with Govt. roadmaps & timelines
- 5-8 year timelines to achieve goals (for NASA, DOD, other) appear to be achievable, but we need the staying power…