Ka-Band Wide-Bandgap
Solid-State Power Amplifier Task

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WBG SSPA Program Status Review
Aerospace Corp. El Segundo, California
September 1, 2004

UNCLASSIFIED
Program Goal
Determine feasibility of a 120–150 W Ka-band SSPA based on WBG semiconductor with an EM build in 3–5 years and FM in 7–8 years to replace TWTAs for space telecommunication

JPL investigating three architectures providing 2X to > 90X combining with target combining loss < 1 dB
- W/G Binary, W/G Radial, Parallel-Plate Radial

Deliverables
- SSPA architecture design and recommendations
- MMIC performance guidelines
- Independent assessment of GaN technology status
- Technology development roadmap through flight qualification

Progress Since Monterey Review:
- Hardware Validation of key components
  - Binary Septum combiner fabricated and measured
  - Mode transducer (for Radial) fabricated and measured
    - Radial Base nearing completion
    - Parallel Plate isolation hardware TBD
- Linearity comm architecture examination started
- MMIC packaging initiated
- Rock Systems on contract for GaN reliability
- New MMIC assy facility on schedule for end of 2004

Financial Status:
- First year funding (9 mo’s) concluded May
- Balance funding (3 mo’s) turned-on mid-July via GRC using second year funding
  - Will round out 12 month effort by FY end
  - Official second-year follow-on will support comm modeling. Will conclude CY end.

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<thead>
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<th>Tasks</th>
<th>Months after start of contract</th>
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<td></td>
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<tr>
<td>1. Architecture Identification</td>
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<td>2. Detailed Analysis</td>
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<td>3. Hardware Validation</td>
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<td>4. Technology Roadmap</td>
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<td>5. Comm/MMIC modeling</td>
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Sep 1, 2004
JPL CL# 04-1721
Power Combiners Studied

- Defined trade space and subsystem requirements
- Selected combining architectures for detailed study
  - W/G Binary, WG Radial & Parallel-Plate Radial (JPL)
- Continuing detailed electrical design
  - Prototype hardware in development
  - Target combining efficiency > 80% (< 1 dB loss)
- Defined preliminary MMIC requirements
  - 1-10 W per MMIC, > 10 dB gain, and 45%-55% PAE
- Established subcontract to evaluate WBG reliability status, identify critical path, and develop a roadmap for insertion into high-reliability applications
  - Completed technology survey

64-Way W/G Binary Combiner, 140 W SSPA Design
- -0.04 dB I.L.
- -25 dB R.L.
- -30 dB Isolation
- -0.9 total loss from MMIC to WR28 output flange including 30% margin
- Estimated Mass 1.7 kg

96-Way W/G Radial Combiner, 150 W SSPA Design
- 24-Way Prototype
- 24 cm
- 16 cm
- Hybrid-Tee Combiners Inside Base
  - -0.2 dB I.L.
  - -23 dB Isolation
- Rectangular to Circular WG Mode Converter
  - -0.14 dB I.L.
- 3.5mm Input
- Input RF Distribution
- 24 cm
- 3.5mm Input
- Estimated Mass 1.5 kg
- -1.0 dB total loss from MMIC to WR28 output flange including 30% margin

100-Way Parallel-Plate Combiner
- 50 Ohm air-coax
- Coax to RWG Transition
  - -0.1 dB I.L.
- Single 3.6 degree Sector Simulated with Symmetry Planes
- H-Wall on both sides
- Microstrip Input
- RWG Output
- -0.9 dB total loss from MMIC to WR28 output flange including 50% margin

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WBG SSPA Status Review
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Hardware Validations
Hardware Validation: Binary Combiner
Fabricated and Measured Prototype Septum Binary Combiner

Four 2X combiner prototype units were fabricated and measured

- Broadband match (>15% bandwidth)
  - Input match >25 dB
  - Output match >30 dB
- Excellent amplitude and phase balance
- Excellent unit-unit uniformity
- Good agreement with HFSS analysis
  - Differences well within fabrication tolerances

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<th>s33</th>
<th>s12</th>
<th>s13</th>
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<td>-25</td>
<td>-3.044</td>
<td>-3.065</td>
<td>-27</td>
<td>0.022</td>
<td>0.43</td>
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</table>
Breakthrough feature: Extremely low insertion loss with high isolation over a broad bandwidth.

- Measured insertion loss less than 0.05 dB (worst case)
- Measured isolation >27 dB
- Good agreement with HFSS analysis.
Millitech CSS-28 Hybrid Coupler
5% Bandwidth for equal power division
0.5 dB max insertion loss
20 dB isolation typical w/ external load

Prototype Septum Combiner
>15% Bandwidth (>3X improvement)
0.05 dB max insertion loss (10X improvement)
27 dB isolation min (30-35 dB typical)
More compact and easier layout
(Enables compact, higher-order combining)

32X combining efficiency:
94% with septum combiner
56% with conventional hybrid

Hardware Validation: Radial Combiner
Fabricated and Measured Mode Transducer

Mandrel for Electroform Process

Input: WR28/WR34
CWG TE01 Mode Diameter = 1.64 cm
Total Length: 29.3 cm

Four Marie Transducers Fabricated
- 2 x WR28 RWG input for 31 - 36 GHz
- 2 x WR34 RWG input parts for Jupiter Icy Moons Orbiter (JIMO) Mission Development (TWTAs radially power combined)
  - Technology transfer benefit to NASA
  - JIMO order decreased our WR28 part cost

Key Results:
- SN1 Match < -31.2 dB
- SN2 Match < -29.4 dB
- Good agreement for over-moded part
- Exceeds bandwidth needs
Hardware Validation: Radial Combiner
Insertion Loss Measurements of Mode Transducer

Key Results:
• Low Loss Transition < 0.19 dB
• 0.055 dB Ripple for single Mode Transducer
  • Worst Case (~ no loss)
  • Within .005 dB of requirements
➢ Measurement with Radial Base planned
  for final validation of gain ripple and mode purity

• Recall effect of trapped modes:
  Mode Transducer w/ Radial Base
  • Trapped modes cause gain and phase ripple in
    the output
  • Assuming 0.25 dB attenuation of the trapped
    mode by the radial base, 3deg phase ripple
    requires spurious modes be < -25 dB relative to
    the desired mode

Back-to-Back Mode Transducer Measurement

S21 WR28 part: back-to-back

Frequency (GHz)

0 0.00 0.05 0.10 0.15 0.20 0.25 0.30 0.35 0.40 0.45 0.50 0.55 0.60 0.65 0.70 0.75 0.80 0.85 0.90 0.95 1.00

dB

-0.00 -0.10 -0.20 -0.30 -0.40 -0.50 -0.60 -0.70 -0.80 -0.90 -1.00

S21 measured SN1 and
SN2

Meas. Insertion Loss

dB(S(cwg:3 wr28:1))
Hardware Validation Summary

• Validated waveguide conductor loss versus plating types onto Aluminum
  – WR28 loss with silver plating (0.19 dB/ft) was ~20% lower compared to loss
    with gold plating (0.24 dB/ft).
  – Chemical polishing of metal surface prior to plating reduced loss by an
    additional 5%.
  ➢ Allows low mass construction from Aluminum

• Validated septum combiner design for waveguide binary architecture
  – Good agreement between analysis and measurement

• Completed fabrication of circular to rectangular waveguide to circular
  waveguide mode transducer for radial architecture
  – Exceeded bandwidth requirements

• Fabrication of Radial Base nearly complete
  – Measurements will determine phase ripple

• Completed electrical design of a novel port-to-port isolation structure for
  parallel-plate radial architecture
  – Hardware validation TBD
MMIC Data for Linearity Study
Comm Marching Orders

- Will combine multiple power MMICs
- May need 2-3 driver/gain stages to achieve 50 dB gain
- Customer desires “advanced digital modulation,” e.g. QAM, but cannot backoff significantly to operate in linear regime; efficiency is King.
- We may be able to provide candidate MMIC performance, expected combiner performance, etc.
- What linearization technique best at Ka-band? Should we just use existing digital predistorters (e.g., Lintech)? Bias modulation?
- How will amplitude/phase balance, # stages, etc., affect
  - Linearity
  - AM/PM conversion
  - Link performance?
Commercial MMIC Eval

- Examined commercial Tri-Quint device for modeling of linearity
  - Don’t have measured GaN MMIC data, yet
- Used preliminary data/assumptions for doing linearity simulations:
  - Amplitude response from data sheet
    - 5th order poly fit coefficients included in plot below
  - Phase response from SSPA extrapolation
    - 4th order poly fit coefficients included in plot
  - Frequency response: flat over 31-36 GHz 3dB BW
- Comm system folks used data for a first look, and as leg stretcher.
Preliminary Evaluation of Higher Order Modulations in the Presence of Non-Linearities
Modulation Types Under Investigation

- Examined two higher order QAM-like modulations for performance under instantaneous non-linearities
  - APSK-16 (12/4 QAM)
  - APSK-32 (16/12/4 QAM)
  - Modulation descriptions based upon DVB S2 proposed standard
- Examined performance of QPSK for baseline performance validation
- Constellations represent noiseless matched filter outputs of 35% excess bandwidth square root raised cosine pulse shaping filters passed through MMIC memoryless nonlinearities (AM-AM, AM-PM)
- Waveform peak is approximately 2 dB above 1 dB compression point
- Pulse shape distortion and AM-PM effects noticeable

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1. Characterization based on Triquint TGA4514-EPU
• Degradation limited to approximately 1 dB compared to ideal waveform detection for an average PAE of 12% and lower
• Phase and amplitude distortion of outer constellation ring likely cause of increasing losses under higher gain compression
• Statistical (e.g. histogram) analysis of symbol error distribution may localize main error contributions
• Possible mitigation techniques include “simple” linearization in amplitude and/or phase
At maximum MMIC amplifier efficiency (peak IBO approx. +8 dB), performance degradation is slightly above 1 dB.

PAE improvement at peak IBO of +8 dB is offset by performance degradation relative to peak IBO of +4 dB operating point.
QPSK Performance

- QPSK exhibits negligible loss when operating in saturation regime of the MMIC amplifier
Possible Next Steps

- Increased fidelity performance characterization
  - Uncoded bit error rate
  - Modulation integrated with high performance forward error correction (FEC)
- Incorporate modular architecture to non-linearity performance analysis
  - Model as \( N \) equally combined amplifiers
  - Introduce parametric errors to amplifier gain and phase curves
  - Characterize errors via statistical distributions
- Assess output spectral regrowth for regulatory/non-interference compliance
  - Spectral mask compliance
  - Adjacent/Co-channel interference analysis
- Examine fixed and adaptive non-linear compensation techniques
  - Single input “average” compensation
  - Multiple input (not necessarily \( N \)) “tailored” compensation
- Incorporate any needed frequency selective modeling and compensation
  - Transmitter
  - Receiver
RELIABILITY DRIVERS
Incorporate Recess-Topology Structures to reduce leakage-current degradation effect

Addition of a Field-Plate to reduce Electric-Field degradation affect

**Performance Drivers**

**GaN Reliability**

<table>
<thead>
<tr>
<th>Performance area under investigation</th>
<th>Parameter / Method to Affect Change in Performance</th>
</tr>
</thead>
</table>
| Gate Leakage Current                 | • Adjust metallization material or barrier layer material  
                                       • Improve dislocations in substrate interface or adjust nucleation layer. |
| Drain Leakage Current                | • Improve material quality                        |
| Electric-Field degradation (dispersion) | • Create a layered structure in the gate-drain region  
                                         • Recess gate  
                                         • Add a field-plate at the gate  
                                         • Add a p-doped cap layer between the gate and drain |
| Channel Temperature                  | • Optimize efficiency of device versus power density  
                                         • Optimize geometry of device periphery layout (fingers and spacing) |
### GaN Reliability

#### Reliability Test Methodology and Metrics

**Accelerated Life-Test Paradigms**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Methodology</th>
<th>Characterization Test Level</th>
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<tbody>
<tr>
<td>Ohmic-contact Resistance</td>
<td>Temperature Dependence</td>
<td>Intrinsic</td>
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<tr>
<td>Leakage-Current</td>
<td>Temperature Dependence</td>
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</tr>
<tr>
<td>Transconductance</td>
<td>Temperature Dependence</td>
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</tr>
<tr>
<td>Forward-Voltage Turn-On</td>
<td>Temperature Dependence</td>
<td>Intrinsic</td>
</tr>
<tr>
<td>Reverse-Bias Breakdown-Voltage</td>
<td>Temperature Dependence</td>
<td>Intrinsic</td>
</tr>
<tr>
<td>Metal Migration</td>
<td>Static Aging</td>
<td>Intrinsic</td>
</tr>
<tr>
<td>Forward-Voltage Turn-On</td>
<td>Dynamic Aging</td>
<td>Device</td>
</tr>
<tr>
<td>Specific-On Resistance</td>
<td>Dynamic Aging</td>
<td>Device</td>
</tr>
<tr>
<td>DC &amp; RF Transconductance</td>
<td>Dynamic Aging</td>
<td>Device</td>
</tr>
<tr>
<td>Reverse-Bias Breakdown Voltage</td>
<td>Dynamic Aging</td>
<td>Device</td>
</tr>
<tr>
<td>Saturated RF Output Power</td>
<td>Dynamic Aging</td>
<td>Device</td>
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</table>
ROADMAP ISSUES
Roadmap Considerations

- JPL Report Construct
  - Challenges
  - Requirements levied on tech dev
  - Cross-cutting issues
  - Potential solutions & pathways

- Materials & Device Performance

- MMIC Development Critical
  - Supporting developments not quite there
  - Production level reliability yields needed

- Reliability & Space Qual
  - Some promising early data
  - Need to learn from GaAs evolution

- Follow-on Proof-of-Concepts
- Performance Trials
- TRL Maturation
Critical Technological Issues

- Materials
  - Processing cost
  - Reproducibility and large scale production
  - Lower microscopic defect density

- Device Processing
  - Ohmics
  - Low electro-migration metals. High-current and temperature devices.
  - Gate recess process (or lack of)
  - Via process through substrate difficult
  - Reproducibility across the wafer
  - Wafer to wafer reproducibility

- Device Performance and RF Amplifier Issues
  - Reliability. Some degrade with DC biasing alone; others show no degradation even under DC, RF and temperature stressing. Reasons for the differences are unknown.
  - Lower gain devices. Power densities pushing towards multi stage designs/hybrids possibly with GaAs based drivers (~25 dB).
GaN Technology – TRL View

- Materials (wafer size & uniformity, yield - GaN on SiC)
  - TRL: 2-4
- Discrete Devices (including Reliability)
  - TRL: 3-4
- MMIC designs
  - TRL: 4
- Thermal Management
  - TRL: 4-5
GaN Insertion @ JPL

- JPL PA architectures can accommodate a large range of MMIC powers and meet SSPA performance targets
  - Can evolve with device technology
  - Flexibility to drive up the timeline
  - Govt. roadmap synergistic
- Selection of N driven by:
  - MMIC availability
  - Insertion schedule(s)
- NASA insertions possible
  - Prometheus, Code T, Mars Technology, New Frontiers, DSN, Discovery Class

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**MMIC Summary**

- **Early Insertion**
  - Larger number of MMICs
  - More complex
  - SSPA target achievable
- **Later Insertion**
  - More compact
  - Better reliability

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**Reported GaN Max Power Density for Various Frequencies**

- 8 - 10 GHz Reported Power Density
- 20 GHz Reported Power Density
- 30 GHz Reported Power Density

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**Architecture Summary**

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<th>Architecture</th>
<th>N</th>
<th>MMIC Power</th>
<th>MMIC Efficiency</th>
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<td>18</td>
<td>9 W</td>
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<td>4 W</td>
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<td>11 W</td>
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<tr>
<td></td>
<td>32</td>
<td>6 W</td>
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</tr>
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<td></td>
<td>64</td>
<td>3 W</td>
<td>52%</td>
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GaN Assessment Roadmap

- GaN technology insertion will be successful with . . . .
  - Device performance maturation
  - Device reliability demonstration (intrinsic reliability)
  - Sub - System performance maturation
  - Sub - System reliability demonstration (performance degradation with age)

For NASA Missions our goal is to aggressively meet or beat this roadmap!

*Time-Lag of GaN Reliability Assessment to Technology Development*

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<th>Substrate/Epi</th>
<th>Device Technology</th>
<th>Subsystem Integration/Modules</th>
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Concluding Summary

- JPL completing hardware validations
- Roadmap report also in work
- Linearity studies and modeling ramping up
  - Need relevant measured GaN data
- Significant issues remain at the MMIC and sub-MMIC level
- Trial SSPA’s at system/subsystem are feasible if:
  - We fully leverage advanced architectures
  - Accept interim performance on the road to higher compliance performers
- Benefits are:
  - Earlier assessments of broad spectrum of issues at the various level of integration
  - Performance characterizations & model development
  - Earlier mission infusion (ground and space)
  - Flexible alignment with Govt. roadmaps & timelines
- 5-8 year timelines to achieve goals (for NASA, DOD, other) appear to be achievable, but we need the staying power…