

Reliability Assessment of Advanced
Flip-Chip Interconnect Electronic
Package Assemblies under Extreme Cold
Temperatures (-190°C and -120°C)

Rajeshuni Ramesham,

Reza Ghaffarian, and Andrew Shapiro

Jet Propulsion Laboratory, Caltech, Pasadena.

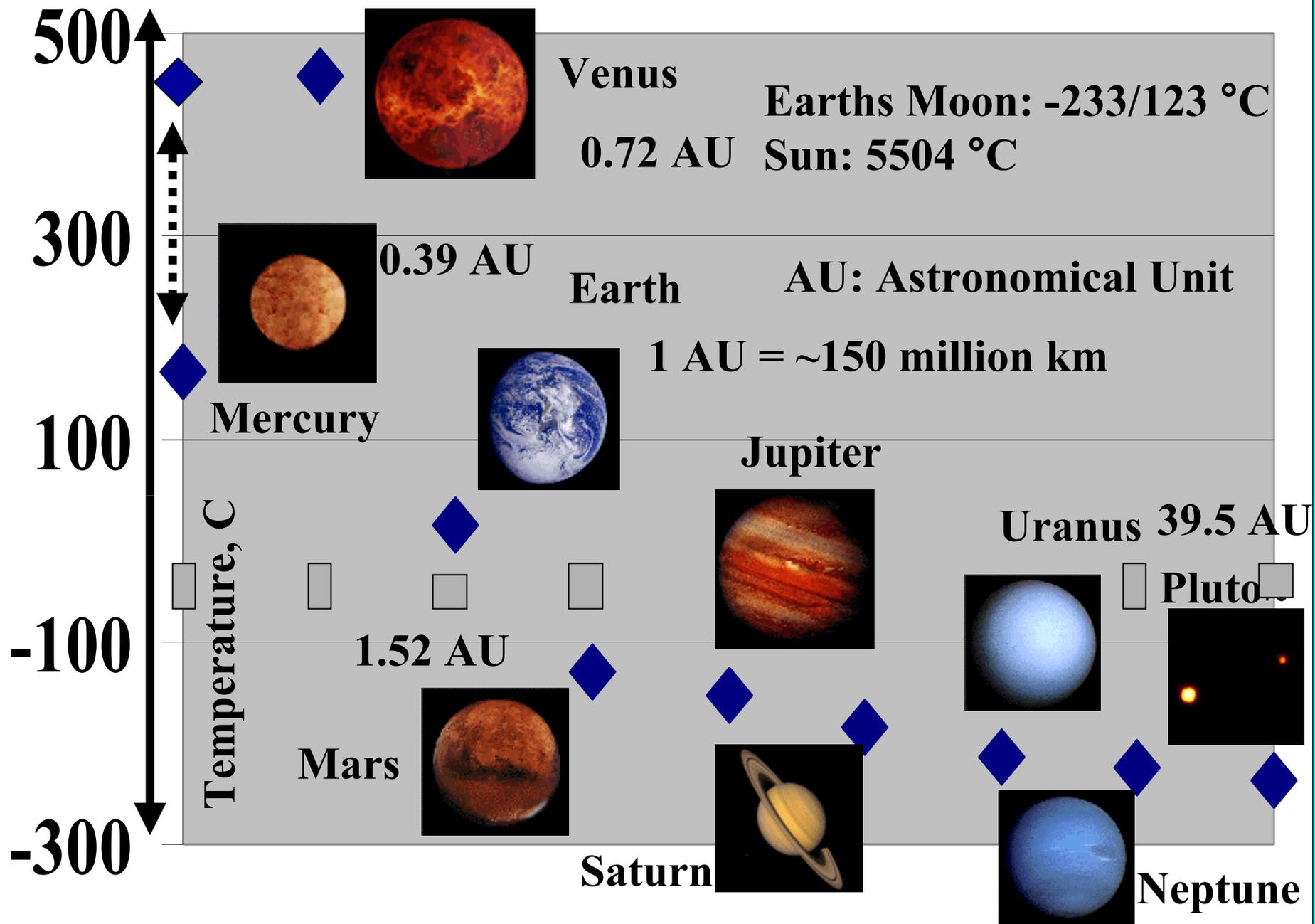
Phil A. Napala, Patrick A. Martin

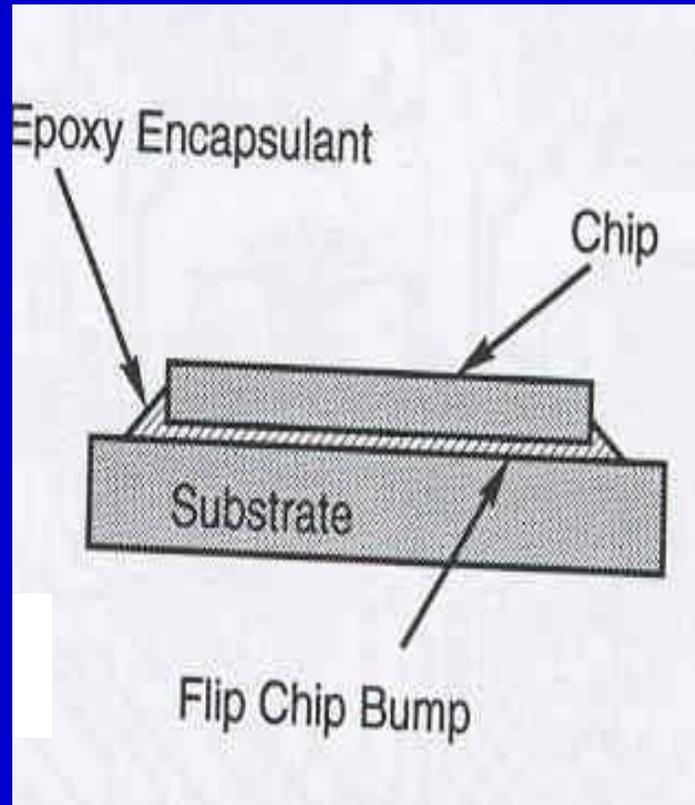
Office of Safety and Mission Assurance

NASA HQ

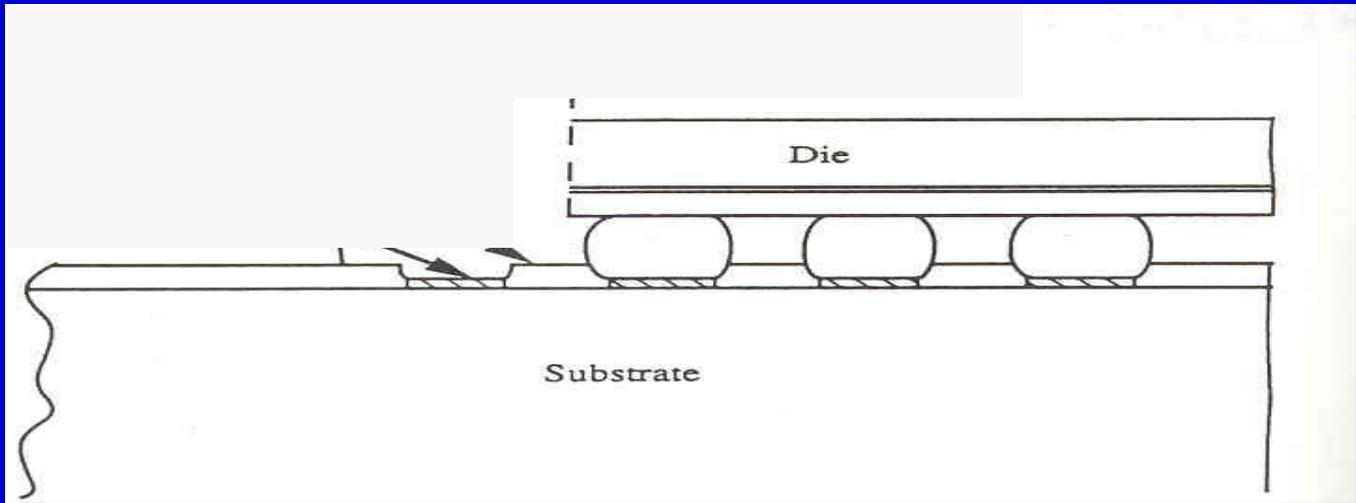
OUTLINE

- Objective
- Introduction
- Test articles
- Experimental data
- Results and discussion
- Conclusions
- Acknowledgements





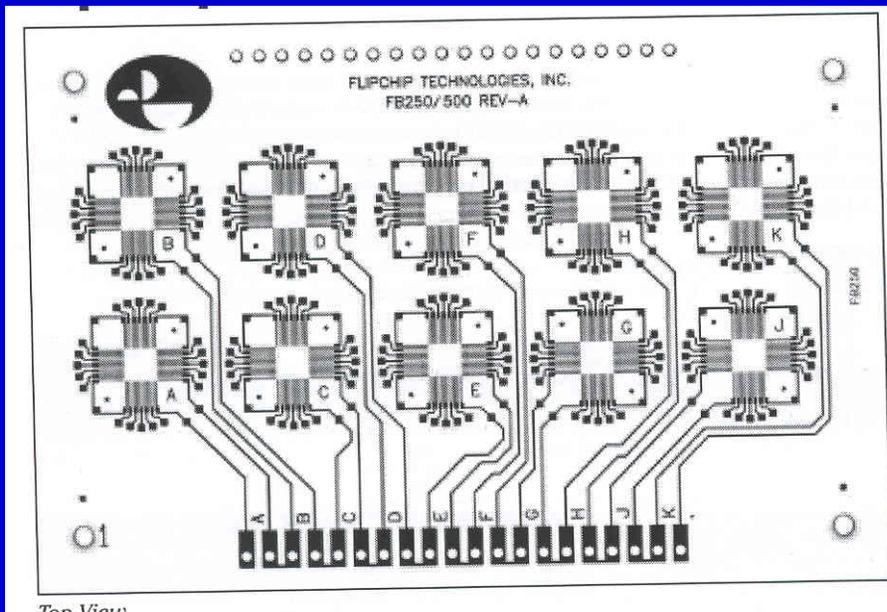
Schematic of the Flip-chip attachment and the chip



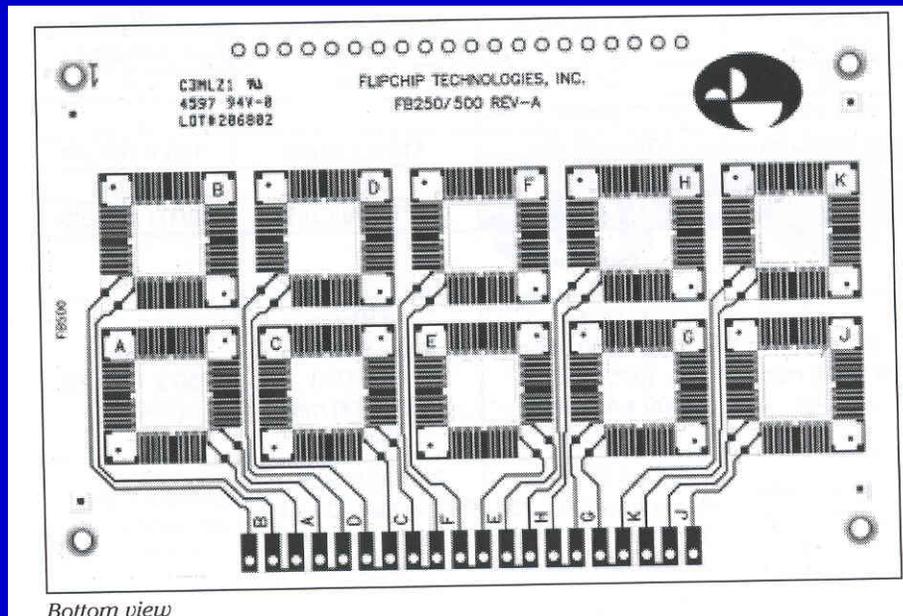
Flip-chip bond structure

Test article details

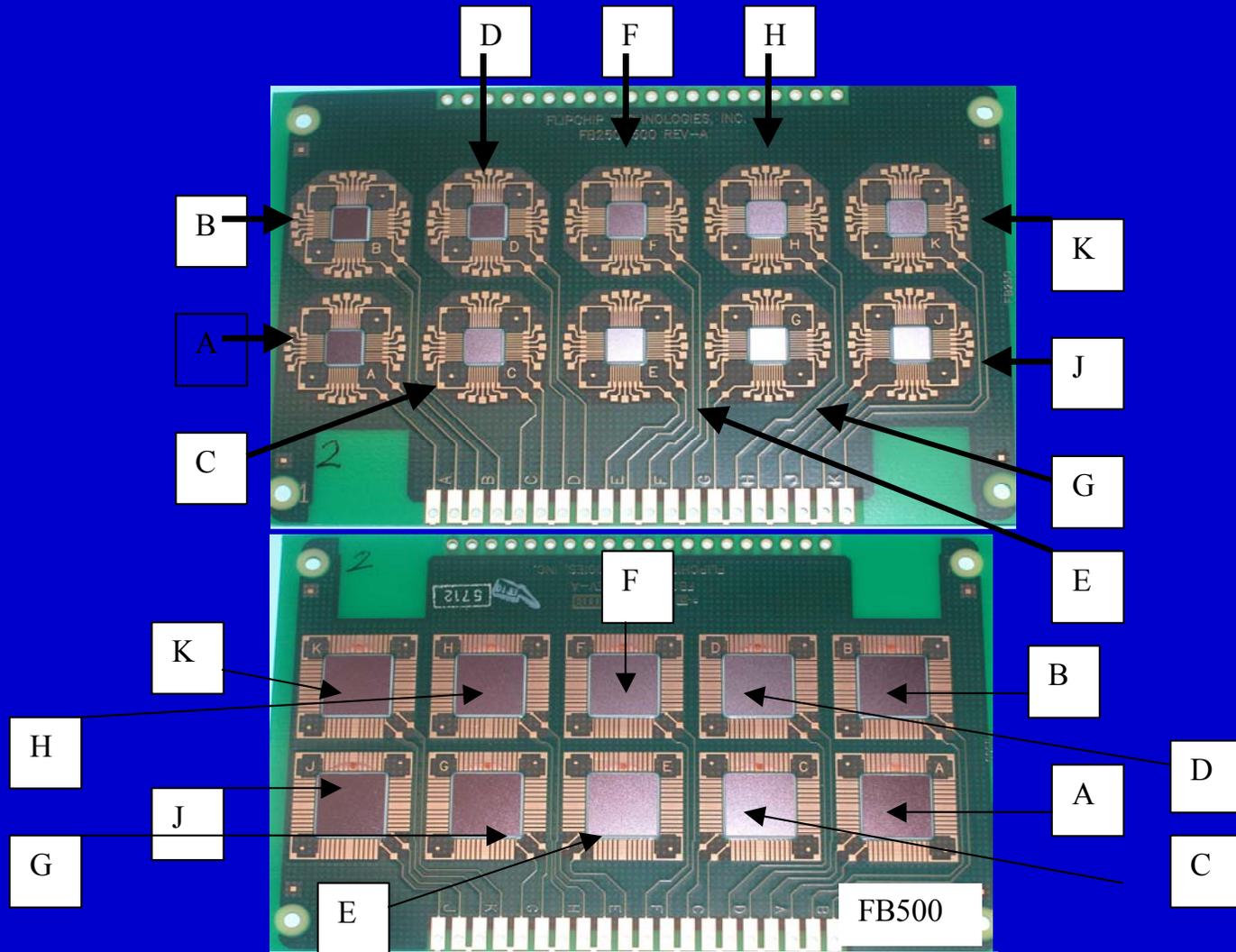
- FB250 and FB500 test boards
- Test board material: FR4
- Tg: 176°C, 0.031" thick, copper conductor, Taiyo PSR-400 solder mask
- **FB250 board:** 10 chips of 250 x 250 mil², 18 mil pitch.
- **FB500 board:** 10 chips of 500 x 500 mil², 18 mil pitch.



Topside of the board



Bottomside of the board



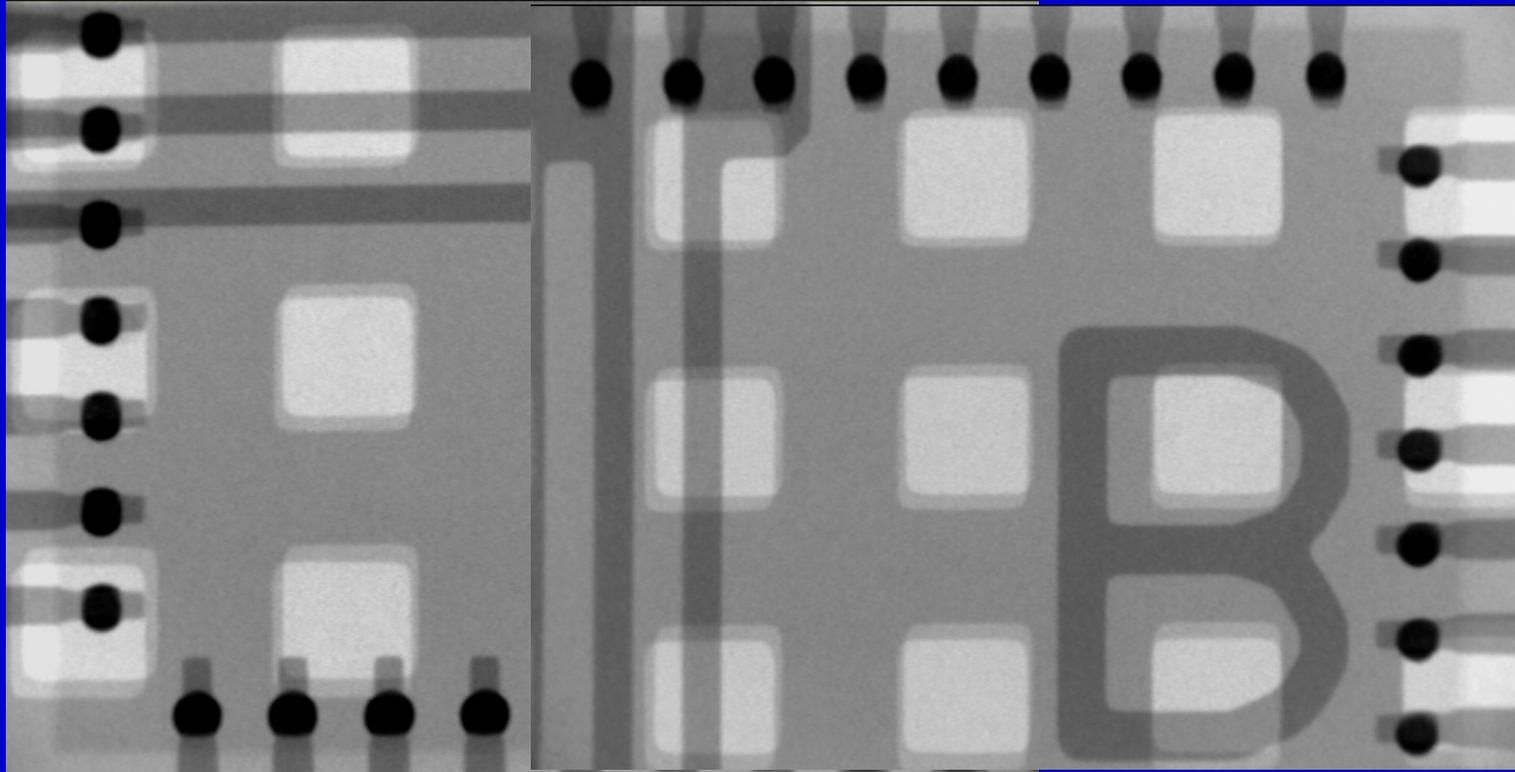
Optical photographs of the assembled advanced flip-chip Interconnect test boards of FB250 and FB500

Underfill	Stage temp.C	Air Pressure (psi)	Needle gauge	RPM	Line speed (in/sec)
RDP-960	80	6	#23	250	0.08

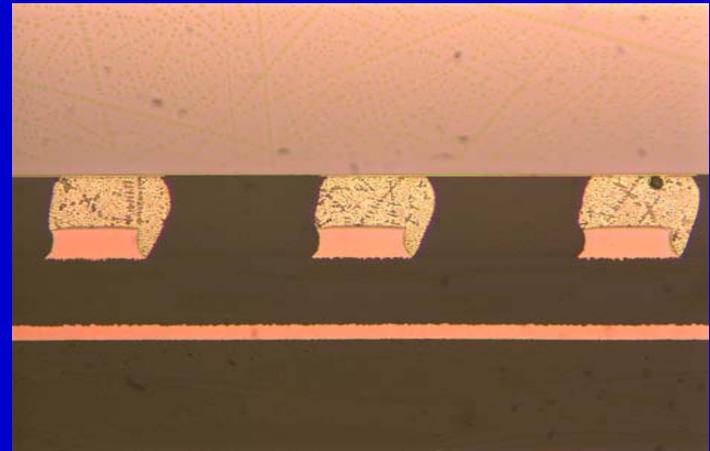
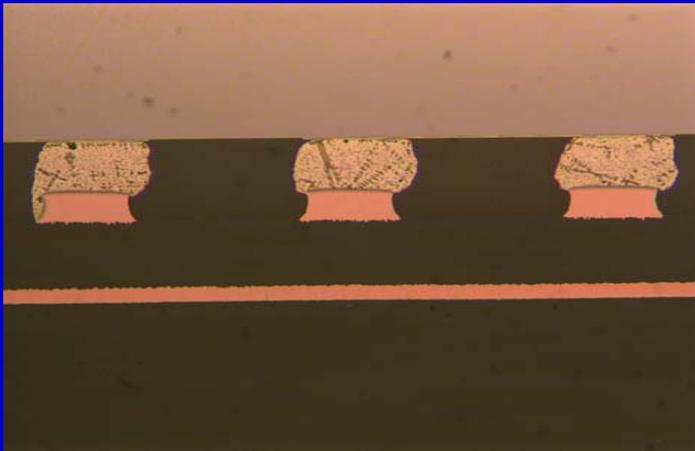
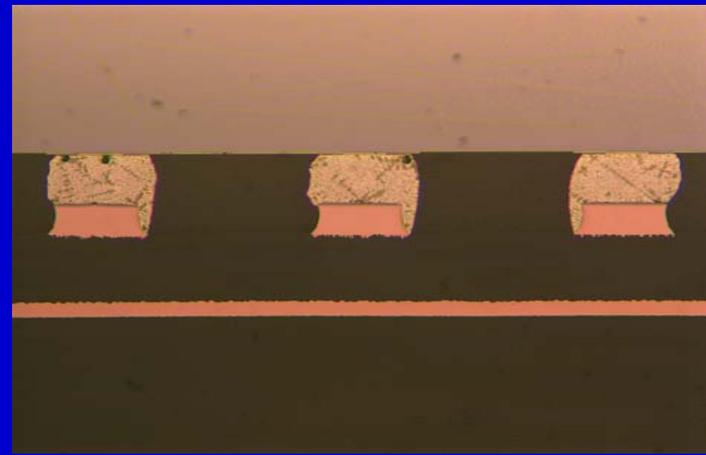
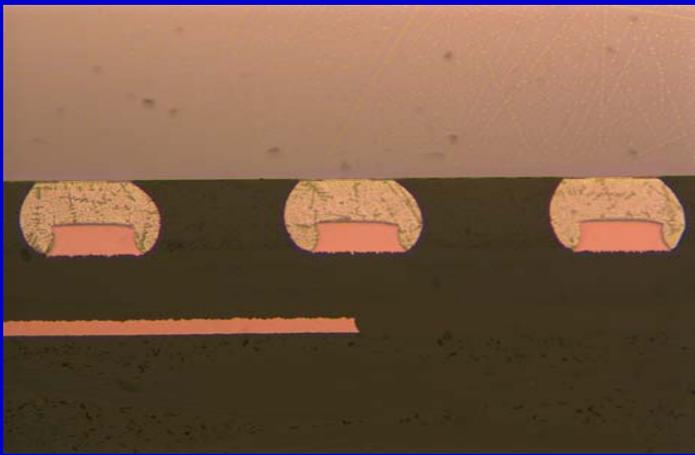
Parameters for underfill component FB500

Underfill	Stage temp.C	Air Pressure (psi)	Needle gauge	RPM	Line speed (in/sec)
RDP-960	100	6	#23	250	0.08

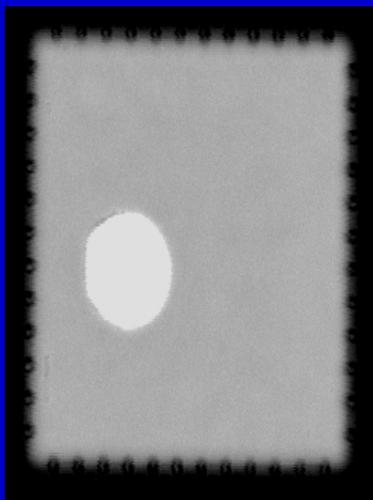
Parameters for underfill component FB250



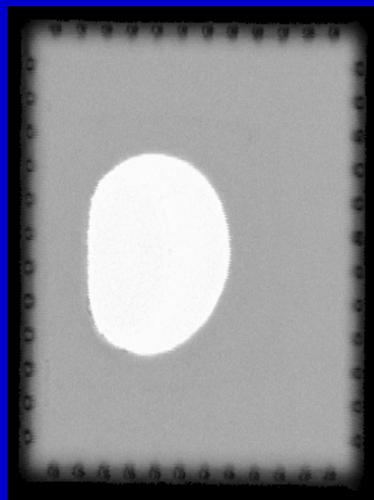
X-Ray image of solder wetting after reflow



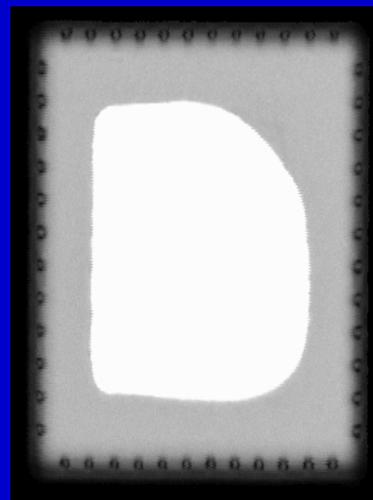
Cross section images of top right corner viewing from chip side



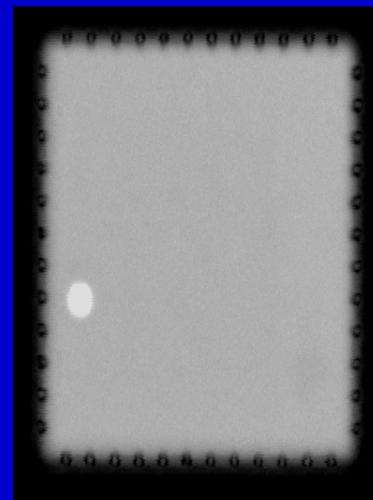
Board1_D



Board5_E

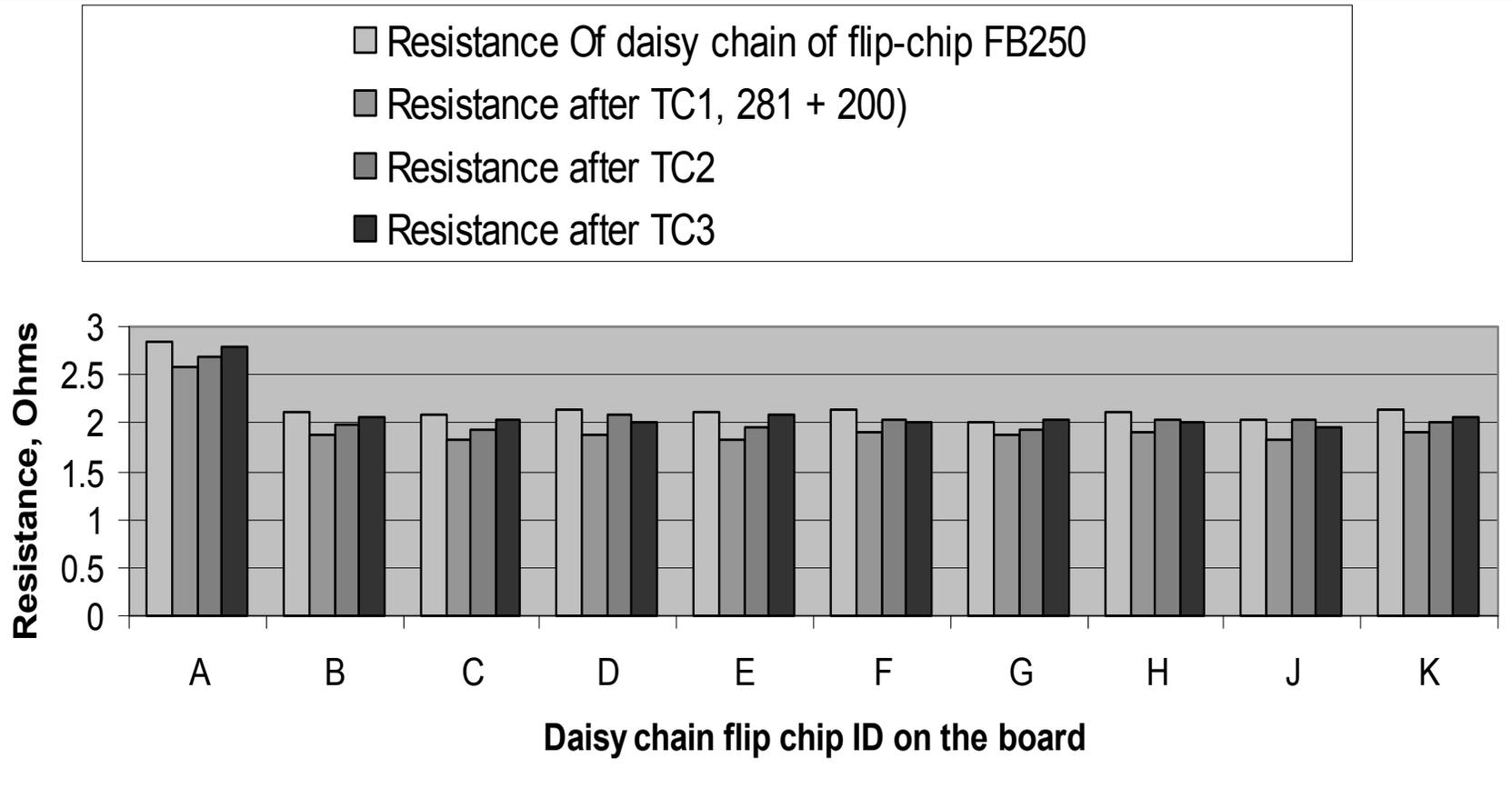


Board7_D

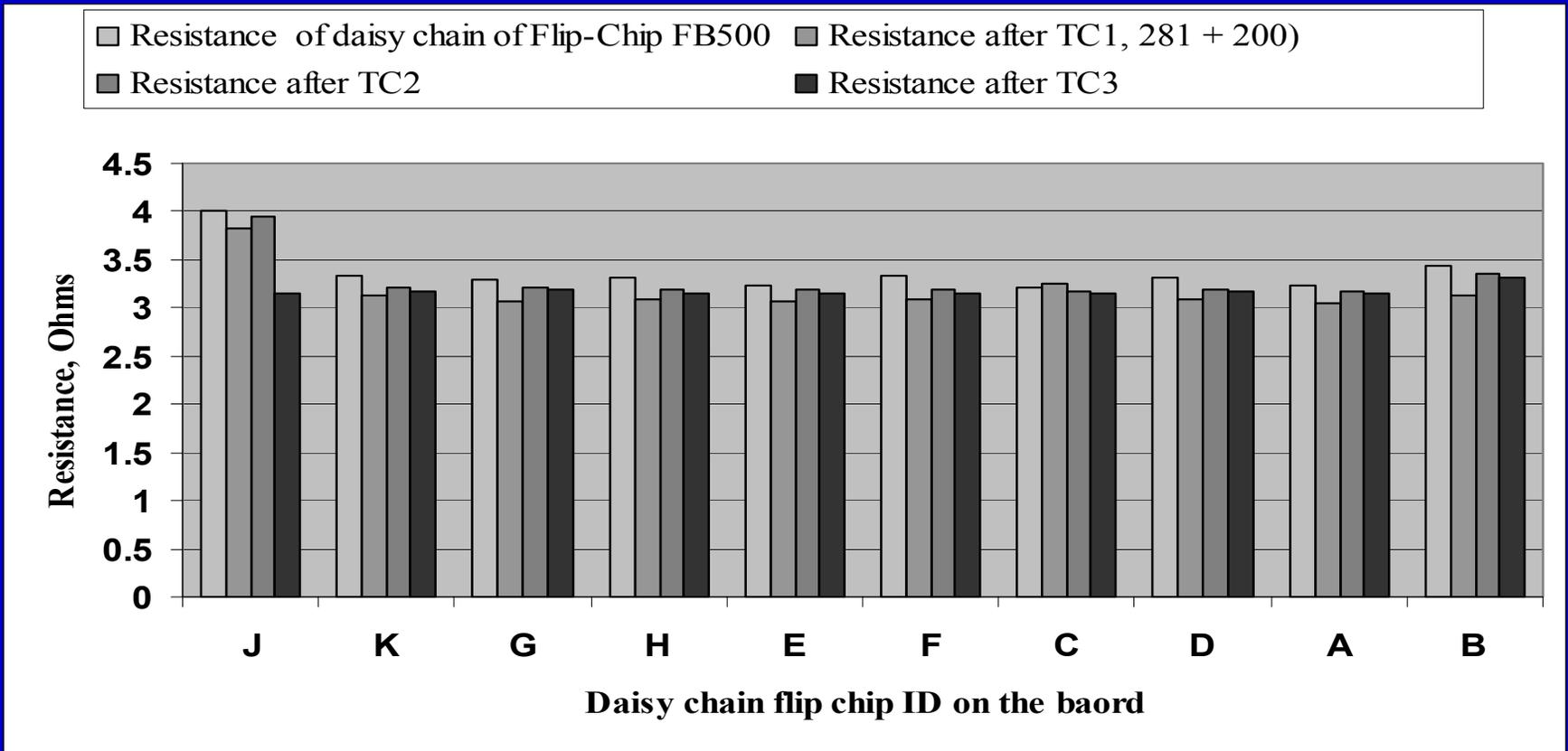


Board7_F

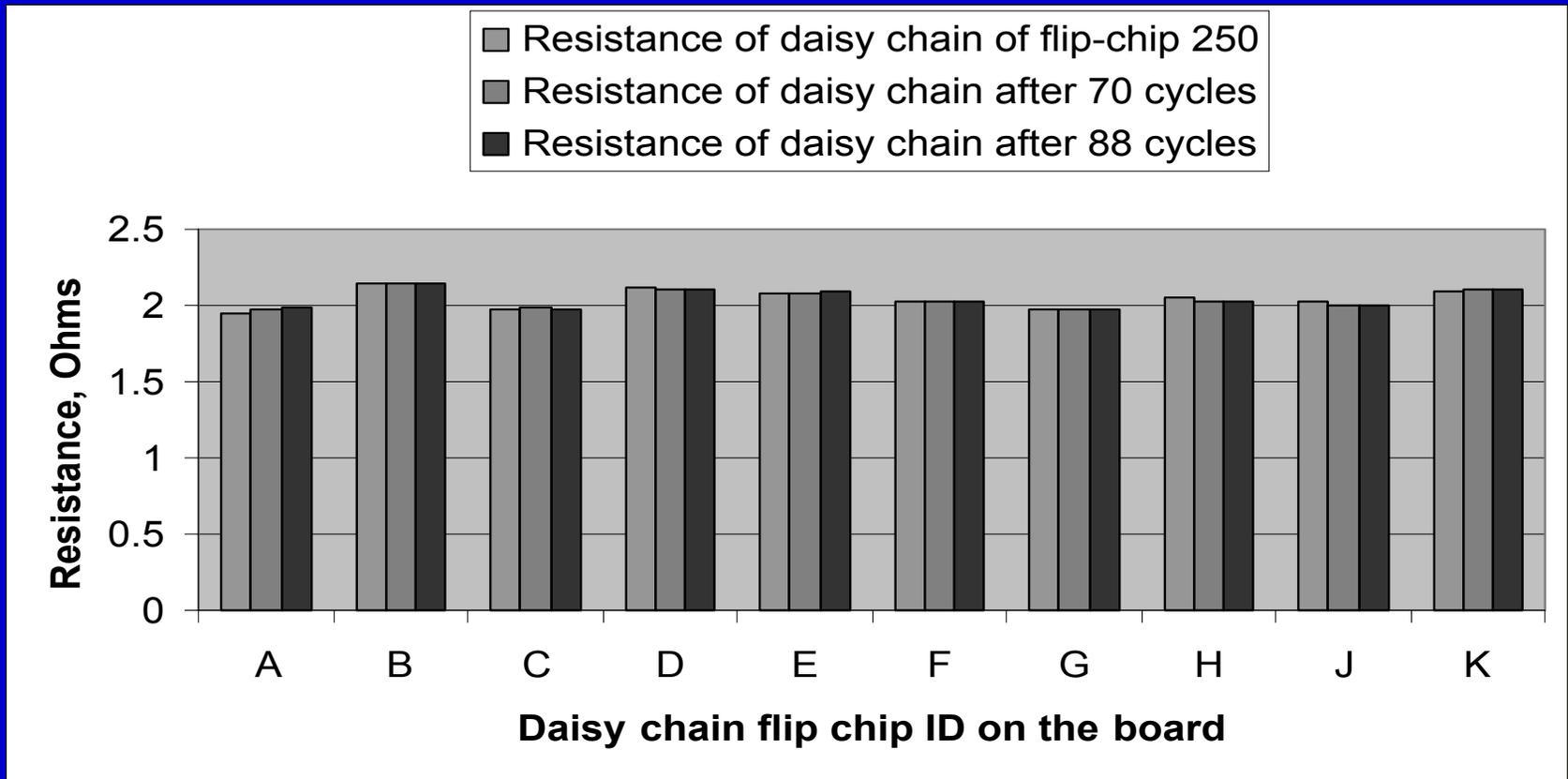
CSAM images of underfill with voids



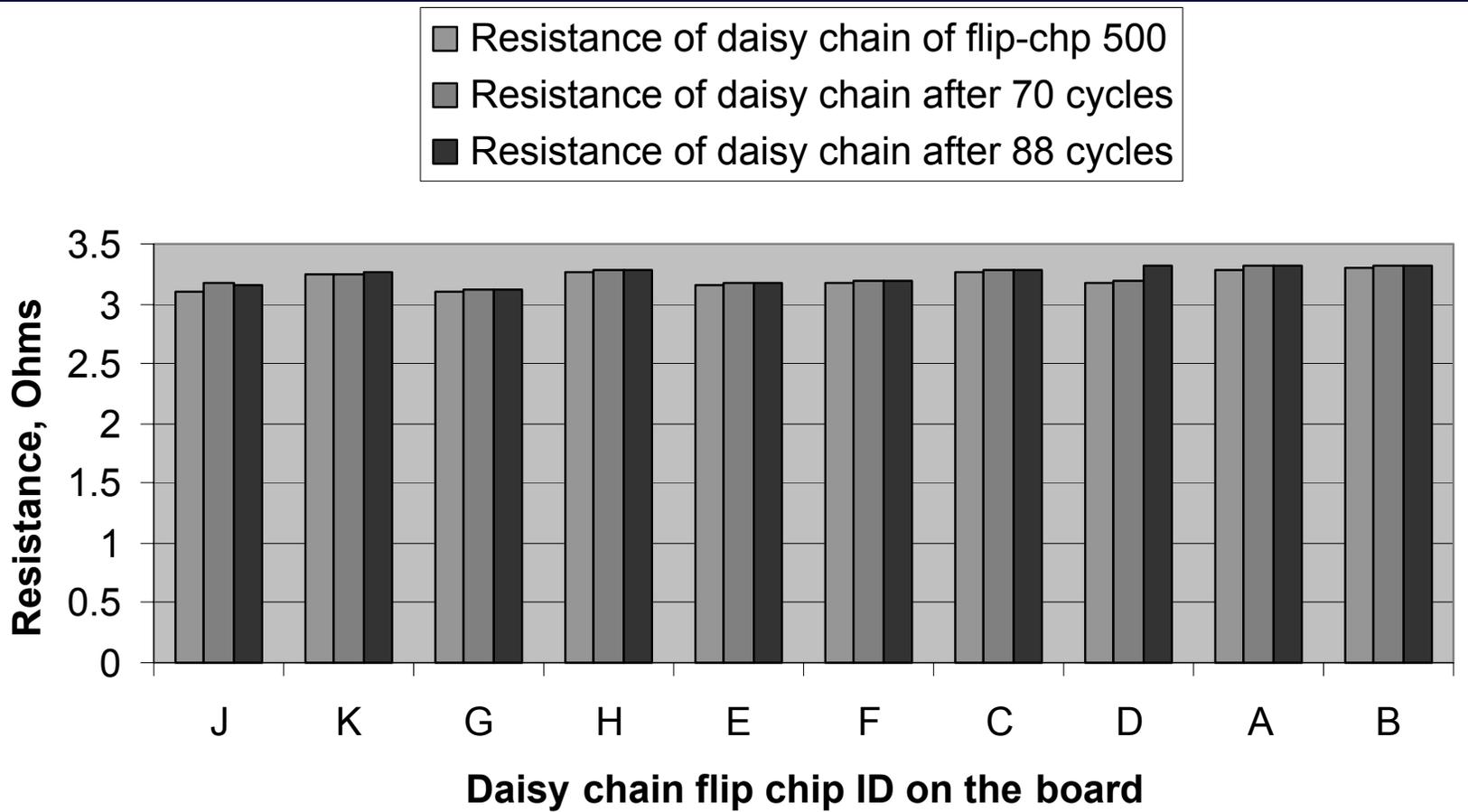
Resistance of daisy chains such as A,B,C,D,E,F,G,H,J,K of flip-chip FB250 test board. A. Measured resistance at room temperature, b. resistance measured after 481 thermal cycles -120°C to 115°C and -120°C to 85°C (TC1), c. Resistance measured after 200 thermal cycles -55°C to 100°C (TC2), and d. Resistance measured after 311 thermal cycles -125°C to 85°C (TC3).



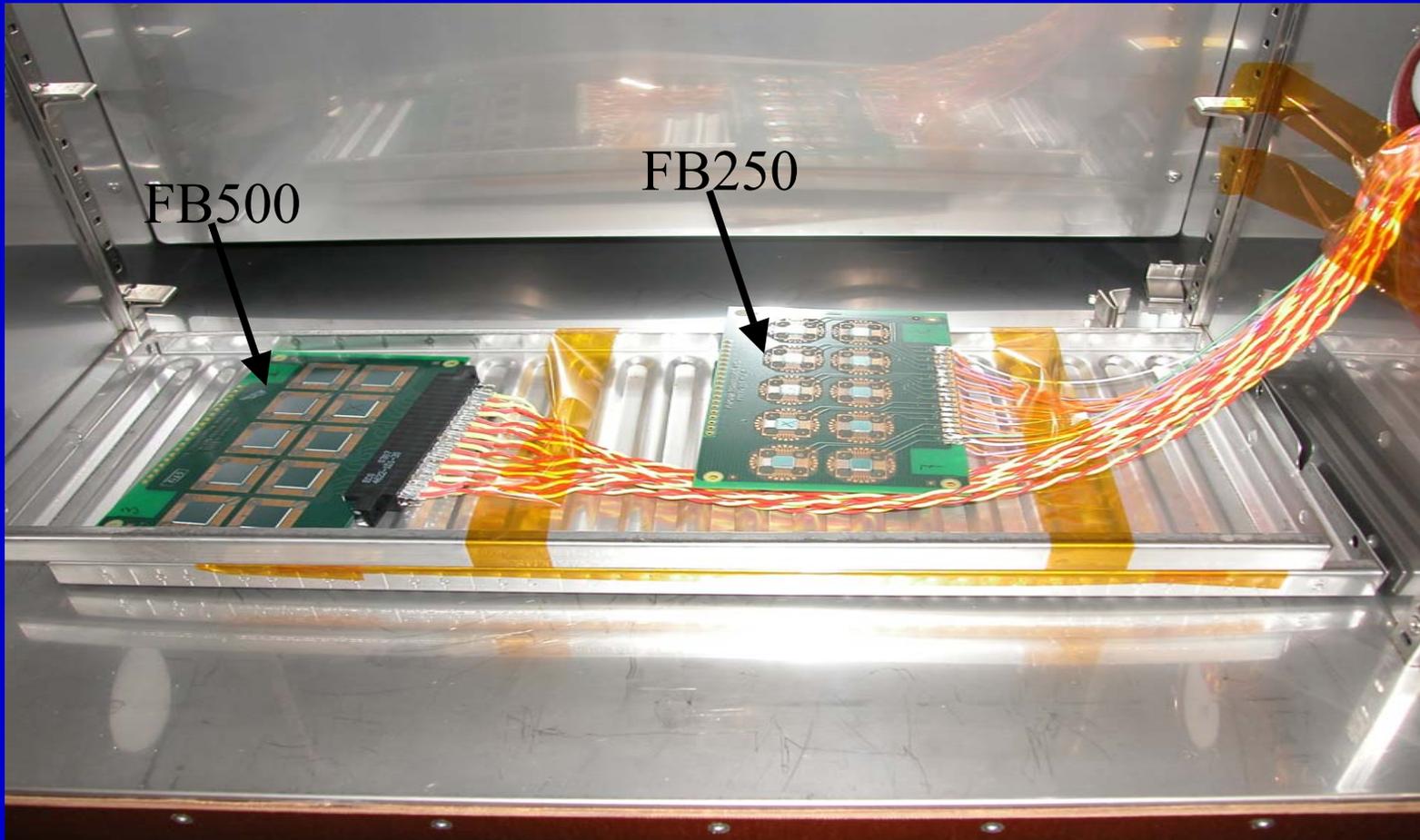
Resistance of the daisy chains such as J,K,G,H,E,F,C,D,A,B of flip-chip FB500 test board. A. Resistance of the pair at room temperature, b. resistance of the pairs measured after 481 thermal cycles -120°C to 115°C and -120°C to 85°C (TC1), and c. Resistance of the pairs measured after 200 thermal cycles -55°C to 100°C (TC2) and d. Resistance of the pairs measured after 311 thermal cycles -125°C to 85°C (TC3).



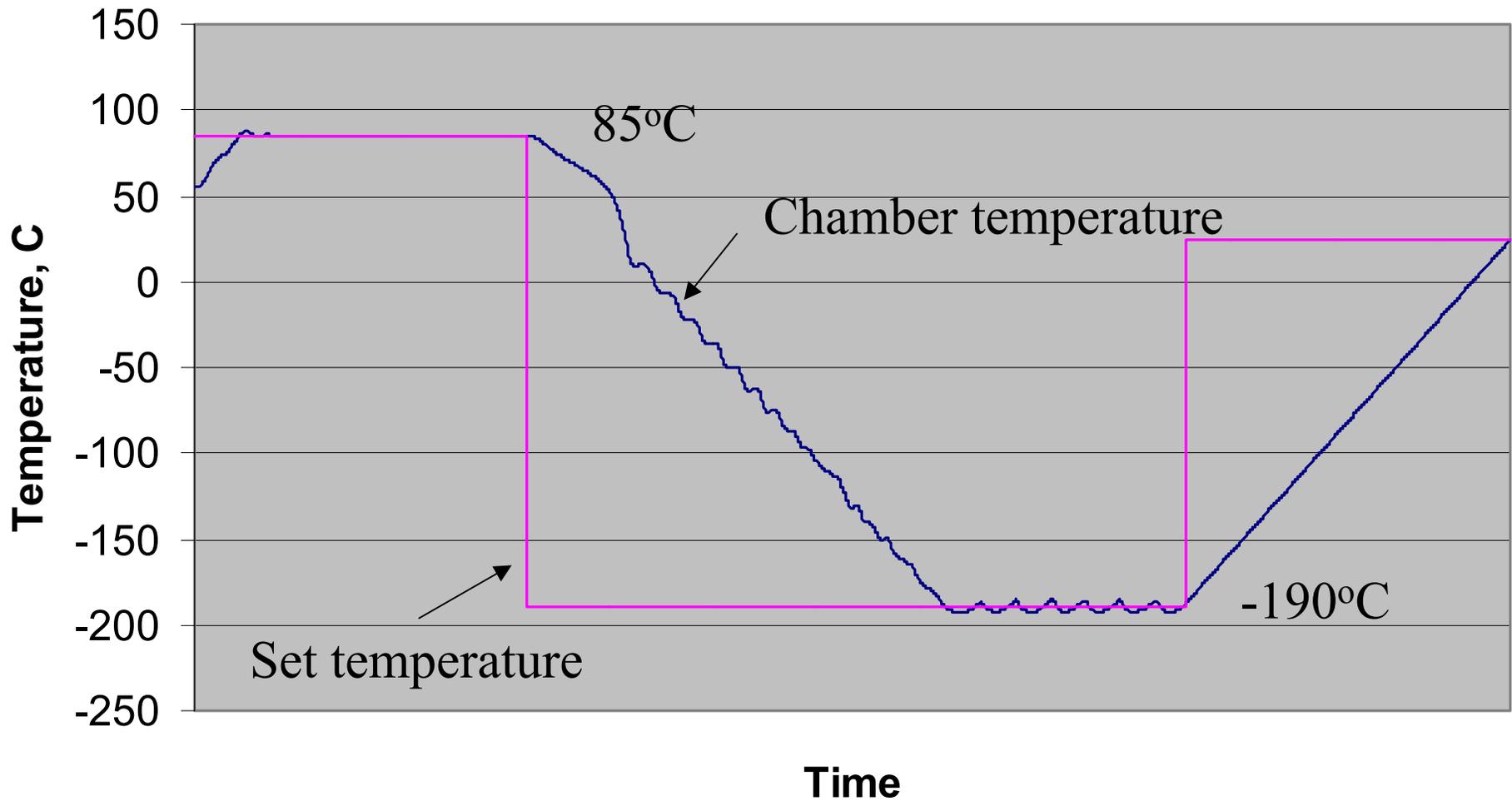
Resistance of the daisy chains such as A,B,C,D,E,F,G,H,J,K of flip-chip FB250 test board. a. Resistance of the daisy chains at room temperature, b. resistance of the daisy chains measured after 70 thermal cycles (-190°C to 25°C) and c. Resistance of the daisy chains measured after 88 thermal cycles (-190°C to 25°C).



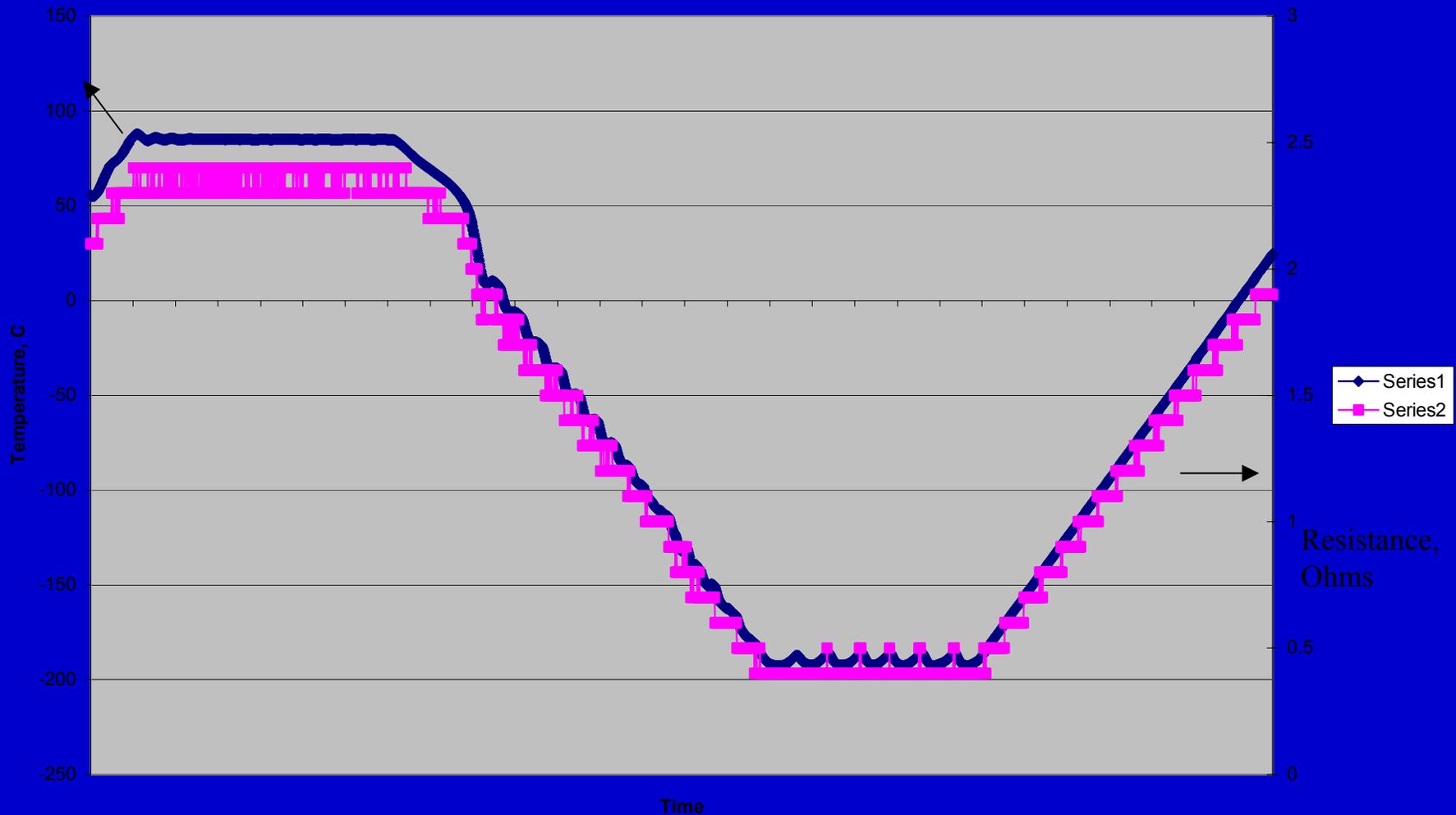
Resistance of daisy chains such as J,K,G,H,E,F,C,D,A,B of flip-chip FB500 test board. A. Resistance of the daisy chains at room temperature, b. resistance of the daisy chains measured after 70 thermal cycles (-190°C to 25°C) and c. Resistance of the daisy chains measured after 88 thermal cycles (-190°C to 25°C).



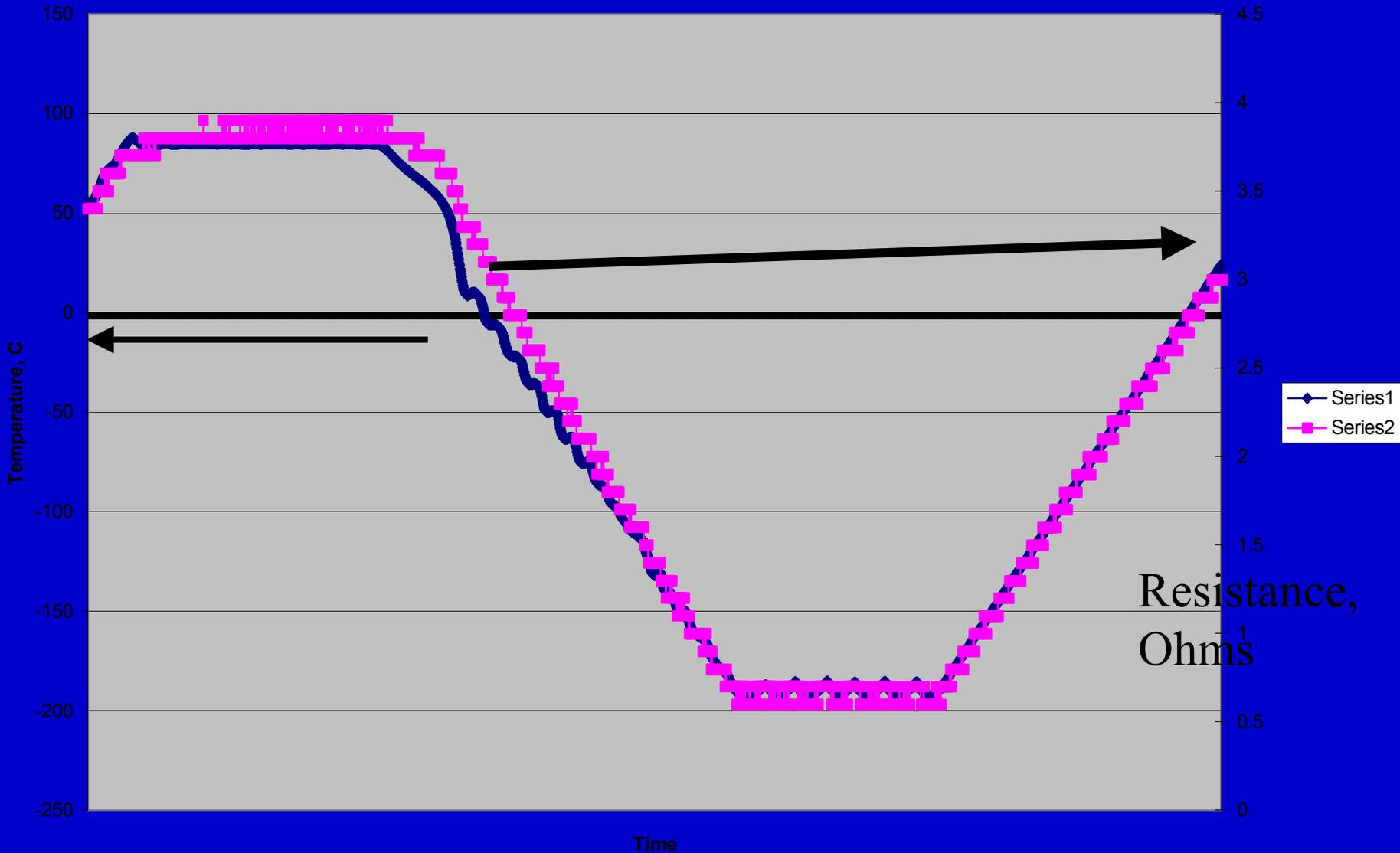
Flip-chip boards with electrical leads in the thermal chamber to monitor daisy chain resistance



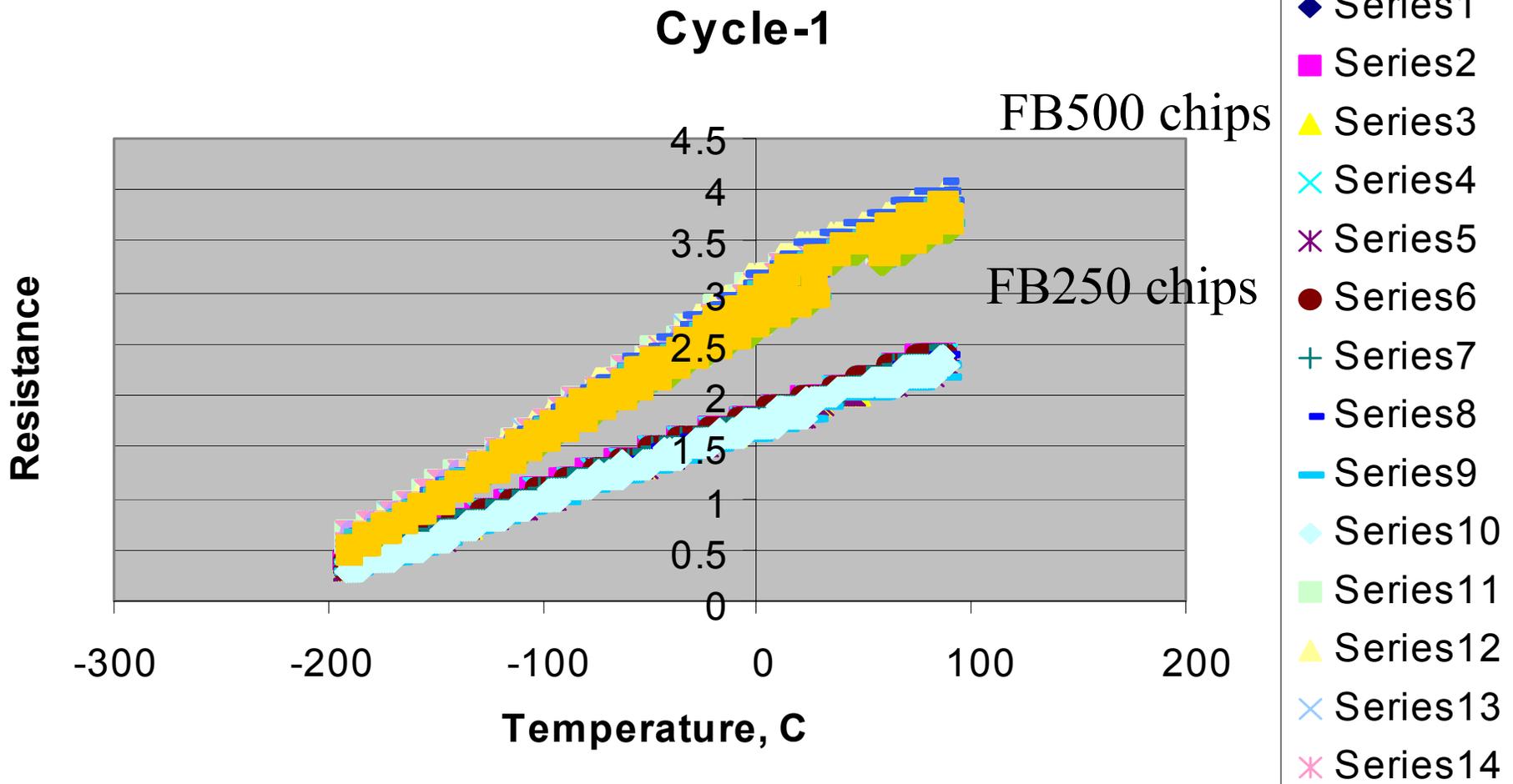
**Experimental extreme temperature test data
obtained during the first cycle.**

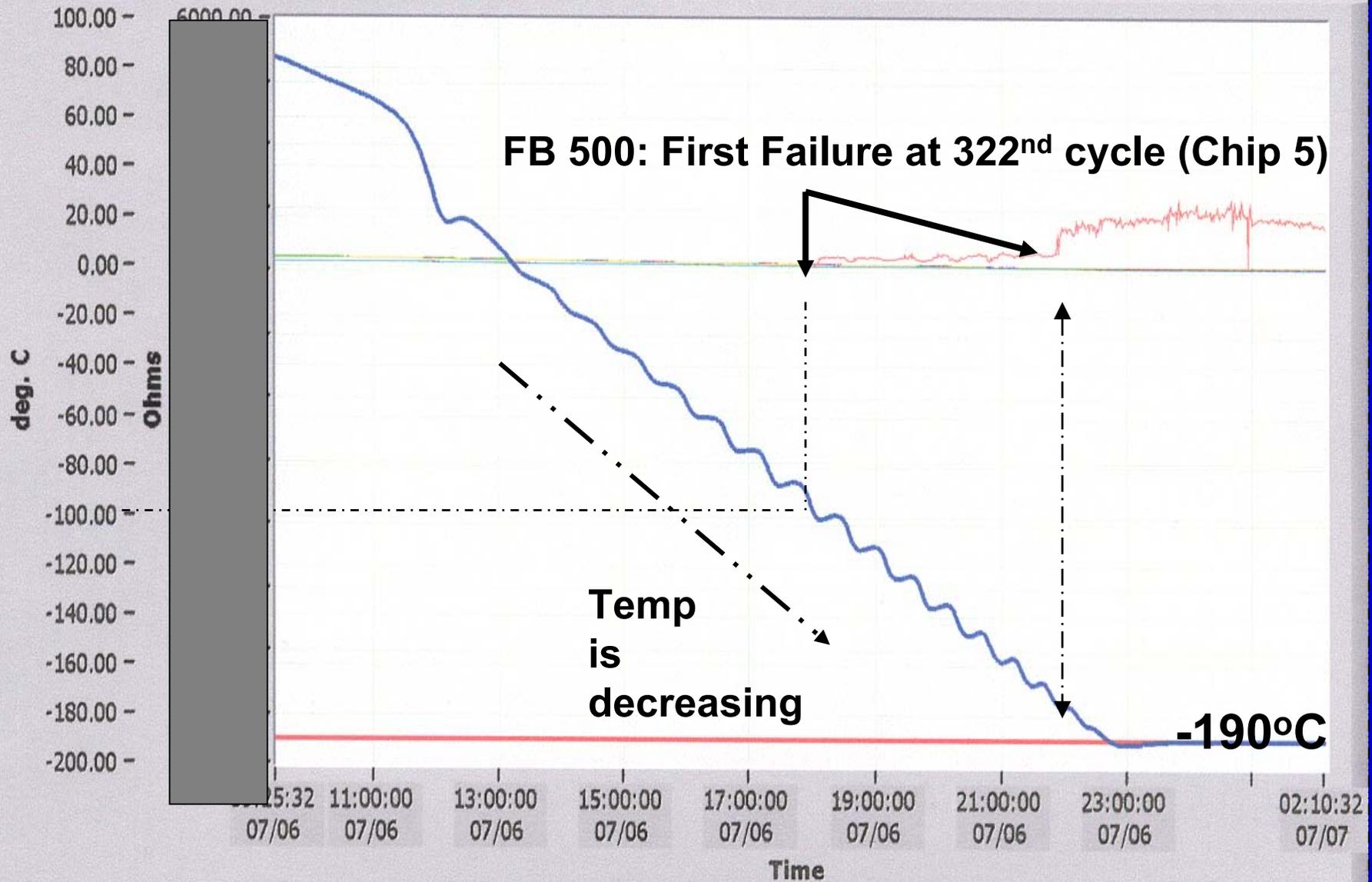


**Resistance of daisy chain associated with FB250 chip
obtained during thermal cycling**



Resistance of daisy chain associated with FB500 chip obtained during thermal cycling





Conclusions

- Flip-chip interconnect test boards were assembled with underfills and subjected to extreme temperature ranges that cover military specifications, extreme Mars and an asteroid environments.
- Very interesting results have been observed when tested over -190°C to 85°C .
- Several failures were observed during the cold cycle and recovers in the hot cycle. More detailed analysis will be performed in the future.
- Diagnostic studies and failure analysis is yet to be done.

Acknowledgements

This work is carried out by the JPL, Caltech/NASA in OSMS Directorate. This work is supported by Ultra Reliability and NEPP programs.