Adaptive Gate Biasing—A New Solution for Body-Driven Current Mirrors

Stephen C. Terry
ECE Dept., University of Tennessee
1508 Middle Way Drive
Knoxville, TN 37996 USA
1-865-974-5473
sterry2@utk.edu

Benjamin J. Blalock
ECE Dept., University of Tennessee
1508 Middle Way Drive
Knoxville, TN 37996 USA
1-865-974-0927
bblalock@ece.utk.edu

Mohommad M. Mojarradi
Jet Propulsion Laboratory
California Institute of Technology
Pasadena, CA 91109 USA
1-818-354-0997
mohammad.m.mojarradi@jpl.nasa.gov

Jesse A. Richmond
ECE Dept., University of Tennessee
1508 Middle Way Drive
Knoxville, TN 37996 USA
1-865-974-5473
jrichmo1@utk.edu

ABSTRACT
A new body-driven current mirror that utilizes an adaptive gate bias to provide accurate operation over a wide range of bias currents is presented. The proposed current mirror can operate with an input and output voltage compliance of V_{DSAT} with no level shifting; thus it is suitable for operation at power supply voltages ≤ 1 V. Measurement results from test circuits implemented in a conventional partially depleted SOI CMOS process show that an nMOS body-driven current mirror that uses the proposed design technique operates reliably over the range 100 nA–1 mA—a four-decade current range which includes the weak, moderate, and strong inversion regions for the devices tested.

Categories and Subject Descriptors
B.7.1 [**Integrated Circuits**]: Types and design styles – advanced technologies

General Terms
Design

Keywords
Ultra-low-voltage analog circuit design, body driving, current mirrors, SOI analog

GLSVLSI'05, April 17–19, 2005, Chicago, Illinois, USA.

1. INTRODUCTION
The scaling of MOSFET dimensions and power supply voltage, in conjunction with an increase in system- and circuit-level performance requirements, are the most important factors driving the development of new technologies and design techniques for analog and mixed-signal integrated circuits. Though scaling has been a fact of life for analog circuit designers for many years, the approaching 1-V and sub-1-V power supplies, combined with applications that have increasingly divergent technology requirements, means that the CMOS analog and mixed-signal IC designs of the future will probably look quite different from those of the past. Foremost among the challenges that analog circuit designers will face in the 1-V regime are reduced power supply voltages, which will limit dynamic range and even circuit functionality, and ultra-thin gate oxides, which give rise to significant gate leakage current and could result in a gate terminal that no longer presents a high input impedance.

Commensurate with the changing landscape of CMOS technology, there has been an explosion of interest in novel analog and mixed-signal design techniques that can deal with these challenges. Foremost among these design techniques are (in alphabetical order) body-driven MOSFETs, common-mode level shifting, floating-gate MOSFETs, and switched op-amp [1]–[4]. Of these, no design technique has emerged as the best in all situations; rather, each is useful in certain situations. For instance, switched-opamp design is useful for low-voltage switched-capacitor circuits, whereas common-mode level shifting with resistors is useful for wide voltage dynamic range, continuous-time signal processing.

While no technique is optimum in all situations, it is the authors' opinion that body driving is one of the most promising and yet least utilized of all the low-voltage design techniques. Body driving, which refers to using the MOSFET body terminal as a signal and/or bias input, is a useful low-voltage design technique because there is no threshold voltage associated with the body terminal; thus dynamic range is increased [5]. In addition, body

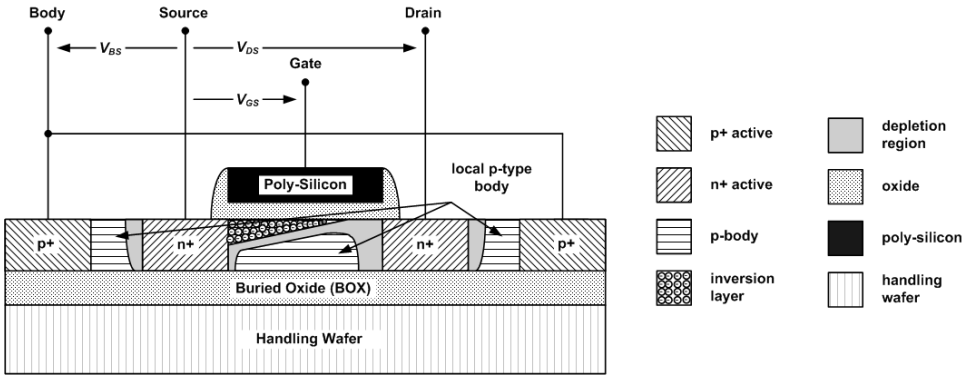

Figure 1. Cross-section of a PD-SOI MOSFET biased in strong-inversion saturation

driving is a promising design technique for highly scaled technologies because the body terminal, as long as it is not excessively forward biased, presents a high input impedance—even while thin gate oxides exhibit significant leakage current.

Taken together, the possible advantages of body driving make it clear that it is a good candidate for analog and mixed-signal circuit design in highly scaled technologies. Indeed, the 2003 International Technology Roadmap for Semiconductors (ITRS) states "Solutions in active threshold regulation, substrate biasing, and novel design architecture will be required to extend the trend for lower supply voltages for mixed-signal applications [6]." However, as of the writing of this paper, body driving has not gained wide favor among analog circuit designers. In general, it is not possible to state precisely why this is the case. However, the authors can point to several likely causes. First and foremost, body driving is an immature design technique when compared to gate driving. Nowhere is this immaturity more apparent than in the fact that a robust body-driven simple current mirror has of yet not been developed. As current mirrors can properly be considered a fundamental element in nearly all analog circuits, the conspicuous lack of a robust body-driven simple current mirror is significant. A secondary though important problem is that it is possible to forward bias the body–source junction while body driving.

In this work a new body-driven current mirror that uses an adaptive gate bias technique to achieve accurate and reliable operation over a wide range of bias currents is presented. In Section 2, some basic concepts related to body driving are discussed, including DC biasing considerations and technology choices for body driving. In Section 3, a standard body-driven current mirror is analyzed and its limitations are clearly stated. In Section 4, the theory of operation of the new current mirror is presented. Measurement results highlighting the operation of the new current mirror are presented in Section 5. Finally, some relevant conclusions of this work are presented in Section 6.

2. INTRODUCTION TO BODY DRIVING

2.1 OPERATION OF A BODY-DRIVEN MOSFET

The physics of body driving can be most easily understood by first considering a MOSFET operating in the strong-inversion region. This bias condition is depicted in Figure 1 for an nMOSFET fabricated in a partially depleted silicon-on-insulator (PD-SOI) CMOS process. To operate in strong inversion, the gate–source voltage must be biased more than 200 mV above the threshold voltage, causing the formation of an inversion layer that connects the MOSFET source and drain. Further associated with this bias condition is a depletion region that is interposed between the inversion layer and the p-type body region [7]. By varying the body voltage we can vary the width of this depletion region, in turn modulating the drain current. Note that a body-driven MOSFET is analogous to a junction field-effect transistor (JFET) and like a JFET it is a depletion-mode or "normally-on" device. Of course, the above discussion considers only the strong-inversion region. When operating in moderate and weak inversion the JFET analogy is less applicable. However, in moderate and weak inversion one can still vary the MOSFET surface potential (and therefore the threshold voltage) as a function of body voltage, in turn modulating the drain current, and as will shown in the next section body driving is just as effective in these operating regions [7].

2.2 DC BIASING FOR A SINGLE BODY-DRIVEN MOSFET

Figure 2 presents the measured drain current versus body–source voltage (I_D–V_{BS}) with V_{GS} swept from 0.4 V to 1.0 V in 0.2-V steps, for an (8/0.5) M = 16 (total W/L = 128/0.5) nMOSFET fabricated on the 3.3-V/0.35-µm standard PD-SOI CMOS process used in this work. The nMOS threshold voltage for this technology is nominally 0.65 V. Several important details about body driving can be learned from this plot. First, as the gate voltage is biased above, below, and nearly equal to the threshold voltage, this plot clearly shows that body driving is viable in the weak, strong, and moderate inversion regions. Second, this plot shows that the body current is insignificant even for relatively large forward bias voltages. Specifically, for a V_{BS} less than 0.5 V the body current is less than 1 nA. From this we can define a "safe operating region" whose demarcation line is the V_{BS} = 0.5 V point. Within this paper the "unsafe operating region" will also be referred to as excessive forward bias. Third, note that within the safe operating region it is possible to control the drain current over a range of more than four decades by manipulating both the gate and body voltages. Note that this clearly points to the ability to operate body-driven current mirrors over a similarly large current dynamic range.

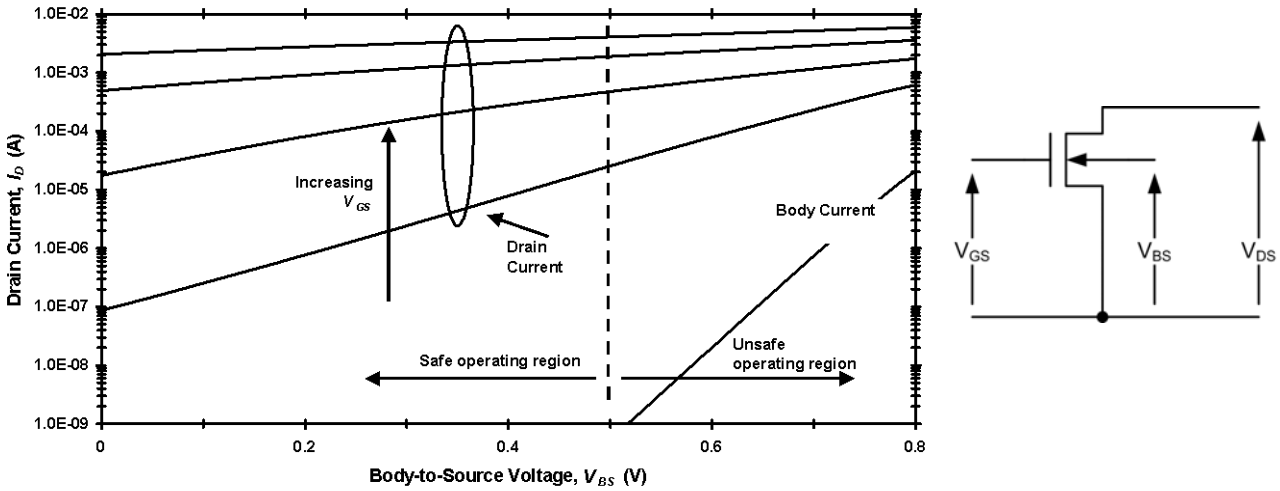

Figure 2. I_D–V_{BS} at several V_{GS} values for an (8/0.5) M=16 body-driven nMOSFET and schematic (V_{DS} = 1 V)

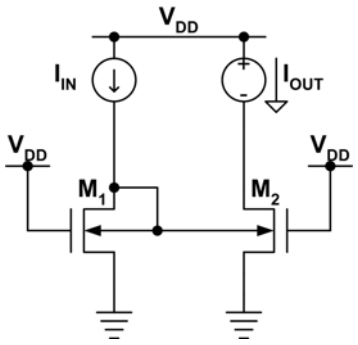

Figure 3. Schematic of a body-driven current mirror with static gate bias [9]

2.3 TECHNOLOGY CONSIDERATIONS

When first proposed as a low-voltage analog circuit technique, body driving was implemented on a standard digital CMOS technology [5]. At the time, it was possible to body drive only nMOS or only pMOS devices within a given technology, as it is only possible to body drive a MOSFET if it has an isolated body connection. For instance, within an n-well bulk CMOS technology, it has historically only been possible to body drive the pMOS devices. This limitation alone has been a motivation for pursuing body-driven circuits on PD-SOI technology, since all devices on PD-SOI have their own local well; hence it is possible to body drive both nMOSFETs and pMOSFETs on PD-SOI [8]. However, a process option that is becoming much more prevalent in modern, highly scaled bulk CMOS technologies is a deep n-well that allows nMOSFETs to reside in their own local p-well, which is junction isolated from the global p-substrate. This means it is possible to body drive both nMOS and pMOS devices in modern bulk CMOS technologies, which removes another important drawback to body driving.

3. BODY-DRIVEN CURRENT MIRROR WITH STATIC GATE BIAS

As it currently stands, the body-driven simple current mirror, which will be referred to in this work as a body-driven current mirror, confronts the designer with great possibilities—and great problems. For low-voltage applications, the body-driven current mirror can be considered optimum becasuse it can operate with an input *and* output voltage of just V_{DSAT}, without the aid of level-shifting circuits. However, this unique advantage is tempered by the fact that it is possible to excessively forward bias the body–source junctions, and that it is difficult to construct a current mirror using depletion-mode transistors. In this section the basic body-driven current mirror will be analyzed in order to gain a better understanding of its limitations

Figure 3 presents a schematic of the original implementation of a body-driven current mirror [9]. In this case nMOS transistors are used, and the gates of the nMOS devices are tied to V_{DD}, typically 1 V, in order to form an inversion channel between the source and drain. The current mirror is implemented by making a drain–body connection for one of the transistors, this becomes the reference device, and connecting the body terminals of the transistors together so that they will have the same body–source voltage. Assuming both transistors are in saturation, this circuit should function just like its gate-driven cousin. Unfortunately, since the body-driven MOSFET is a depletion-mode device, it can be quite difficult to guarantee that the input transistor is in saturation.

To better understand the limitations of the circuit shown in Figure 3, consider how the mirror will operate as the bias current is swept over a wide current dynamic range. For very low currents the reference device (M_1) will be in the Ohmic region because the saturation current, estimated by

$$I_{DSAT} = \frac{\beta}{2}\left(V_{GS} - V_{TH0} - \gamma\sqrt{2\varphi_F - V_{BS}} - \gamma\sqrt{2\varphi_F}\right)^2, \quad (1)$$

will be greater than the input current. However, we can assume that device M_2 will be in saturation, so its output current will be equal to the saturation current plus a small error due to channel

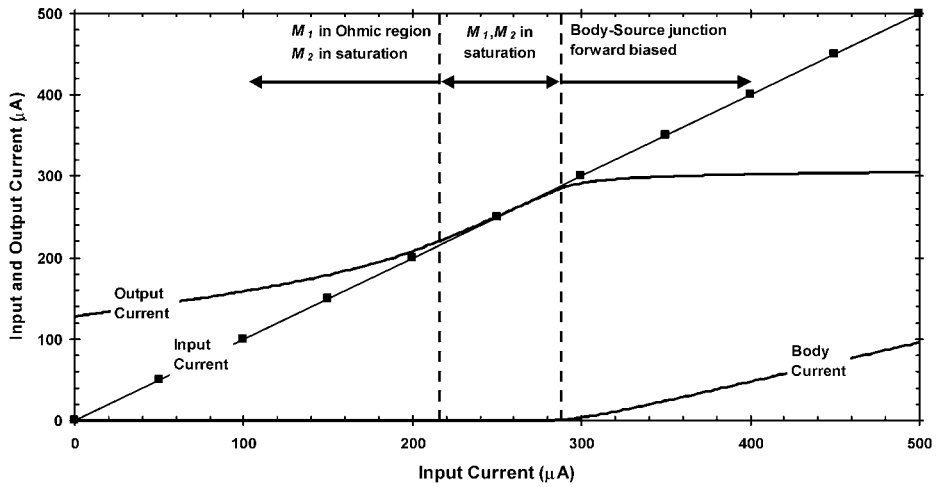

Figure 4. Simulated I_{OUT}–I_{IN} transfer characteristic for the body-driven current mirror shown in Figure 3.

length modulation. Thus for small input currents M_1 will be in the Ohmic region and M_2 will be in saturation, the result being that the output current will only weakly track the input current. As the input current is increased the drain voltage of M_1 will increase in direct proportion (since M_1 is in the Ohmic region); however, the saturation current will increase less than proportionally because V_{BS} is inside the radical and multiplied by γ. Thus at some point the input current will become larger than the saturation current. When this happens both M_1 and M_2 will be in saturation, and the body-driven current mirror will function just like a gate-driven current mirror. This operating mode will be referred to as the "linear region" because this is where the output current tracks the input. Unfortunately as the input current is increased still further the body–source junctions will become excessively forward biased, in which case the input current flows through the body–source junction and the output current saturates.

Figure 4 presents a plot of the simulated input–output current transfer characteristic for the nMOS current mirror presented in Figure 3. For this simulation V_{DD} = 1 V, the current mirror output voltage is 0.5 V, and the bias current is swept from 0 to 500 μA. Each nMOS device is sized 10/2 M = 5 (total W/L = 50/2). In this plot one can clearly see the three operating regions of the body-driven current mirror presented in Figure 3, and the limitations of the standard body-driven current mirror. Namely, the operating region where both MOSFETs are in saturation, and where the body–source junctions are not excessively forward biased, is extremely small. Furthermore the boundaries of this linear region will vary chip-to-chip due to threshold and mobility variations. The net result is that the standard body-driven current mirror is not a realistic choice for use in a practical circuit design because it has a small linear region, and with process variations it is difficult to bias the reference transistor of the current mirror in this operating region.

4. BODY-DRIVEN CURRENT MIRROR WITH ADAPTIVE GATE BIAS

The fundamental problem with the body-driven current mirror is that the saturation current varies from chip-to-chip, which means that it is difficult to bias the current mirror in the linear region. To solve this problem an adaptive gate bias circuit has been developed that allows the user to explicitly define the saturation current—independent of process variations. Furthermore when using the adaptive gate bias circuit the width of the linear region, for a given saturation current, can be increased simply by increasing the aspect ratio of the devices. Figure 5 presents a schematic diagram of the improved body-driven current mirror presented in this work. Note that the relative sizing of each MOSFET is indicated on the schematic. Also note that the current source on the left represents the input terminal for the user defined saturation current, and the current source on the right represents the current mirror input.

The basic idea of this circuit is to bias the gates of the body-driven devices (M_1, M_2) such that the saturation current is an accurately defined quantity. Devices M_{B2}, M_{B3}, M_{B5}, and M_{B6} form the core of the adaptive gate-bias circuit, and they are used to generate a reference voltage equal to the V_{DSAT} of the body-driven transistors [10]. To understand how the V_{DSAT} generator operates, one must refer to the EKV MOSFET model, which defines a forward MOS current (I_F) controlled by the source and a reverse MOS current (I_R) controlled by the drain [11]. If the forward current is much larger than the reverse current, the transistor is operating in saturation. Using the EKV model to analyze the V_{DSAT} generator [10], it can be shown that the ratio of the forward to reverse drain current in device M_{B6} is given by

$$\frac{I_{F,MB6}}{I_{R,MB6}} = 1 + m(1+n). \tag{2}$$

Since the ratio of the forward and reverse currents can be explicitly set to a value that is much greater than one (typical values are m=n=4)—independent of the bias level—the drain–source voltage of M_{B6} is guaranteed to be equal to or slightly greater than V_{DSAT}. The V_{DSAT} reference voltage is used to forward bias the body of device M_{B7}, which is otherwise connected as a standard MOS diode (V_{GS} = V_{DS}) and biased at the desired saturation current. Finally, the gate voltage of M_{B7} is used as the adaptive gate bias for the body-driven current mirror. Now, assuming that the current mirror input is equal to the user defined saturation current, and noting that the transistors in the body-

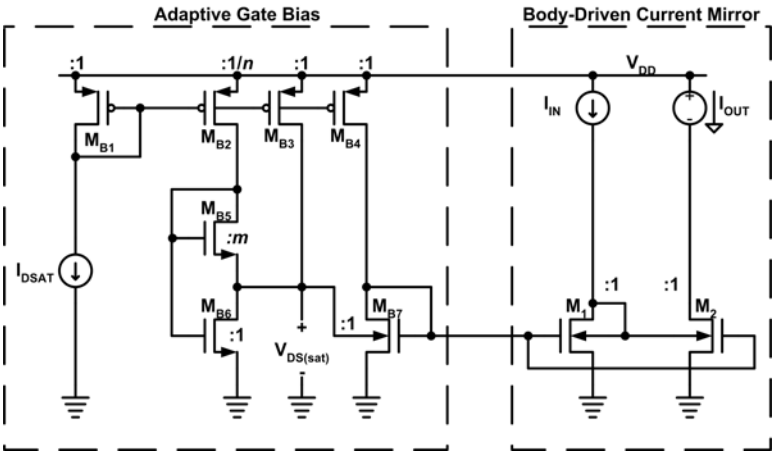

Figure 5. Adaptively biased body-driven current mirror

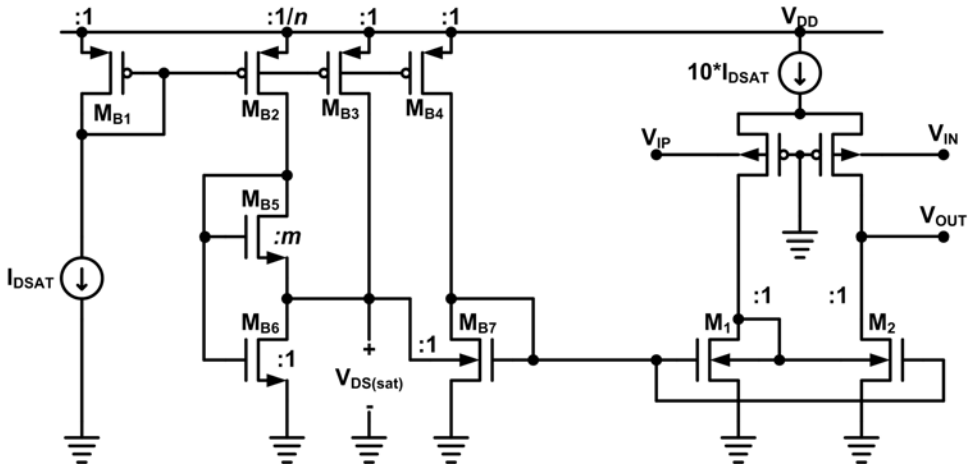

Figure 6. Schematic of a body-driven OTA utilizing a body-driven differential pair and body-driven current mirror

driven current mirror are matched to M_{B7} and biased at the same V_{GS}, they must also have the same body voltage as M_{B7}. Given that the body voltage of M_{B7} is greater than or equal to V_{DSAT}, M_1 is guaranteed to be operating in saturation. Thus, when the mirror input is equal to the user defined saturation current, the reference device (M_1) will be biased at the edge of saturation. Of course, this is the definition of saturation current; that is, the drain current produced when a transistor is biased at the edge of saturation. Therefore, by adaptively biasing the gate voltage, this circuit allows the user to explicitly define the saturation current of a body-driven transistor.

Now that we can define the saturation current, the body-driven current mirror becomes a robust, useful circuit element. For instance, consider using the body-driven current mirror as an active load for a differential pair, which represents a typical application and is shown in Figure 6. One could define the saturation current to be a fraction of the tail current, for instance one could set the saturation current as 5 μA and the tail current as 50 μA. When the differential pair is balanced, each device in the mirror conducts 25 μA; which being larger than 5 μA guarantees that the M_1 and M_2 are in saturation. Furthermore by sizing the mirror to have a low V_{DSAT} (< 150 mV) at 5 μA, the body–source junctions will not be excessively forward biased when operating even at 50 μA (the full tail current). Using this bias technique the mirror will be in the linear region over the entire current range 5 μA–50 μA. Below 5 μA the current mirror will become somewhat non-linear (large-signal); however, this condition will only occur when the amplifier is slewing, which is already a non-linear operating region. Additionally one can be certain of not excessively forward bias the body–source junctions by choosing a tail current/saturation current ratio in the range of 10 to 50, and by sizing the MOSFETs (M_1, M_2) so that V_{DSAT} is low. Thus the adaptive gate bias enables process-insensitive current mirrors using the depletion-mode body-driven transistor, and protects against turning on the body–source junctions.

5. MEASUREMENT RESULTS

Correct operation of this circuit was verified through measurement. Specifically, an nMOS current mirror that uses the adaptive bias technique presented in Figure 5 was fabricated and tested. The mirror devices are sized 8/0.5 M = 4 (total W/L = 32/0.5) and the *m* and *n* factors are four and three, respectively.

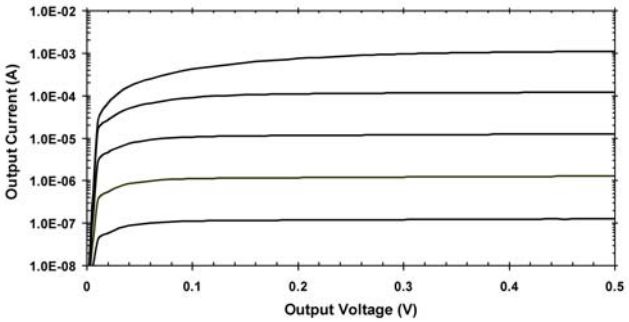

Figure 7. Measured I_{OUT}–V_{OUT} for the body-driven current mirror. In this measurement I_{DSAT} equals I_{IN} and is stepped by decades from 100 nA to 1 mA.

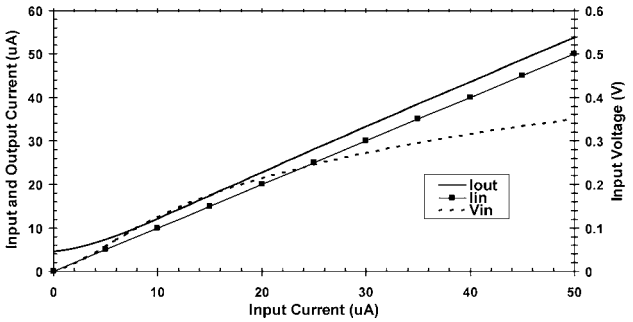

Figure 8. Measured I_{OUT}–I_{IN} transfer characteristic for the adaptively biased body-driven current mirror. I_{DSAT} is equal to 5 μA.

Figure 7 presents the I_{OUT}–V_{OUT} characteristic for the current mirror as the saturation current is stepped in decades from 100 nA–1 mA. In this test the input current is equal to the saturation current, thus this plot shows the wide range of bias current over which the adaptively biased body-driven current mirror is able to operate. Figure 8 presents the I_{OUT}–I_{IN} transfer characteristics as the input current is swept from 0 to 50 μA, with a saturation current of 5 μA and an output voltage of 0.5 V. In this plot one can see that the output current tracks the input over nearly the entire range, with non-linearity occurring for input currents below 5 μA. Additionally, on the right axis one can see that the input voltage is never larger than 350 mV. In both Figure 7 and Figure 8 one can see that there is a small error in the output current. This error is due to channel length modulation, and is the same for body-driven and gate-driven simple current mirrors.

6. CONCLUSION

A body-driven current mirror capable of accurate operation over a wide range of bias currents has been presented. Special attention has been paid to developing a bias circuit that guarantees good linearity without excessively forward biasing the body–source junctions. In addition, the proposed circuit enables robust operational amplifiers that can operate at power supply voltages ≤ 1V. The combination of good linearity and sub 1-V operation should make the improved body-driven current mirror a useful circuit element in the next generation of low-voltage analog integrated circuits. In a broader context, it is hoped that the availability of a robust body-driven current mirror will pave the way for increased use of body-driven circuits for analog signal processing.

7. ACKNOWLEDGMENT

This work was funded in part by the Honeywell Corporation and in part by the Jet Propulsion Laboratory, California Institute of Technology under a contract with the National Aeronautics and Space Administration.

8. REFERENCES

[1] S. Yan and E. Sanchez-Sinencio, "Low voltage analog circuit design techniques: a tutorial," *IEICE Trans. On Electronics*, vol. E83-A, no. 2, pp. 179–196, February 2000.

[2] S. S. Rajput and S. S. Jamuar, "Low voltage analog circuit design techniques," *IEEE Circuits and Systems Magazine*, vol. 2, no. 1, pp. 24–42, 2002.

[3] J. W. Fattaruso, "Low-voltage analog CMOS circuit techniques," *Proceedings of the VLSI Symposium*, pp. 286–289, June 1999.

[4] J. F. Duque-Carillo, J. L. Ausin, G. Torelli, J. M. Valverde, and M. A. Deminguez, "1-V rail-to-rail operational amplifiers in standard CMOS technology," *IEEE J. Solid-State Circuits*, vol. 35, no. 1, pp. 33–44, January 2000.

[5] B.J. Blalock, P.E. Allen and G.A. Rincon-Mora, "Designing 1-V op-amps using standard digital CMOS technology," *IEEE Transactions on Circuits and Systems II*, vol. 45, no. 7, pp. 769–780, July 1998.

[6] *International Technology Roadmap for Semiconductors*: Process Integration, Devices, and Structures Chapter, p. 25, 2001 edition

[7] Y. Tsividis, *Operation and Modeling of the MOS Transistor*, McGraw-Hill, 1999.

[8] S. C. Terry, B. J. Blalock, L. K. Yong, B. M. Dufrene, and M. M. Mojorradi, "Complementary body driving—a low-voltage analog circuit technique for SOI," *Proceedings of the 2002 IEEE International SOI Conference*, pp. 80–82, Williamsburg, VA, October 2002.

[9] B.J. Blalock and P.E. Allen, "A Low-Voltage, Bulk-Driven MOSFET Current Mirror for CMOS Technology," in *Proc. 1995 IEEE Int. Symp. On Circuits and Systems*, pp. 1972–1975, 1995.

[10] B.A. Minch, "A Low-Voltage MOS Cascode Bias Circuit for All Current Levels," in *Proc. 2002 IEEE Int. Symp. On Circuits and Systems*, Vol. 3, pp. 619–622, 2002.

[11] C.C. Enz, F. Krummenacher, and E.A. Vittoz, "An Analytical MOS Transistor Model Valid in All Regions of Operation and Dedicated to Low-Voltage and Low-Current Applications," *Analog Integrated Circuits and Signal Processing*, vol. 8, no. 1, pp. 82–114, 1995.