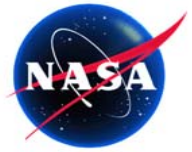

X2000 Power System Control Architecture

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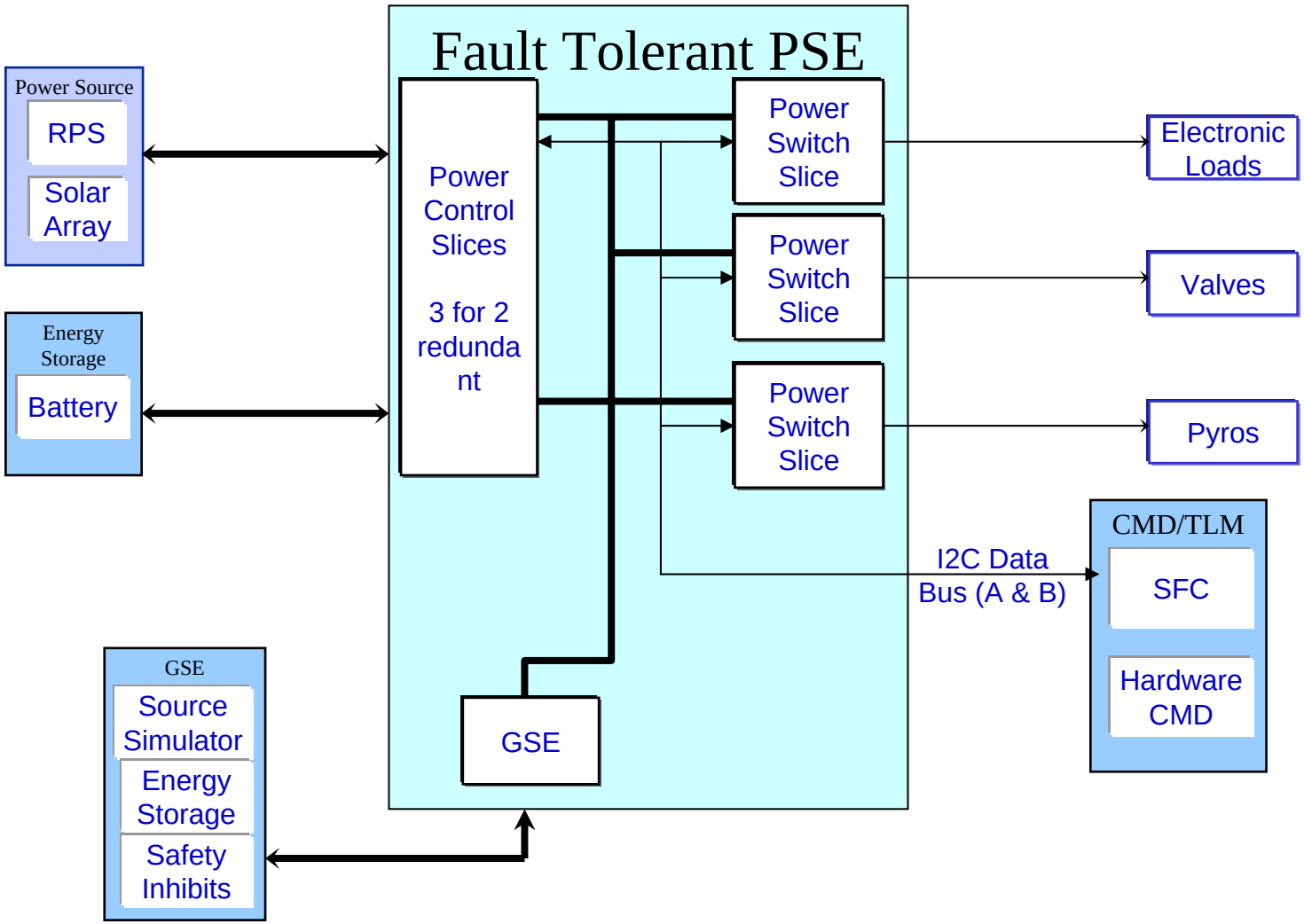
Agenda

- Introduction
- X2000 Power System Electronics (PSE) Functional Block Diagram
- X2000 PSE Implementation Approach
- Distributed Control Architecture
- CIA Functional Description
- AIA Functional Description
- Other Applications
- Summary
- Acknowledgements

Introduction

- X2000 Power System Control Architecture:
  - Provides command and telemetry interface for all power system components
  - Multi-master and multi-drop capability
  - Minimum of single fault tolerant
  - Provides isolation for the fault containment regions
  - A single solution for both the switching and regulation of a spacecraft power bus.
- Implementation
  - Space-rated Inter-Integrated Circuit (I2C) Standard data bus
  - Utilizes 1 Mrad hard Honeywell mixed-signal ASICs

X2000 Power System Functional Block Diagram



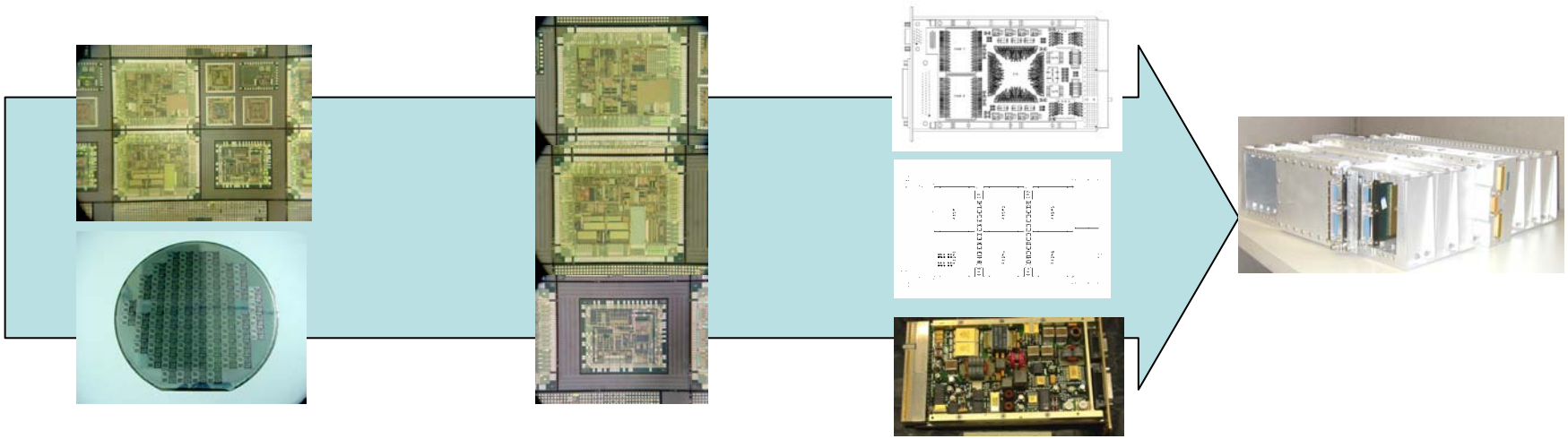
X2000 Implementation Approach

Intellectual Property Level
* ASIC Library
* Verilog Code
* Firmware Code
* Power Control Algorithm
* Power System Architecture

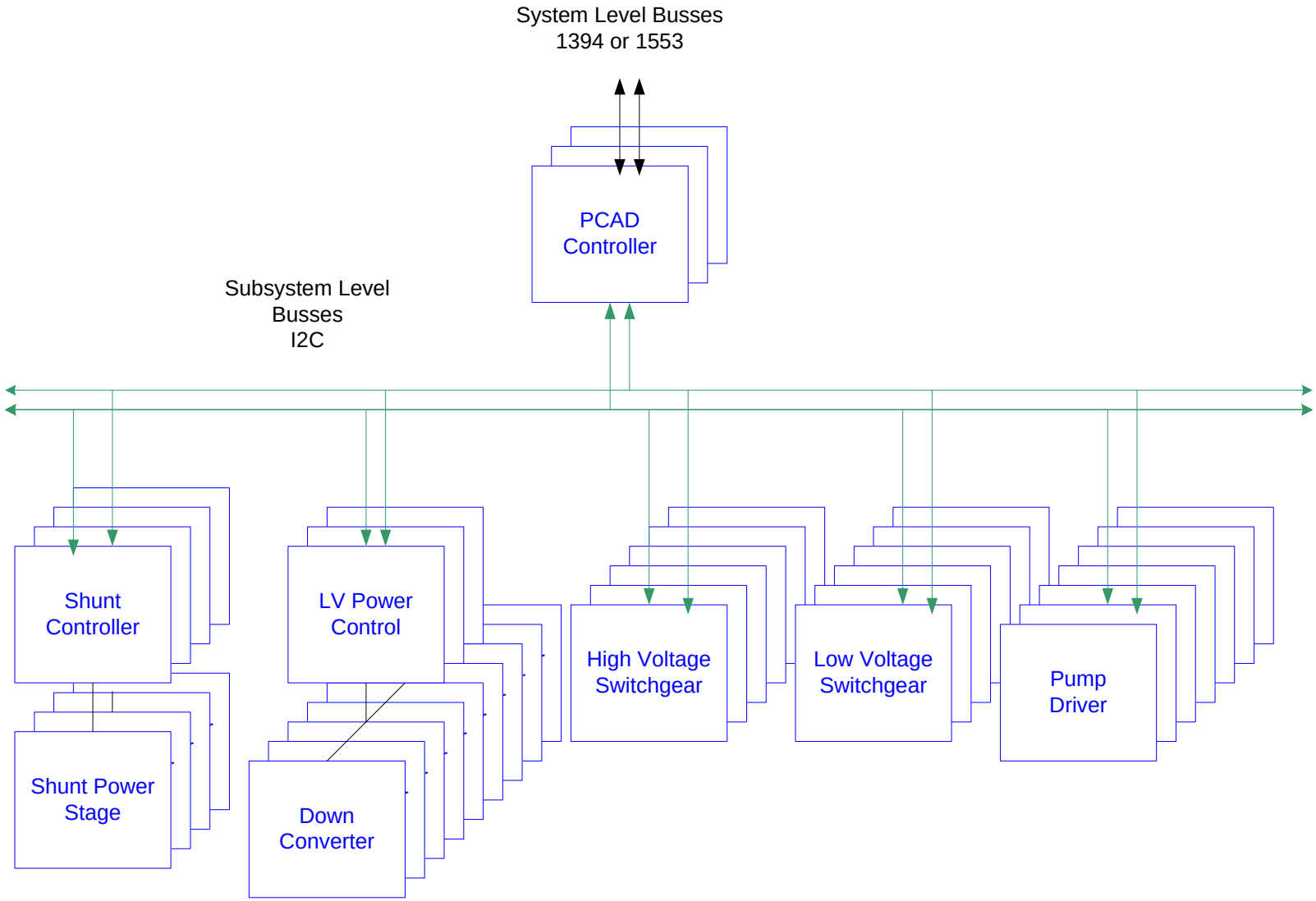
ASIC and Module Level Components
* SCAH
* SCAL
* PWMA
* CIA
* AIA
* PASM

Slice Level Components
* Power Control Slice (PCS)
* Power Switch Slice (PSS)
* Dual Converter Slice (DCS)

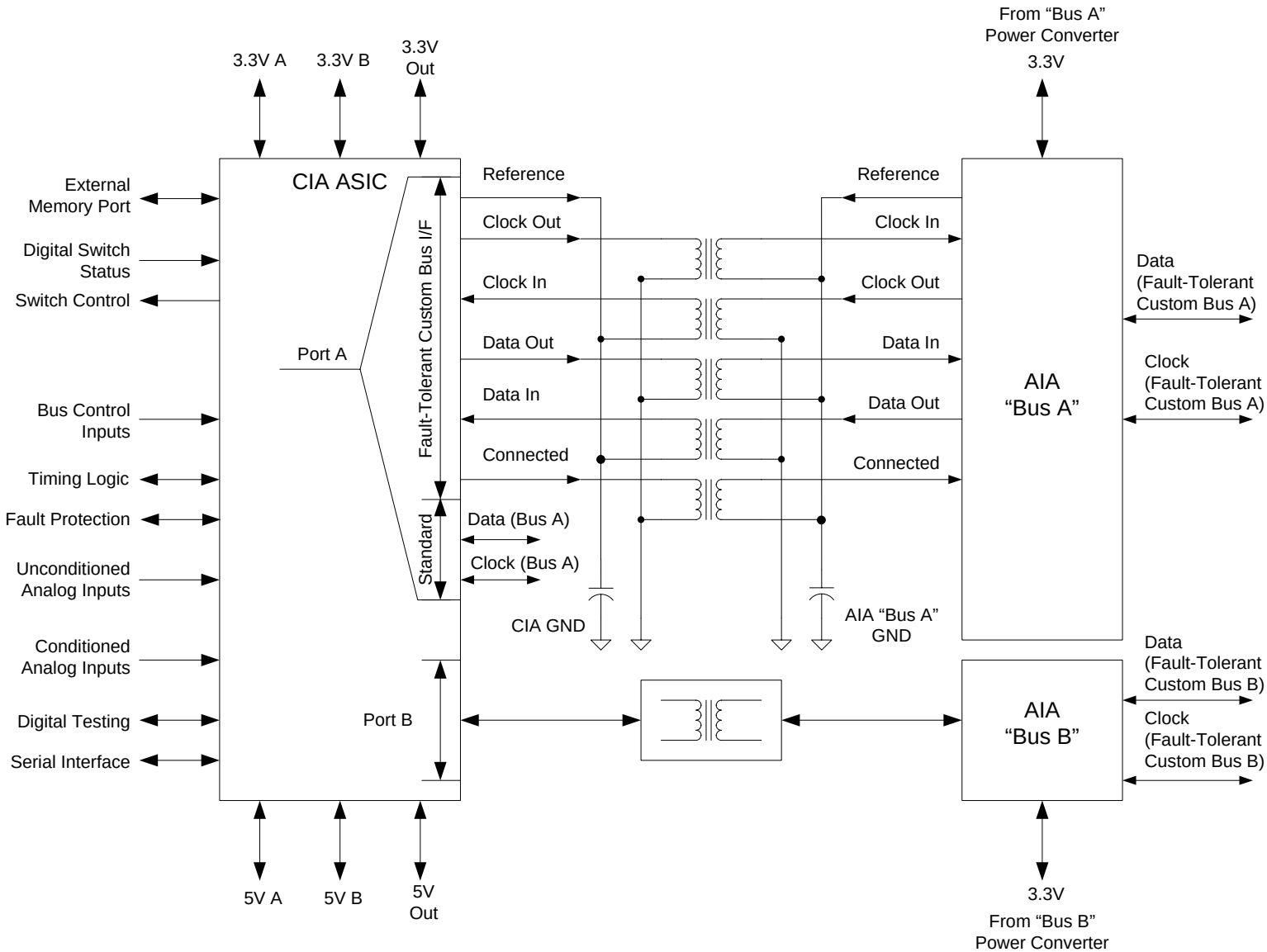
Subsystem Level
* Power System Electronics (PSE)
* Power Control
* Power Distribution
* Valve Drive Electronics
* Pyro Drive Electronics
* Power Conversion



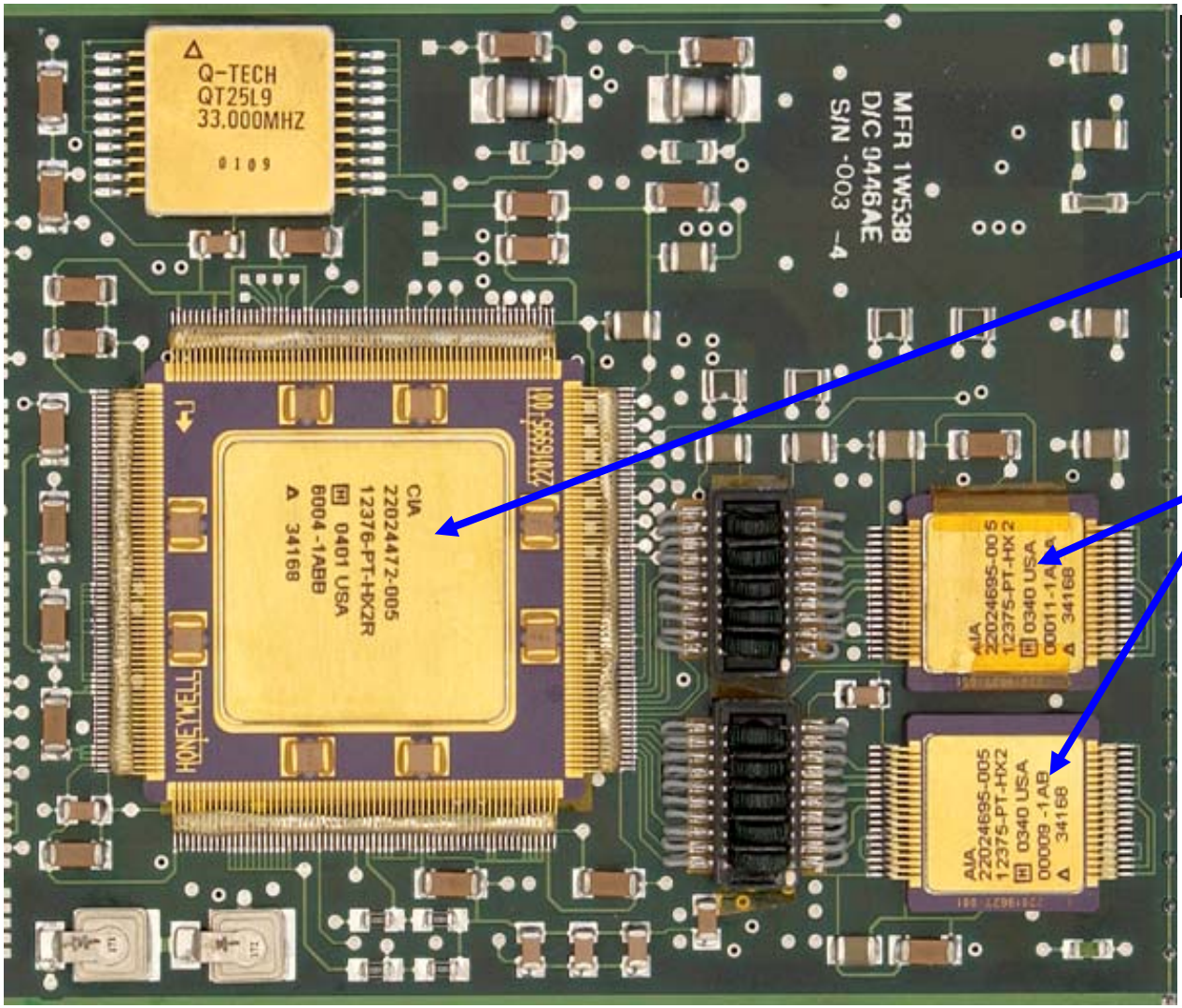
Distributed Control Architecture



Command Interface Chipset



Command Interface Chipset

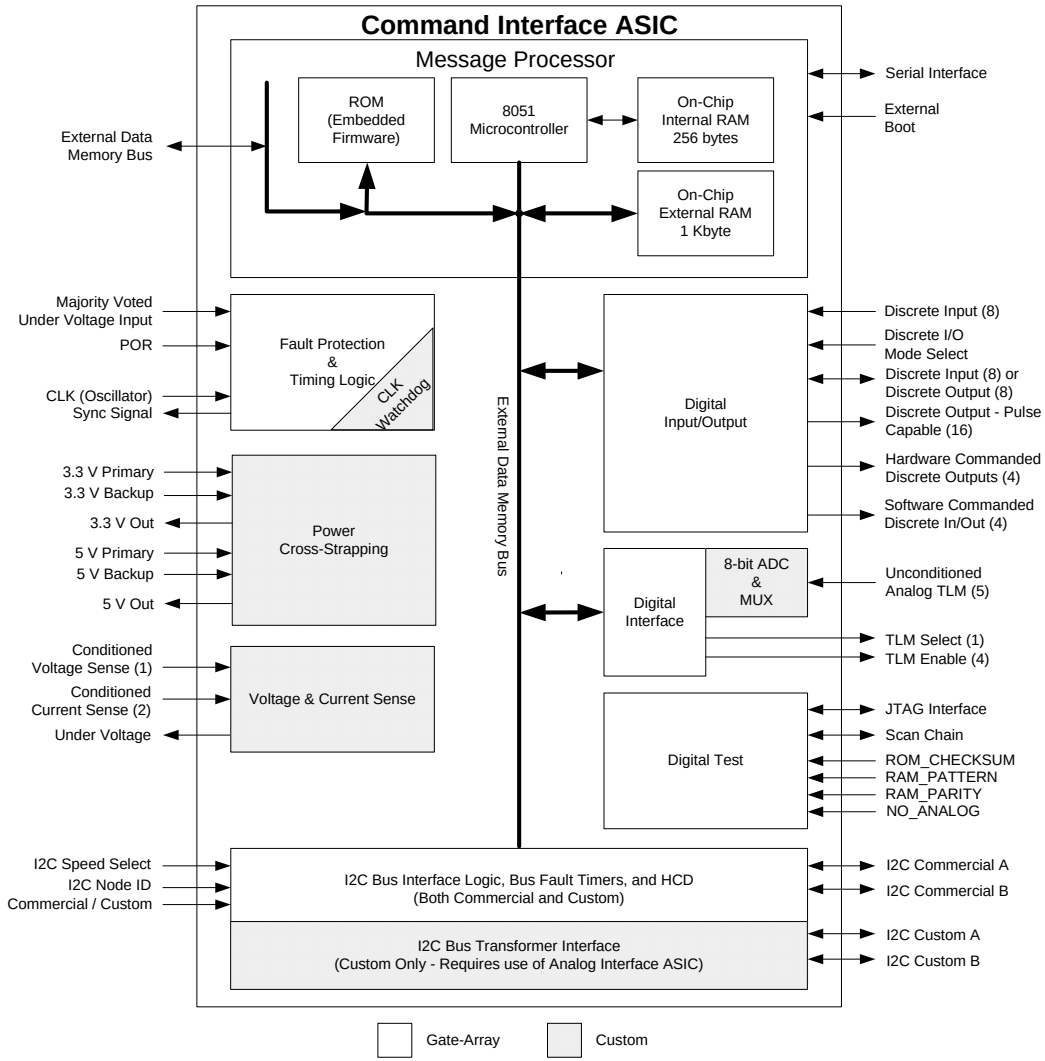


Command Interface ASIC (CIA)
Honeywell HX2000r
1 Mrad, LET > 75 MeV
3.3V, 5V: 125 – 600 mW

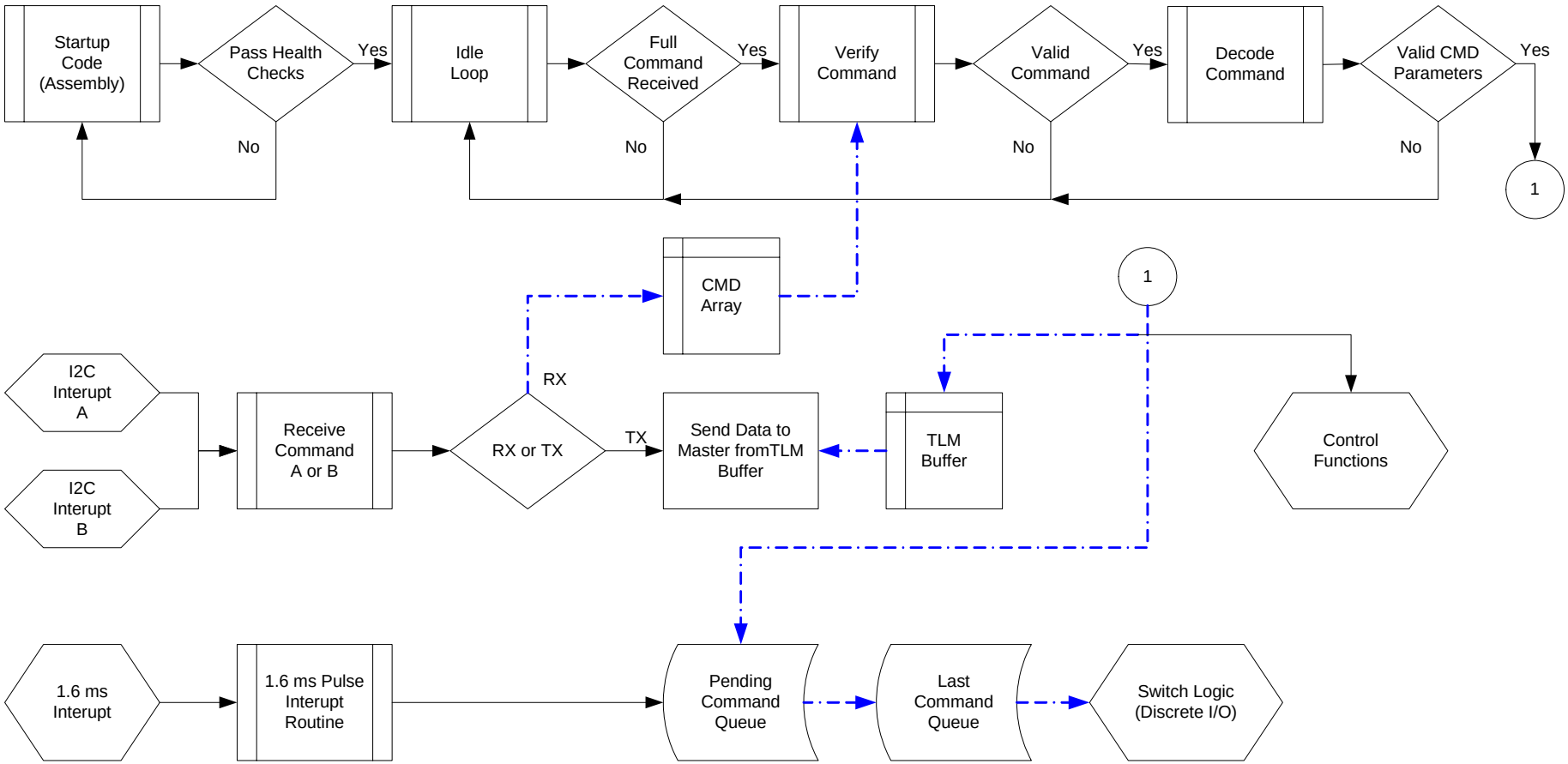
Analog Interface ASIC (AIA)
Honeywell HX2000
1 Mrad, LET > 75 MeV
3.3V, <100 mW

CIA HW Functional Description

- Message Processor
  - 8051 Microcontroller Core
  - 256 Bytes of Internal RAM
  - 1K Byte of External
  - 8K x 8 On-Chip Boot ROM
- Digital Input/Output
  - Functions as Switch Control and Digital Status
- On-Chip ADC
- Space-rated I2C bus I/F
  - Watch Dog Timers
- Crossed –strapped Power



CIA FW Functional Description

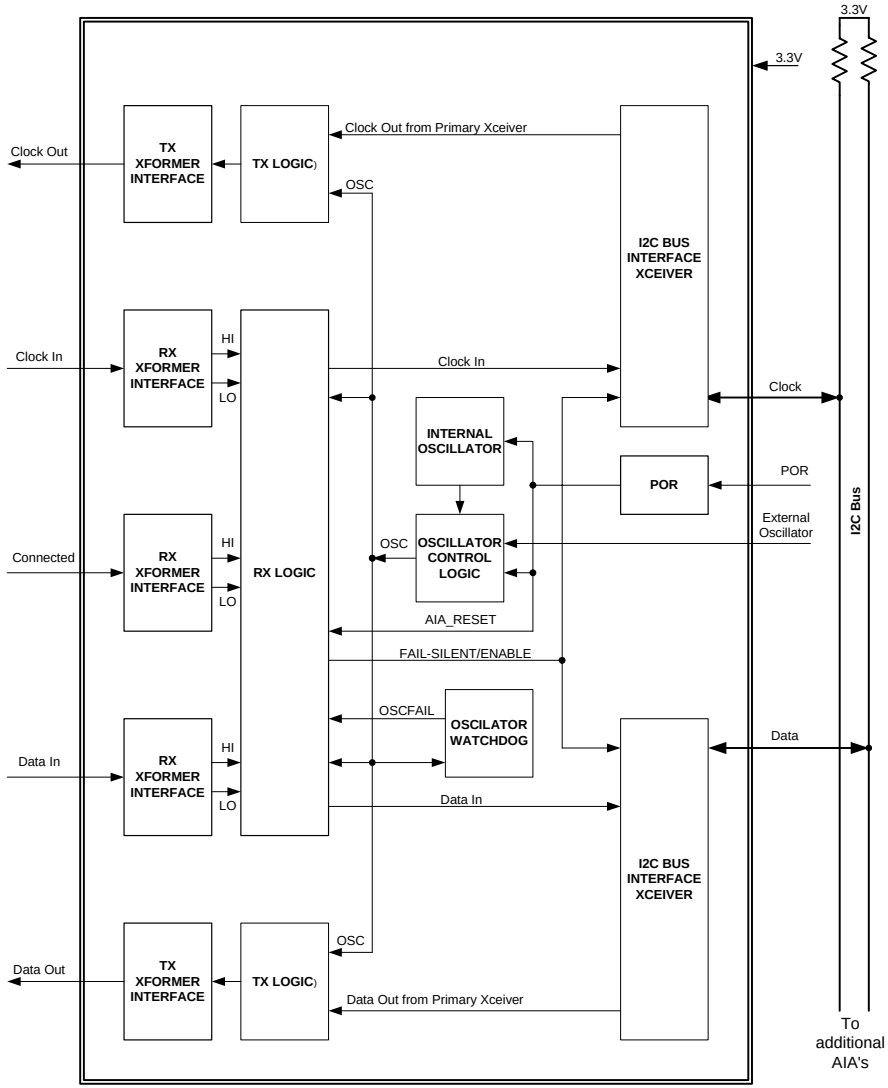


Legend:

Control Flow
Data Flow

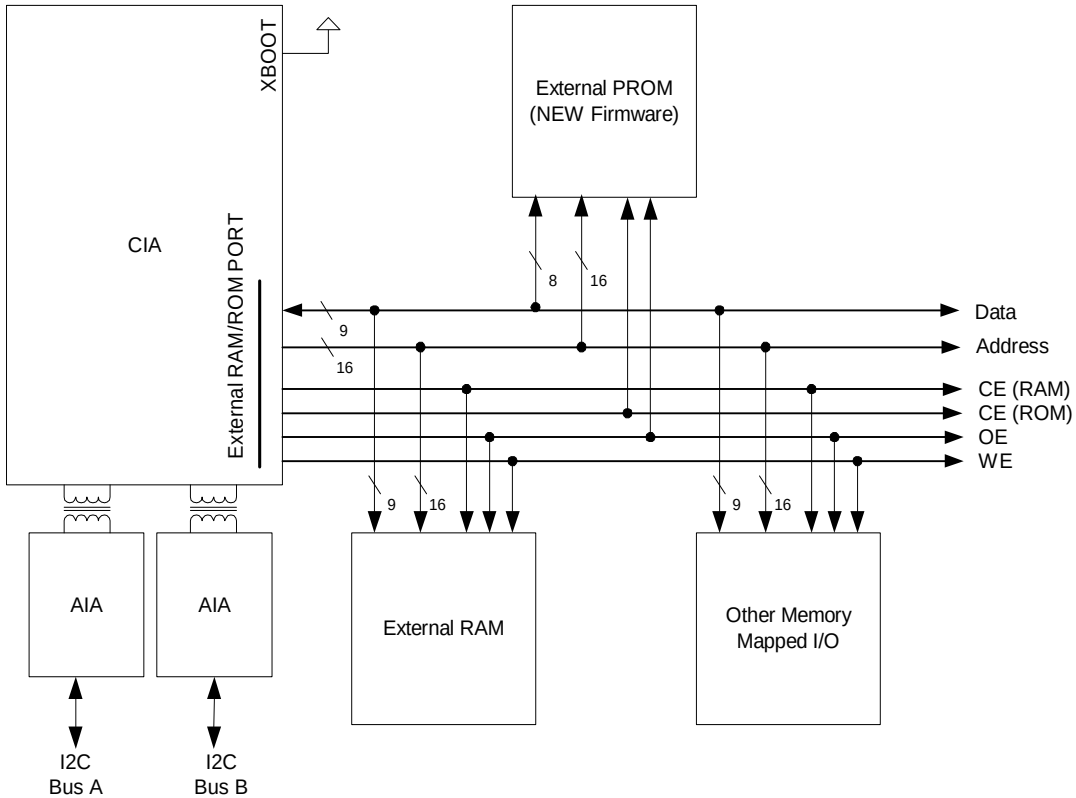
AIA Functional Description

- Power
- I2C Bus Interface
  - Slew rate controlled
- I2C Transformer Interface
- Power-On-Reset Circuitry
- Fail-Silent Timer
- Internal Oscillator and Support Circuitry



Other Applications

- **Power Control**
- **Motor Control**
- **Instrument Interface**
- **Remote Engineering Unit**



Power Control Algorithm

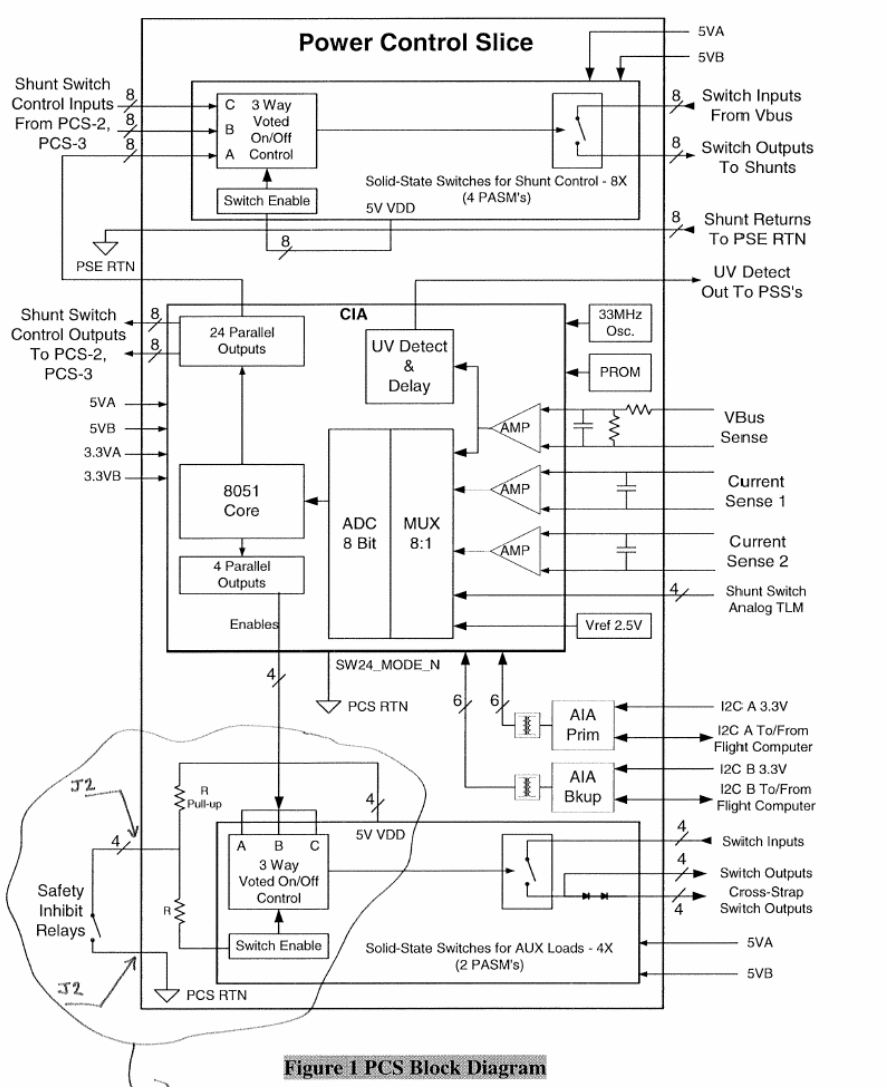
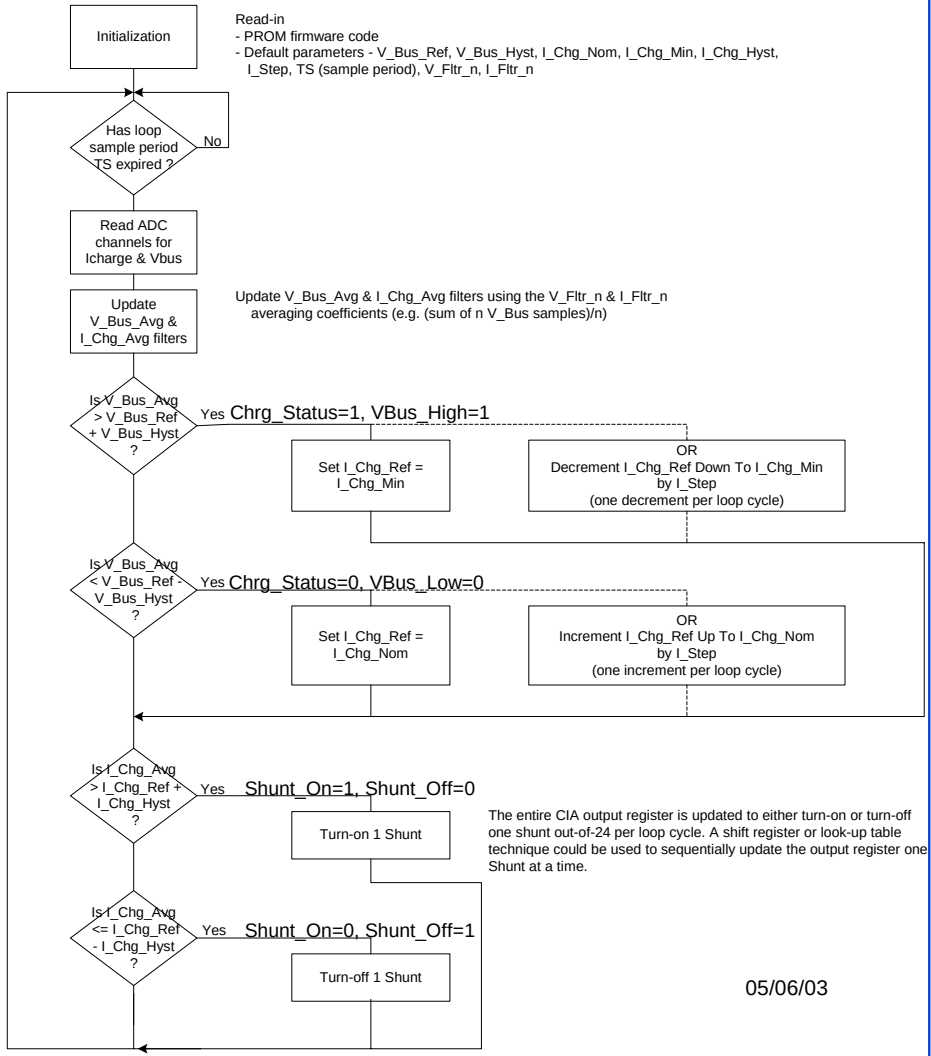


Figure 1 PCS Block Diagram



Summary

- **Designed to provide a flexible solution to power switching and power bus regulation.**
- **Open-Systems Architecture allows for other powerful applications**
  - **Embedded Microcontroller (8051 – 2 clock cycles/instruction)**
  - **Fault Protection Logic and Timers**
  - **Embedded 8-bit ADC**
  - **Redundant and Fault Tolerant Custom and Standard I2C bus connection**
  - **Additional RAM can be added.**
  - **Other Memory Mapped I/O can be added**

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The research described in this paper was carried out at the Jet Propulsion Laboratory, California Institute of Technology, under a contract with the National Aeronautics and Space Administration.

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