

Large CMOS Imager Using Hadamard Transform Based Multiplexing

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We have developed a concept design of a large (16 Mpixel or more) imaging array whose elements are grouped in small subarrays with N pixels in each, which, in turn, are code-division multiplexed using the Hadamard Transform based encoding. The Hadamard code improves the signal-to-noise ratio to the reference of the read-out amplifier by a factor of $N^{0.5}$. This way of grouping pixels reduces the number of hybridization bumps by N . A single chip layout has been designed and the architecture of the imager has been developed to accommodate the Hadamard Transform base multiplexing into existing CMOS technology. This multiplexing technique improves a number of performance figures including power dissipation and allows for a trade-off between the speed and the sensitivity. The imager architecture and modeling results will be presented at the meeting.