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SEU Evaluation of FeRAM Memories for Space Applications.

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Abstract

SEU cross-sections were obtained for two different FeRAM memories: The 64 kbit and 256 kbit Ramtron FeRAM and the Hynix 64 kbit device. The devices were seen to have latch-up characteristics typical of commercial CMOS. Also, errors in the memory were also seen from heavy ion irradiation.

I. Introduction

Due to the ever increasing need for viable space avionics systems, more and more Commercial-Off-the-Shelf (COTS) parts are being investigated for application in radiation environments. FeRAMs are candidates especially since the current non-voltile workhorse Flash memory has many space flight liabilities. FeRAM technology presents an attractive alternative for use in remote systems [1].

II. FeRAM Devices

CMOS-based FeRAM been studied somewhat for both TID and SEE effects [2,3]. Studies have concentrated on areas as far ranging as models to real-time flight studies [4,5]. Since FeRAM technology has become attractive for avionics systems, the SEE response is of great importance [6]. The primary consideration of many of the studies is the characterization of SEL cross-section curves and the thresholds for the respective phenomenon [7]. Latch-ups present the added concern of catastrophic damage, which is very important.

In this study similar investigations are conducted [8] with SEU cross sections also are calculated. The three different FeRAM devices were used in this study: two Ramtron series and a Hynix FeRAM. Table 1 shows basic features of the devices. Three of each device type were tested for response under heavy ions. The devices were encased in lidded DIP packages, which were easily delidded for exposure to heavy ions.

Table 1. Properties of the FeRAM devices under test.

Device	Man.	Size	Code	Tech.
FM1806	Ramtron	64kx8	9951	PZT
FM1808	Ramtron	128kx8	na	PZT
Hy8064	Hynix	8kx8	NA	SBT

III. Test Setup And Procedure

The test setup consisted of two PCs, a power supply, and a specially designed test board. One PC controlled a HP6629A power supply. This allowed precision voltage control and latch-up detection and protection since the PC had millisecond control over the operation of the power supply. Latch-ups were recorded in a separate file during the test.

A dedicated PC controlled the test circuit board designed specifically for this FeRAM test to read and write to the DUTs. Custom daughter boards allow each FeRAM type to be tested by the same test board. The address of each DUT could be accessed randomly. This setup allows complete freedom to interact with the DUT. The address of a failure and the value at that address were recorded in a file for each run. This allowed for any structure in the SEEs or predilection for certain pattern failure or type of SEU to be observed. A depiction of the setup used is shown in Figure 1. Testing was done at the Brookhaven National Laboratory.

Table 2. Ions used in testing.

Species	Site	LET	Angles used
Chlorine	BNL	11.4	0, 45, 55, 60
Nickel	BNL	26.6	0, 45, 55, 60
Iodine	BNL	59.9	0, 45, 55, 60
Carbon	BNL	1.4	0, 45, 55, 60

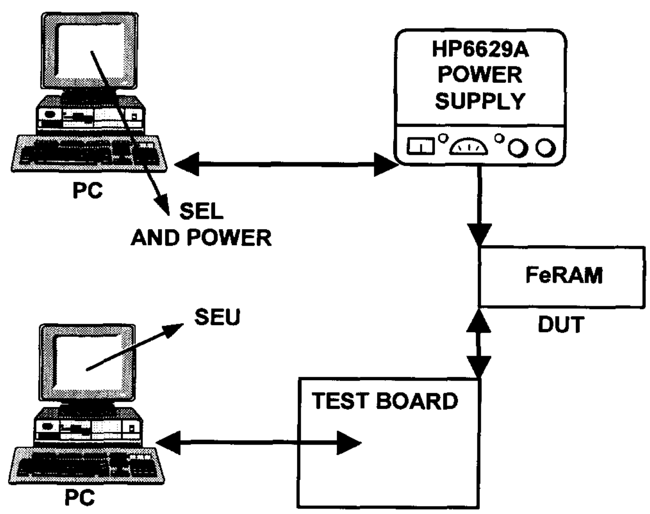

Figure 1. A block diagram of the test system.

For this test, most of the radiation runs were done when the DUT was in stand by mode with a known pattern written in the DUT. The PC cycled through the address space of the DUT, stored address, which exhibited an error, along with the error value, and rewrote the correct pattern to the address. The most common pattern written to the device was a checkerboard pattern, i.e. an 8-bit address would have 170 in address 0, 85 in address 1, 170 in address 2, and so on. This pattern was reversed from time to time to prevent any CMOS imprinting. Some tests were done while actively reading or writing data to test for susceptibility to SEE during such processes.

The Vdd voltage was always set to 5 volts and the operating temperature was approximately 25 °C throughout the study.

IV. Heavy Ion Results

A. SEU Results

All of the devices had similar results. They were programmed and read using the same handshaking protocol and only 64kx8 of the memory was tested. Figures 2 and 3 show the cumulative response for the Ramtron and Hynix devices, respectively. The devices were seen to have these effects occasionally, but when it occurred the result was tens or hundreds of errors. So the actual cross section is expected to be much less, but the ramifications to EDAC may be greater. For the purposes of this summary, only the runs that resulted in an upset are shown and the cross sections plotted are results of that error count-to-fluence ratio. The full paper will explore the cross section of these events more exactly. The errors were read errors after the device was irradiated in stand-by mode. Some upsets were seen in runs that experienced no latch up. So the mechanism is not entirely related to large voltage transients that occur during latch up. Possible mechanisms are transients in the control circuits emulate re-write commands. The full paper will examine this novel phenomenon in depth.

No stuck bits or residual programming problems were seen in any of the devices. Error bars on all graphs are based on Poisson counting statistics. Some exposures were done during programming or reading to determine any contribution these processes. No effect was seen.

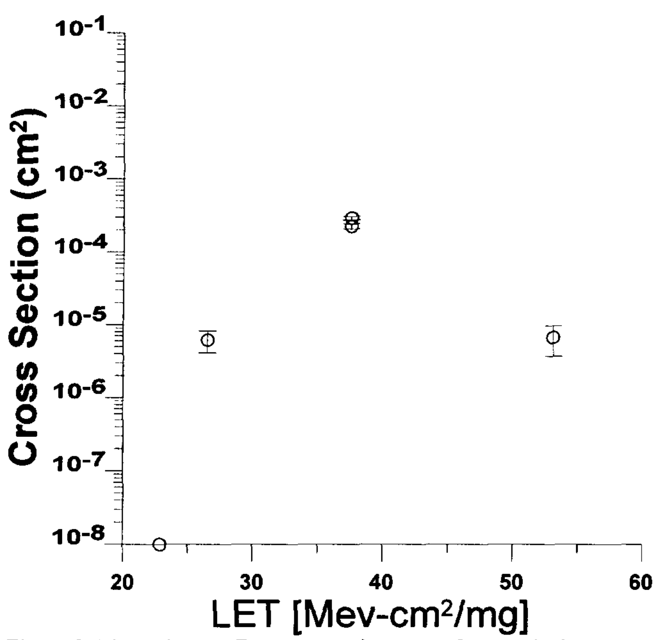

Figure 2. The SEU vs. LET cross section curve for a typical Ramtron FeRAM. Both the results of the 64 kbit and 256 kbit are shown.

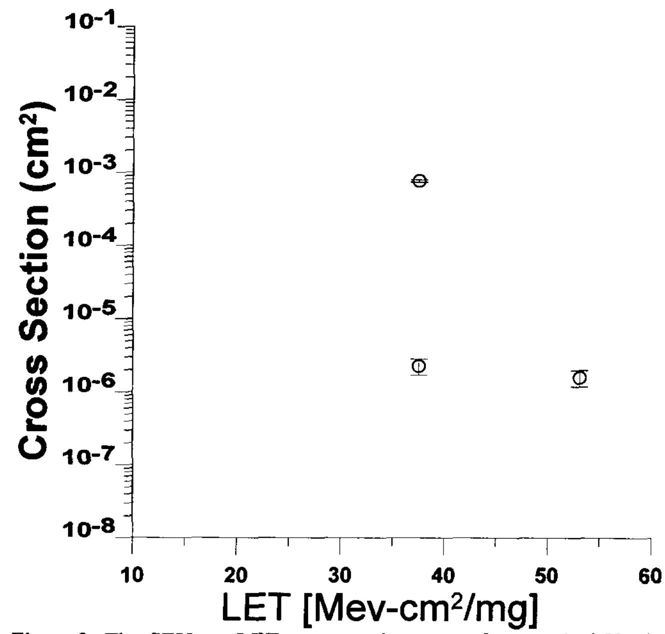

Figure 3. The SEU vs. LET cross section curve for a typical Hynix FeRAM.

B. SEL Results

Figures 4 and 5 show the cumulative SEL response for the Ramtron and Hynix devices, respectively. The LET threshold of the device is about 20 MeV/mg/cm2 in both cases.

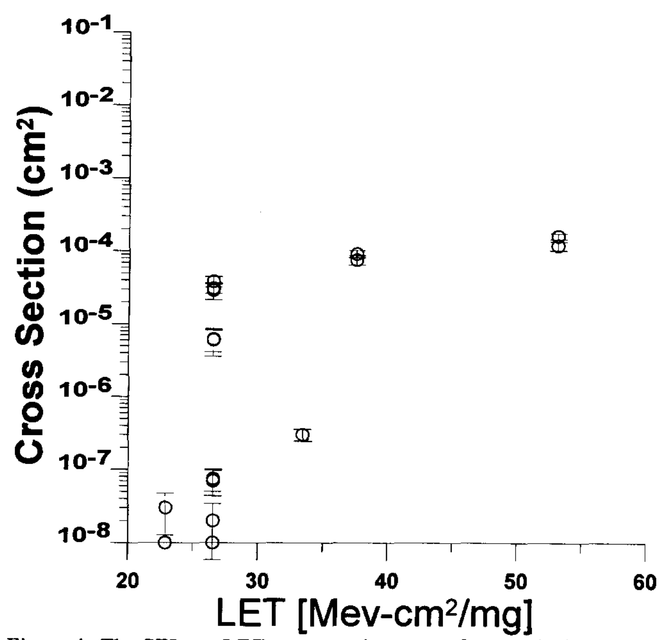

Figure 4. The SEL vs. LET cross section curve for a typical Ramtron FeRAM. Both the results of the 64 kbit and 256 kbit are shown.

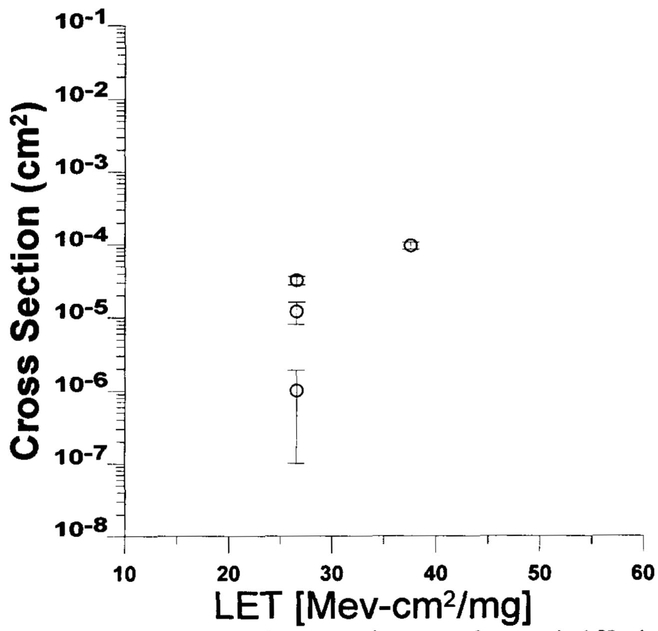

Figure 5. The SEL vs. LET cross-section curve for a typical Hynix FeRAM.

C. Threshold Calculation

The LET threshold of the device was found using two definitions. The typical 10% of saturation value definition was used. Another definition was the LET at which the cross-section would be the inverse of the number of bits multiplied by the estimated die area. This is approximately 10^{-7} cm^2 for all devices. Both LET thresholds are shown in Table 2 along with the SEL thresholds.

V. CONCLUSION

The radiation testing of these FeRAMs has shown that CMOS FeRAM technology is sensitive to SEU and less sensitive to SEL. The devices are mostly excluded from use in a severe radiation environment.

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Table 2. Thresholds for various FeRAMs.

Device	SEU Threshold Using 10% of Sat. (MeV cm^2/mg)	SEU Threshold 10^{-7} cm^{-2} floor. (MeV cm)	SEL Threshold (MeV cm^2/mg)
Hynix	30	30	25
Ramtron	22	22	20

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