Rapid Qualification of CSP Assemblies by Increase of Ramp Rates and Cycling Temperature Ranges

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ABSTRACT

A JPL-led chip scale package (CSP) Consortium of enterprises, composed of team members representing government agencies and private companies, have joined together to pool in-kind resources for developing the quality and reliability of chip scale packages (CSPs) for a variety of projects. Previous test results has now been published as a chip scale package guidelines document and distributed by Interconnection Technology Research Institute (ITRI).

The Consortium assembled fifteen different packages from 48 to 784 I/Os and pitches from 0.5 to 1.27 mm on multilayer FR-4 printed wiring board (PWB). In addition, two other test vehicles built by two team members, each had a control wafer level CSP package for data comparison. To meet various qualification needs of team members, assemblies were subjected to thermal cycling ranges representative of military , space, and commercial. The most rapid qualification was performed using thermal cycling in the range of –55 to 125°C with a near thermal shock ramp rates. Cycles-to-failure (CTF) test results to 3,000 cycles performed under this and three other thermal cycling ranges including 0 to 100° C are presented. The effect of ramp rate increase on CTFs and failure mechanisms for thermal cycling performed under near thermal shock and thermal cycle in the range of –55 to 125°C are also presented.

INTRODUCTION

Advanced electronics packaging, including CSPs, brought about new package technology including materials and processes as well new applications with environmental requirements not seen in their previous generation. Rapid insertion of electronics packaging technology necessitates faster qualification implementation and therefore development of accelerated test methods. Increase of ramp rate up to 20°C/min is allowed in a recently released specification, IPC 9701, "Performance Test Methods and Qualification Requirements for Surface Mount Solder Attachments".

Accelerated thermal cycling with a large temperature swing can be used for environmental screening test and often has been considered as qualification requirement for harsh environmental applications. There are many concerns, however, when such accelerations are performed especially for electronics packages with no environmental testing heritage. These concerns include: the effects of cold and hot temperatures in a cycle range, time and temperature at dwells, temperature exposure to higher than 110°C for eutectic solder, and the effects of heating/cooling rates.

In this investigation, in addition to providing CTFs under four thermal cycle condition for several FPBGAs, CSPs, and wafer level CSPs, the effects of heating/cooling rates will be also presented.

CSP TYPES AND TEST MATRIX

Chip Scale Packages (CSP) are now widely used for many electronic applications including portable and telecommunication products. The CSP definition has evolved as the technology has matured and refer to those packages with a pitch of 0.8 mm, aka fine pitch ball grid array (FPBGA), and lower. Packages with fine pitches especially those with less than 0.8 mm may require the use of microvia printed wiring board (PWB) which is costly and they may perform poorly when are assembled on board. A test vehicle (TV1) with eleven different package types and pitches was built using both standard and microvia PWBs and tested under various environmental conditions by the JPL MicrotypeBGA Consortium during 1997 to 1999. Lessons learned by the team were published as a guidelines document [1].

The finer pitch CSP packages which recently become available were included in the next test vehicle of the JPL CSP Consortium [2]. The Consortium team jointly concentrated their efforts on building of the second test vehicle (TV-2) with fifteen (15) packages. In addition to the TV-2 test vehicle, other test vehicles were designed and built by individual team members to meet their needs. For example, one test vehicle, herein refers to TV-H, was designed and assembled by Hughes Network System using their internal resources. The other test vehicle was designed by Litton/Northrop, TV-L, and manufactured at two facilities using their resources. At least one common package was included as control in each of these test vehicles in order to be able to compare the environmental test results and understand the effect of PWB build and manufacturing variables.

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TV-2 built by Consortium -- The PWBs were fabricated from FR-4 materials with 6 layers. Microvia design with 3 mil vias was considered for all packages except for the 784 I/O flip chip BGA in one design. In another design, estimated optimized PWB pads with 3 mil microvias was considered. The majority of PWBs had an organic solder preservative surface finish. Hot air solder level (HASL), immersion Au/Ni, and immersion silver were also used.

TV-H-- The PWB had four layers with the two resin coated copper (RCC) layers and an FR-4 core (1+2+1) having a total thickness of 0.43 mm. Microvia technology was used. The pad had a 0.1 mm (4 mil) microvia hole at the center of pad. A non-solder-mask-design (NSMD) pad with a diameter of 0.3 mm and 0.05 mm clearance was used. The surface finish of the PWB was Ni/Au immersion with about 2-8 micro inch of gold over 100-200 micro inch Ni. No clean solder paste was applied for assembly using a 5 mm laser-cut stencil thickness.

TV-L-- The PWBs had two layers of resin copper coated materials (RCCs) for ease of microvia formation at the top and bottom of glass epoxy core materials, with a total thickness of 1.62 mm (.065″).

Test Vehicle Features/Daisy Chain Patterns

All packages were daisy-chained, and they were divided into several internal chain patterns. The daisy chain pattern on the PWB completes the chain loop into the package through solder joints. Several probing pads connected to daisy chain loops were added for failure site diagnostic testing. All packages were prebaked prior to assembly.

TEST CONDITIONS

Thermal Cycling test

Thermal cycling was performed in four facilities, JPL (A, A_1), Boeing (B), StorageTek (C), and ITT (D), using different thermal profiles and cycling conditions. The cycles were in the range of -55 to 125°C and –30 to 100°, -55 to 125°C, 0 to 100°C, and -55 to 75°C, respectively. Figures 1 and 2 show the thermal profiles for chamber setting and thermal couple readings of A and B conditions. For A condition (-55/125°C), the heating and cooling rates were 2° to 5°C/min with a dwell at maximum temperature of more than 10 minutes and a shorter dwell time duration at the minimum temperature. Each cycle lasted 159 minutes.

The near thermal shock cycle, B condition, had the same temperature range performed in a chamber with three regions of hot, ambient, and cold. Heating and cooling rates were nonlinear and varied averaging between 10 to 15 °C/min with dwells at extreme temperatures of about 20 minutes. The total cycle lasted approximately 68 minutes.

The C condition ranged from 0 to 100°C had heating and cooling ramp rates of 14.29°C/min (7 minute ramps) with 10 and 2 minute dwells at hot and cold temperatures, respectively. The total cycle lasted 26 minutes.

The D condition in the range of –55 to 75°C was chosen to have equal ΔT value (130°C) as the A_1 condition (–30 to 100 °C) in order to be able to determine the effect of maximum temperature on CTFs. This condition had a 5°C/min ramp rates with dwells of 5 minutes at cold and 20 minutes at hot temperature.

Monitoring

All facilities were equipped with continuous monitoring systesms, eventhough they were different. All test vehicles were monitored continuously during the thermal cycles for electrical interruptions and opens. The criteria for an open solder joint specified in IPC-SM-785, Sect. 7.8, were used as guidelines to interpret electrical interruptions. In general, it is expected that once the first interruption is observed, there will be a large number of additional interruptions within the 10% of the cycle life. This was not the case for most assemblies. Generally, failures detected by continuous monitoring were verified manually at room temperature after periodical removal from the chamber.

Thermal Cycling Results

Failure Characteristics of Wafer Level CSPs

Figure 2 shows cycles to first failures for three different wafer level chip scale package (WLCSP) technology, I/O counts, and pitches. To generate plots, the CTFs were ranked from low to high and failure distribution percentiles were approximated using median plotting position, F_i = (i-0.3)/(n+0.4).

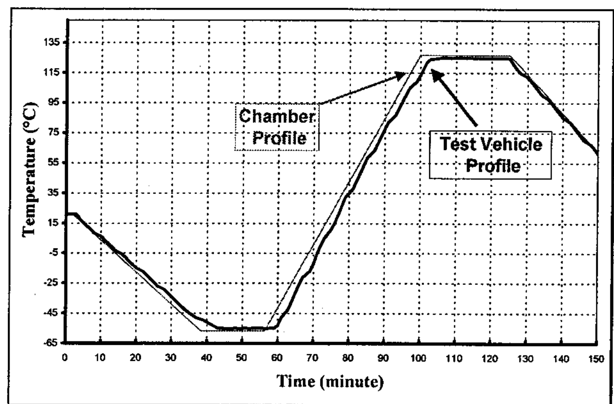

Figure 1 Thermal cycle profile in the range of –55°C to 125°C, condition A, 159 minutes/cycle

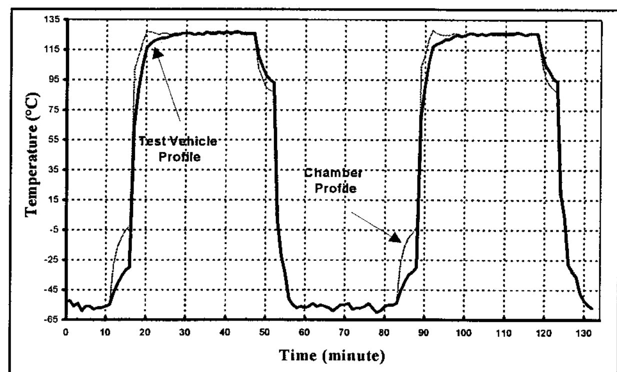

Figure 2 Near thermal shock profile in the range of –55°C to 125°C, condition B, 68 minutes/cycle

Often, two-parameter Weibull distributions have been used to characterize failure distribution and provide modeling for prediction in the areas of interest. The Weibull equation is

$$F(N) = 1 - \exp(-(N/No)^m)$$

where

F(N)	is the cumulative failure distribution function
N	is the number of thermal cycles
No	is a scale parameter that commonly is referred to as characteristic life, and is the number of thermal cycles with 63.2% failure occurrence.
m	is the shape parameter and for a large m is approximately inversely proportional to the coefficient of variation (CV) by 1.2/CV; that is, as m increases, spread in cycles to failure decreases

This equation, in double logarithm format, results in a straight line. The slope of the line defines the Weibull shape parameter. The cycles-to-failure data in log-log can be fitted to a straight line to calculate the two Weibull parameters.

The Weibull cumulative failure distribution was used to fit the experimental cycles-to-failure data for three WLCSPs. Weibull parameters were also generated and failure distributions were plotted in Figure 3 which are shown as continuous graphs. Weibull parameters for each assembly failure is also given. The m value ranged from 7 to 13, with the lowest value projected for the WLCSP48I/O-U8 based on an about 50% of total sample failures to 1,000 cycles.

The lowest CTFs were in the range of 276 to 451 cycles with No and m values of 377 and 8.2, respectively, for the 60 I/O WLCP with a 0.8 mm pitch. The solder joint failures for this package were at the package interface, verified by cross-sectioning and pull testing after dye-penetrant to detect the sites of failures. This package has already been modified by the manufacturer for improved reliability and is currently being evaluated by Consortium. The CTFs for the 54 I/O package with 0.8 by 1 mm pitches were in the range of 543 to 778 cycles with No and m values of 660 and 13, respectively. The 48 I/O package with a 1 mm pitch showed the highest CTFs, even though the first failure was at 638 cycles. Eight out of 17 packages failed to 1,000 cycles in the range of 638 to 959 cycles with estimated Weibull parameters of No and m values of 1,032 and 7, respectively.

Effects of Die Size and I/O Counts

CTFs for the FPBGA packages with different I/Os and die sizes are shown in Figure 4. For this package technology, the relative die size had the most significant effects on CTFs. The 208 I/O package with an 11.4 mm die size in a 15 mm package showed CTFs in the range of 176 to 573 cycles whereas the CTFs were in much higher range of 417 to 799 cycles for a 9.5 mm die size. The 180 I/O package with a 6.3 mm die in a 12 mm package failed at much higher failure cycles, six assemblies showed no failures to 1,000 cycles. The CTFs for those failed were in the range of 778 to 969 cycles.

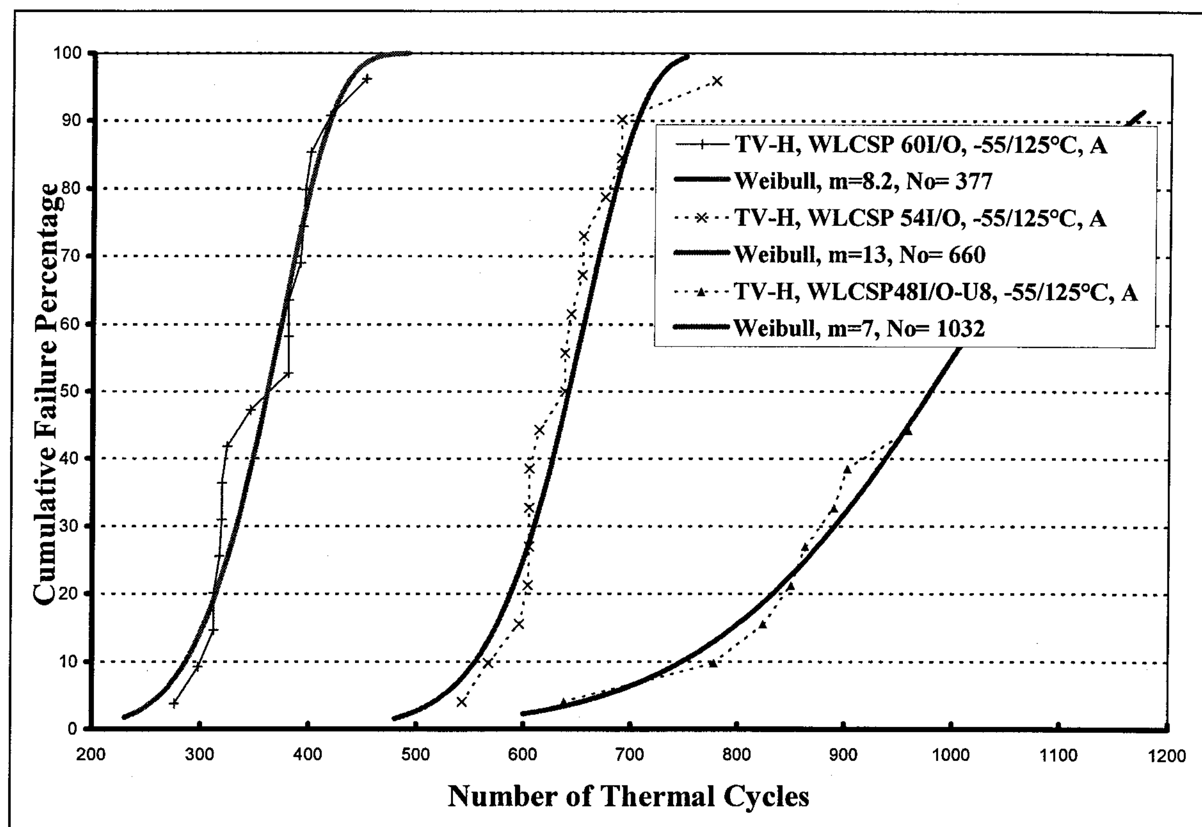

Figure 3 Cumulative failure distribution for three wafer level CSP assemblies under thermal cycle A condition (-55° C to 125°C)

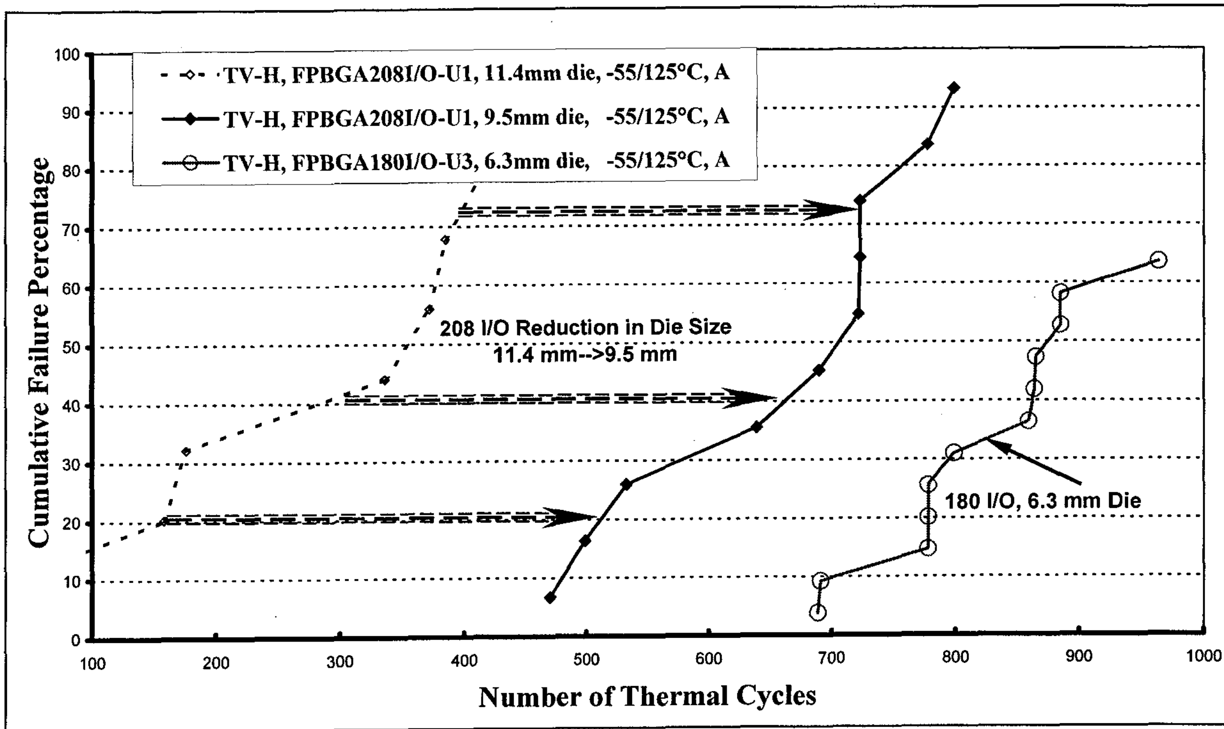

Figure 4 Cumulative failure distribution for an FPBGA technology with three different I/Os and die sizes under thermal Cycle A condition (-55 ° to 125°C)

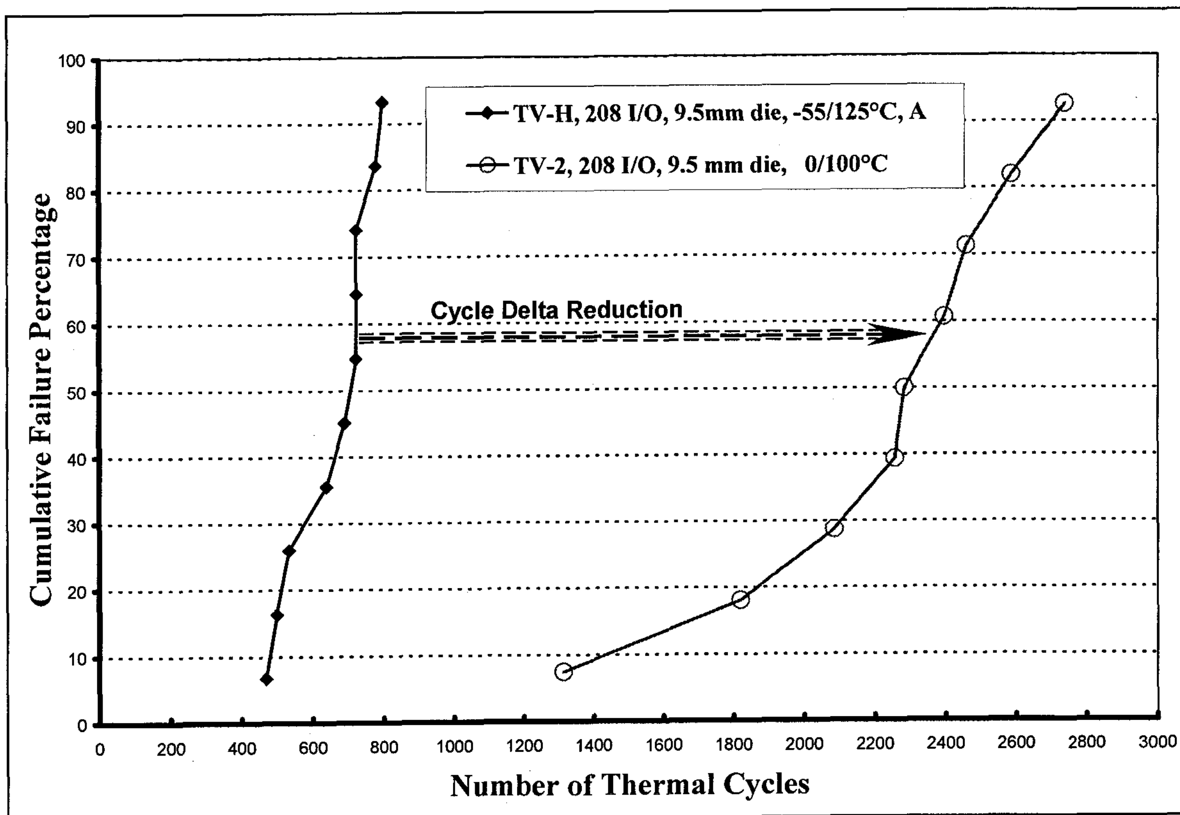

Figure 5 Cycles-to-failure data for the 208 I/O FPBGA, 0.8 mm pitch, under -55 ° to 125°C (A) and 0 to 100° C thermal cycle conditions. Failure mechanism was wear out at PWB interface.

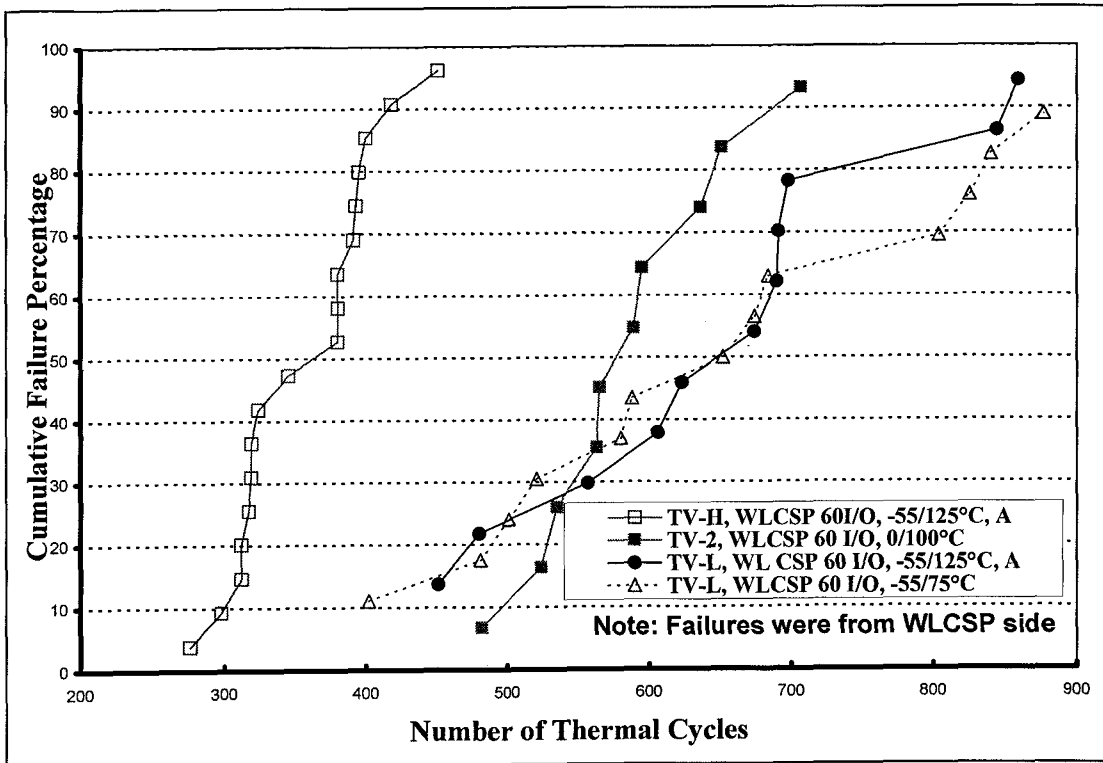

Figure 6 Cycles-to-failure data for the 60 I/O WLCSP, assembled on three different PWBs and cycled under three different conditions. Failures were at the package interfaces.

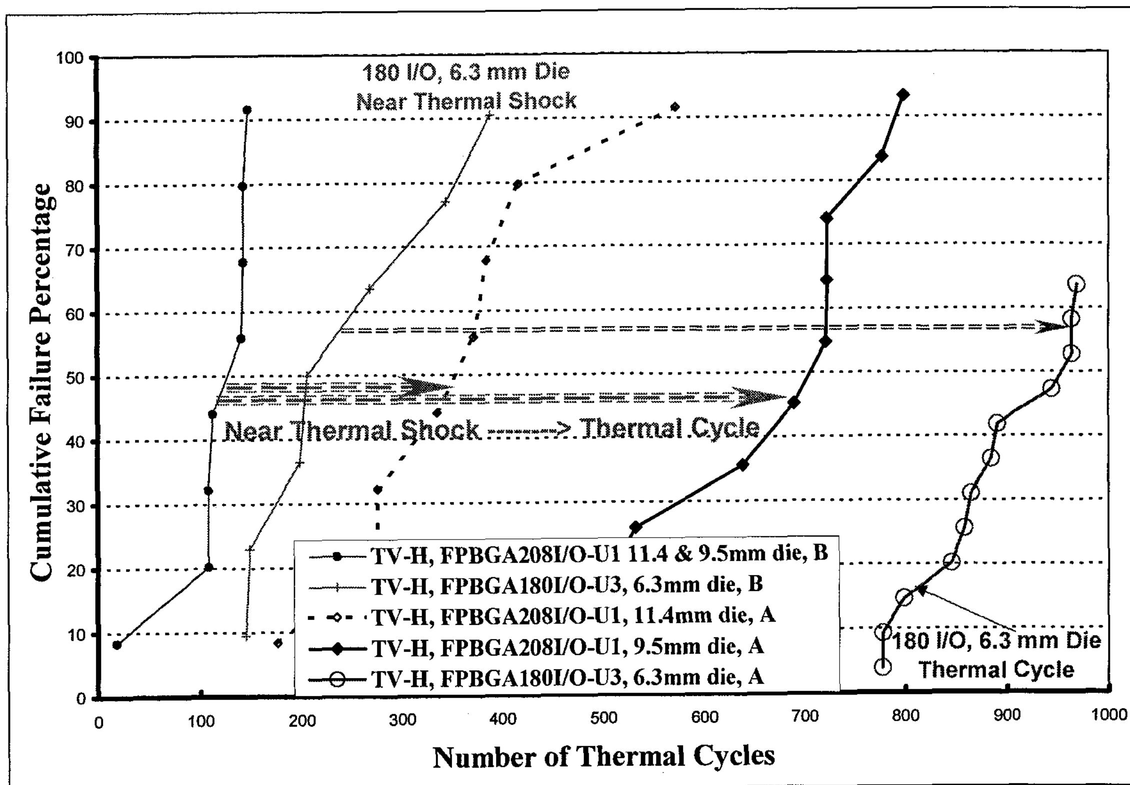

Figure 7 Cumulative failure distribution for two FPBGAs under equal thermal cycling range (-55 ° to 125°C), but different rates

Effects of Thermal Cycle ΔT for solder wear-out failure
CTFs for the 208 I/O FBPBGA package, 9.5 mm die, on TV-H and TV-2 under thermal cycling A (-55/125°C) and C (0/100°C) conditions are compared in Figure 5. CTFs under A condition were from 470 to 799 cycles with the 50% failures at 705 cycles. These values were 1315 to 2740 and 2284 cycles under C condition. The failure mechanism for this assembly was wear out of solder joint, and, therefore, the CTFs should be correlated by Coffin-Manson relationship, ignoring the effects of variables such as board pad design and thickness, manufacturing variables, and ramp rate and hold time for thermal cycle. In spite of these differences, using the values for the 50% failures, an acceptable coefficient of about 2 was calculated.

Effects of Thermal Cycle ΔT for WLCSP 60 I/O
CTFs for the 60 I/O WLCSP assembled on three different test vehicles and cycled under three conditions are compared in Figure 6. As discussed previously, the failures for this package were from package side. Only two data sets showed some indication of CTFs decrease with an increase in ΔT; there were no other apparent trends for the two sets. This is somewhat puzzling. One strong possible reason may be due to non-wear-out failure, i.e., failure from package side. Others may include difference in PWB thickness and pad design, manufacturing, and thermal cycling profile.

Effects of Thermal Cycle Ramp Rate
Figure 7 shows the test results for the 180 I/O FPBGA with a die size of 6.3 mm and the 208 I/O with the die sizes of 11.4 and 9.5 under the same thermal cycling range (-55°C/125°C), but with two different ramp rates, A and B conditions. It is apparent that under the near thermal shock cycle, the CTFs for the 208 I/O package with 11.4 and 9.5 mm dies were within the data scatter. This is not the case for those under thermal cycle A condition where the effect of die size clearly demonstrated. The CTFs for the 180 I/O package with a 6.3 mm die size are also differed significantly under two cycling conditions. The CTFs were in the range of 145 to 389 cycles for the near thermal shock whereas the first failure was observed at 689 cycles for the thermal cycle condition.

Conclusions
These conclusions are based on the CTFs that included many variables such as, use of small sample size of assemblies, variation in design and build of printed wiring boards, manufacturing build variables, difference in thermal cycling ranges and profiles, and in some cases termination fo testing prior to failures of all samples in population. Currently, addition thermal cycling on numerous other test vehicles including double-sided test vehicles are being performed and their failure analyses are being gathered to further substantiate and define the effects of various parameters on assembly reliability.

- CTFs for wafer level packages and FPBGAs with 0.8 mm pitch were relatively much lower than their 1.27 mm pitch BGA counterparts [1].
- Coffin-Manson relationship could be used to project CTFs for most cases, but not for one case. This is somewhat puzzling. One reason for such a mix test results is dominant failure at PWB (wear-our) for most cases and failure at package for the latter case.
- The effect of die size on CTFs were demonstrated—as die size increased, CTFs decreased. The relative die size to package may be considered as the most critical parameter. For example, for the 208 I/O FPBGA package with the largest relative die size to package dimension (11.4 mm die in 15x15 mm package) showed the lowest CTFs and the 180 I/O package with the lowest relative die size to package (6.3 mm die in 12x12 mm package) showed the highest CTFs under thermal cycle condition in the rang of –55 to 125°C.

Recommendations
The question is if increase in ΔT and ramp rates can be utilized to perform rapid qualification of CSPs. The answer is yes with some limitation. One of the key one is failure mechanism. It is recommended to establish any package materials and process weakness prior to assembly, e.g., integrity of ball attachment by slow and rapid shear testing as specified in IPC 9701. If the solder joint failure is by wear out at PWB, then it might be possible to increase thermal cycling temperature range to limits defined by materials and processes. It is also advisable to have ramp rate lower that 20°C/min. Be aware of the effect of board thickness and double-sided assemblies and their effects on reliability, especially when extrapolating CTFs for application.

Acknowledgments
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2. Ghaffarian, R., Nelson, G, Cooper, M., Lam, D., Strudler, S., Umdekar, A., Selk, K., Bjorndahl, B., Duprey, R., "*Thermal Cycling Test Results of CSP and RF Package Assemblies*", The Proceedings of Surface Mount International

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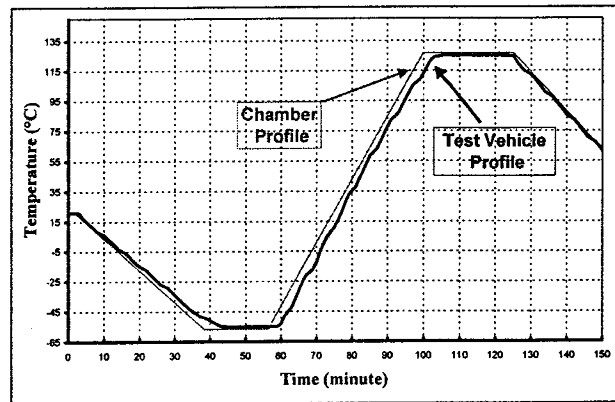

Figure 1 Thermal cycle profile in the range of –55°C to 125°C, condition A, 159 minutes/cycle

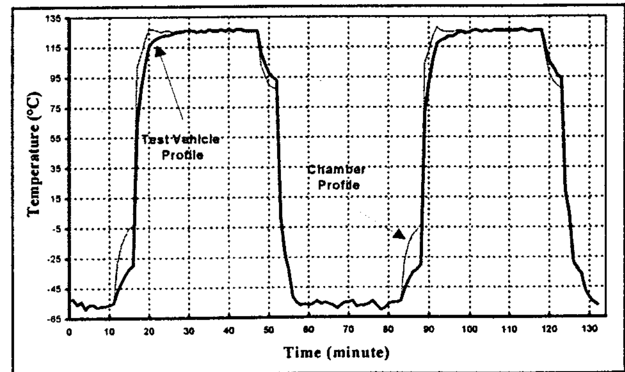

Figure 2 Near thermal shock profile in the range of –55°C to 125°C, condition B, 68 minutes/cycle

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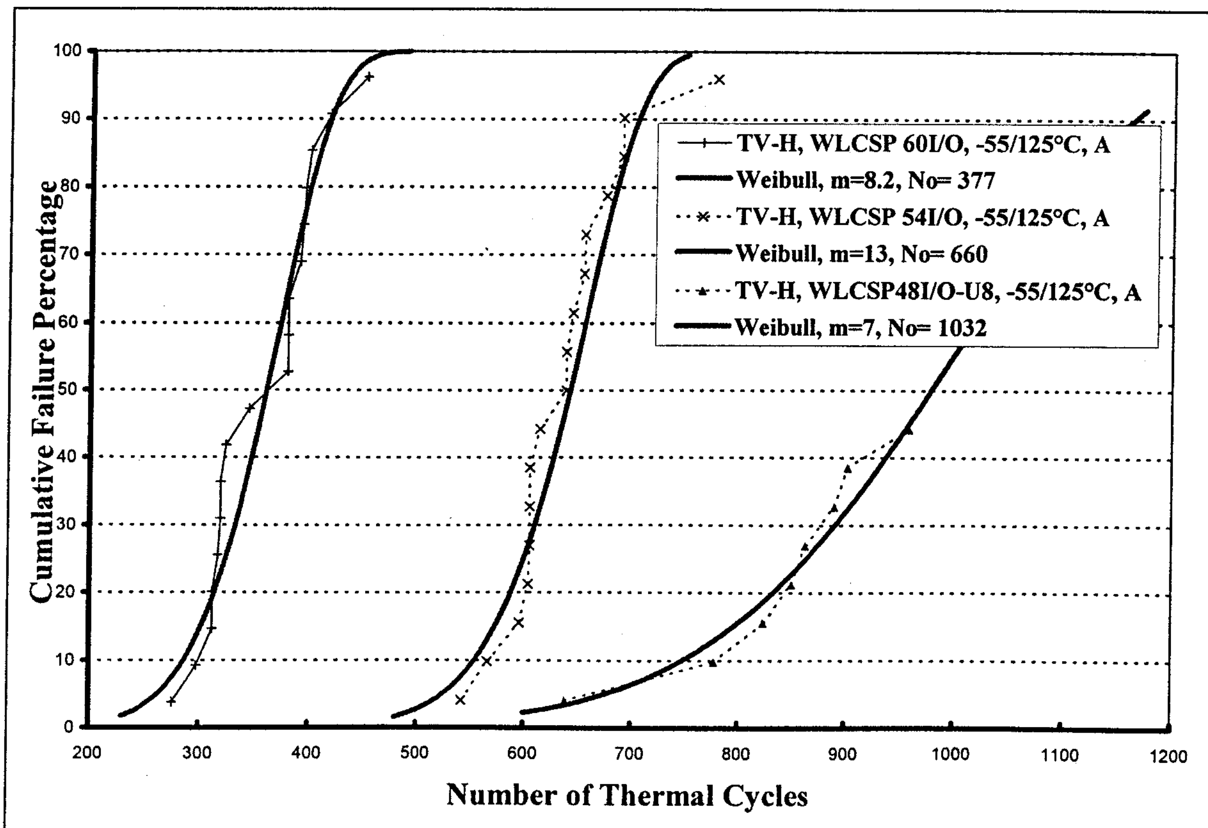

Figure 3 Cumulative failure distribution for three wafer level CSP assemblies under thermal cycle A condition (-55° C to 125°C)

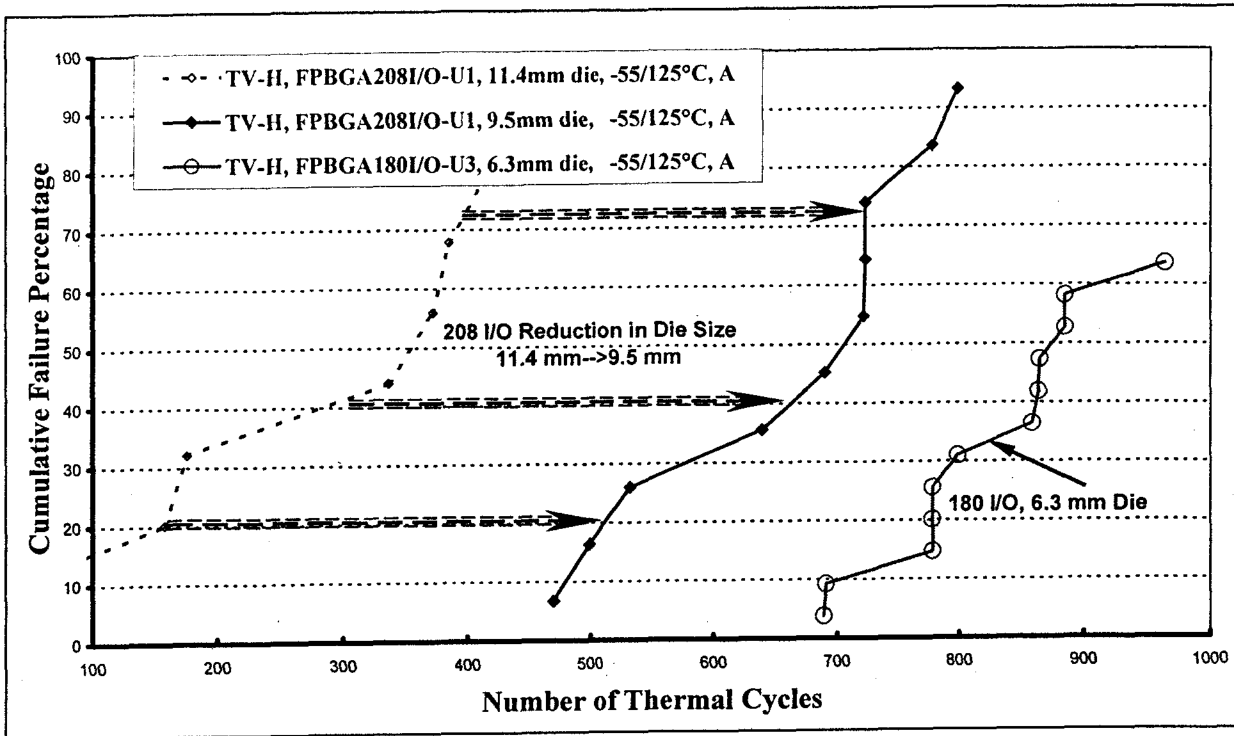

Figure 4 Cumulative failure distribution for an FPBGA technology with three different I/Os and die sizes under thermal Cycle A condition (-55 ° to 125°C)

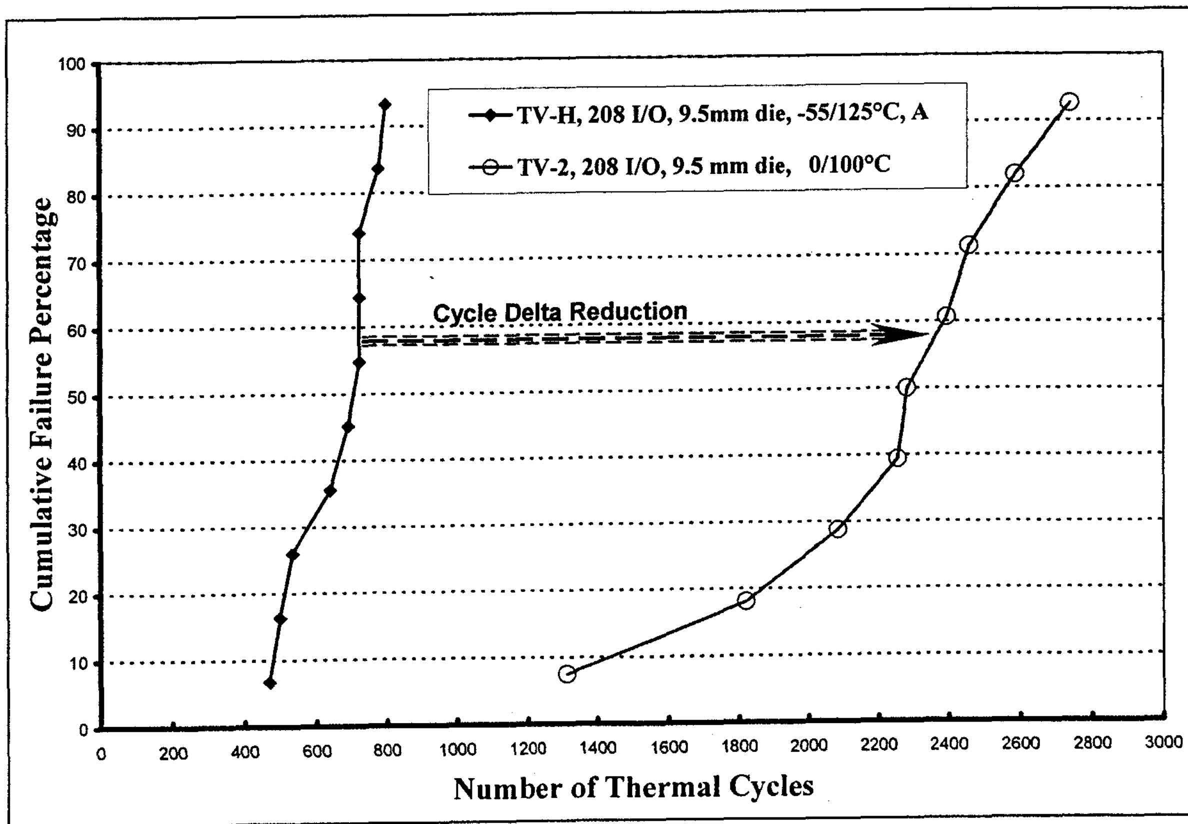

Figure 5 Cycles-to-failure data for the 208 I/O FPBGA, 0.8 mm pitch, under -55 ° to 125°C (A) and 0 to 100° C thermal cycle conditions. Failure mechanism was wear out at PWB interface.

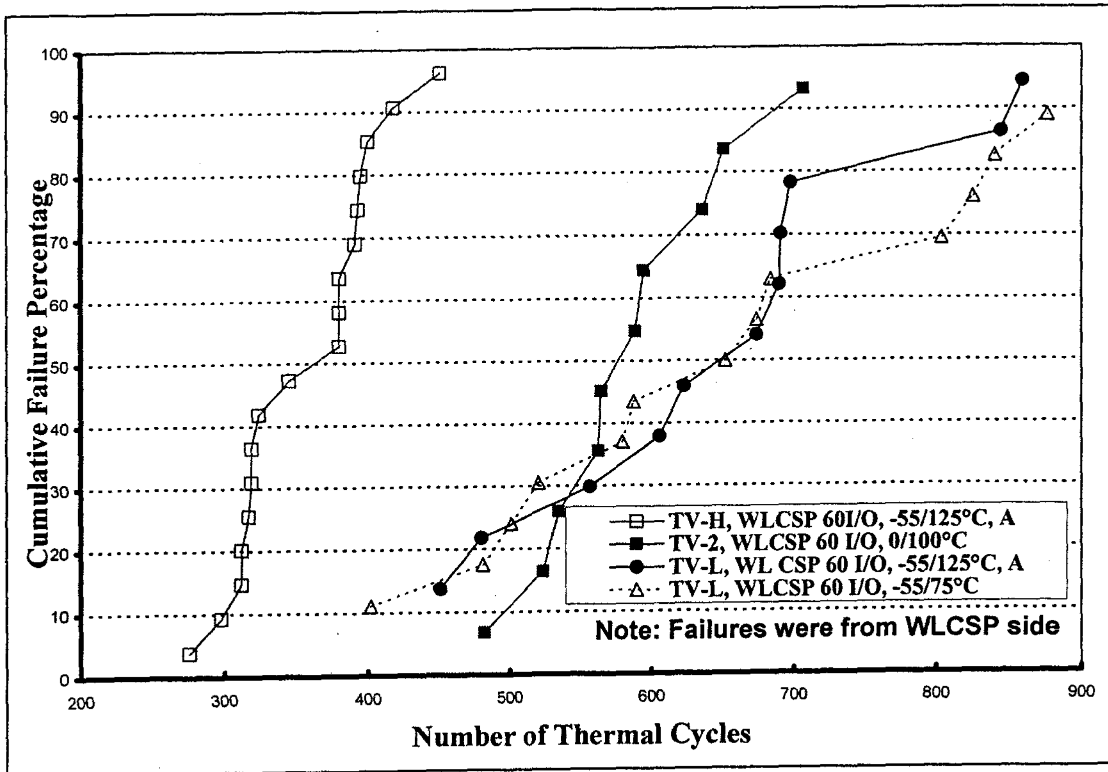

Figure 6 Cycles-to-failure data for the 60 I/O WLCSP, assembled on three different PWBs and cycled under three different conditions. Failures were at the package interfaces.

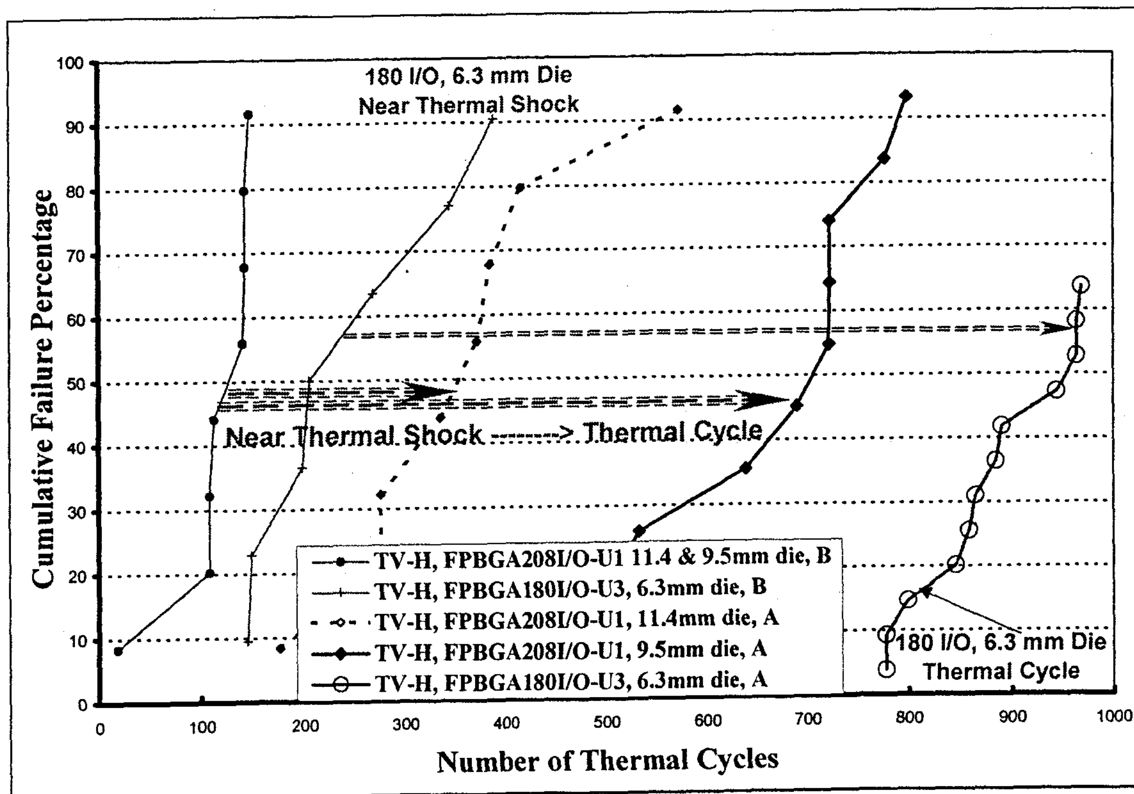

Figure 7 Cumulative failure distribution for two FPBGAs under equal thermal cycling range (-55 ° to 125°C), but different rates

Effects of Thermal Cycle ΔT for solder wear-out failure
CTFs for the 208 I/O FBPBGA package, 9.5 mm die, on TV-H and TV-2 under thermal cycling A (-55/125°C) and C (0/100°C) conditions are compared in Figure 5. CTFs under A condition were from 470 to 799 cycles with the 50% failures at 705 cycles. These values were 1315 to 2740 and 2284 cycles under C condition. The failure mechanism for this assembly was wear out of solder joint, and, therefore, the CTFs should be correlated by Coffin-Manson relationship, ignoring the effects of variables such as board pad design and thickness, manufacturing variables, and ramp rate and hold time for thermal cycle. In spite of these differences, using the values for the 50% failures, an acceptable coefficient of about 2 was calculated.

Effects of Thermal Cycle ΔT for WLCSP 60 I/O
CTFs for the 60 I/O WLCSP assembled on three different test vehicles and cycled under three conditions are compared in Figure 6. As discussed previously, the failures for this package were from package side. Only two data sets showed some indication of CTFs decrease with an increase in ΔT; there were no other apparent trends for the two sets. This is somewhat puzzling. One strong possible reason may be due to non-wear-out failure, i.e., failure from package side. Others may include difference in PWB thickness and pad design, manufacturing, and thermal cycling profile.

Effects of Thermal Cycle Ramp Rate
Figure 7 shows the test results for the 180 I/O FPBGA with a die size of 6.3 mm and the 208 I/O with the die sizes of 11.4 and 9.5 under the same thermal cycling range (-55°C/125°C), but with two different ramp rates, A and B conditions. It is apparent that under the near thermal shock cycle, the CTFs for the 208 I/O package with 11.4 and 9.5 mm dies were within the data scatter. This is not the case for those under thermal cycle A condition where the effect of die size clearly demonstrated. The CTFs for the 180 I/O package with a 6.3 mm die size are also differed significantly under two cycling conditions. The CTFs were in the range of 145 to 389 cycles for the near thermal shock whereas the first failure was observed at 689 cycles for the thermal cycle condition.

Conclusions
These conclusions are based on the CTFs that included many variables such as, use of small sample size of assemblies, variation in design and build of printed wiring boards, manufacturing build variables, difference in thermal cycling ranges and profiles, and in some cases termination fo testing prior to failures of all samples in population. Currently, addition thermal cycling on numerous other test vehicles including double-sided test vehicles are being performed and their failure analyses are being gathered to further substantiate and define the effects of various parameters on assembly reliability.

- CTFs for wafer level packages and FPBGAs with 0.8 mm pitch were relatively much lower than their 1.27 mm pitch BGA counterparts [1].
- Coffin-Manson relationship could be used to project CTFs for most cases, but not for one case. This is somewhat puzzling. One reason for such a mix test results is dominant failure at PWB (wear-our) for most cases and failure at package for the latter case.
- The effect of die size on CTFs were demonstrated—as die size increased, CTFs decreased. The relative die size to package may be considered as the most critical parameter. For example, for the 208 I/O FPBGA package with the largest relative die size to package dimension (11.4 mm die in 15x15 mm package) showed the lowest CTFs and the 180 I/O package with the lowest relative die size to package (6.3 mm die in 12x12 mm package) showed the highest CTFs under thermal cycle condition in the rang of –55 to 125°C.

Recommendations
The question is if increase in ΔT and ramp rates can be utilized to perform rapid qualification of CSPs. The answer is yes with some limitation. One of the key one is failure mechanism. It is recommended to establish any package materials and process weakness prior to assembly, e.g., integrity of ball attachment by slow and rapid shear testing as specified in IPC 9701. If the solder joint failure is by wear out at PWB, then it might be possible to increase thermal cycling temperature range to limits defined by materials and processes. It is also advisable to have ramp rate lower that 20°C/min. Be aware of the effect of board thickness and double-sided assemblies and their effects on reliability, especially when extrapolating CTFs for application.

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