PROTOTYPING AN FPGA-BASED MAP SYNCHRONIZER FOR VERY HIGH RATE FQPSK. N. E. Lay, A. Gray, E. Kang, Jet Propulsion Laboratory, California Institute of Technology, Pasadena, CA, e-mail: norman.e.lay@jpl.nasa.gov.

Introduction: While fundamental formulations of maximum *a posteriori* (MAP) estimation for symbol timing [1] have been in existence for some time, it has generally not seen widespread usage in communications receivers due to its relatively greater complexity in comparison to other designs. However, MAP has been shown to provide significant performance advantages for the acquisition and tracking of digital modulations under low SNR conditions when compared to traditional techniques, such as the data transition tracking loop [2]. In this paper, we describe the development efforts to prototype a high speed MAP synchronizer, implemented with field programmable gate array (FPGA) technology. The principal objective of this work is the design, demonstration and evaluation of the synchronizer utilizing a 200-300 Msps FQPSK signal as the test waveform. Since it has been recently recommended by the CCSDS as a spectrally efficient, modulation format for use in high rate, near Earth communications applications, FQPSK serves as an appropriate candidate for the initial synchronizer design and evaluation.

Design Approach, Parallel Algorithms and Synchronizer Architecture: The choice of an FPGA implementation has been driven by a number of different considerations. These include rapidity in hardware prototyping, hardware platform re-use through reconfigurability, IP capture and straightforward design migration for ASIC implementation. By selecting a digital CMOS technology for implementation of the signal processing algorithms, we achieve the advantage of lower power consumption over other high-speed IC processes, such as GaAs. The attendant constraint requires system clock rates many factors below the input sample rate required for digitizing Mbaud signals, thereby requiring the formulation and use of efficient parallel processing algorithms.

A block diagram of a prototype hardware configuration is shown in figure 1 and depicts a state-of-the-art digitizer, typically operating in the GHz range. Its sample outputs are then de-multiplexed to lower the data interface rate to a frequency that can be supported by the FPGA.

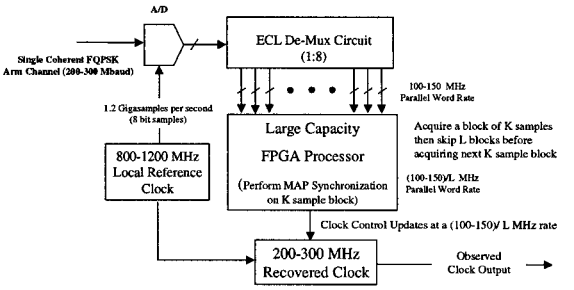

Figure 1. Prototype Hardware

The synchronizer algorithms developed for the FPGA are then developed to operate on block sample inputs and require the effective use of numerous parallel correlation elements to achieve the throughput required to process all incoming samples. This paper will describe several algorithms ranging from high precision interpolative approaches to techniques that operate on subsampled data blocks. Tradeoffs between required gate array capacity, operating frequency and overall performance will also be discussed. In addition, simulation performance and laboratory results will also be compared.

References: [1] W. C. Lindsey and M. K. Simon, *Telecommunication Systems Engineering*, Prentice-Hall, NJ, 1973. [2] L. V. Lam, T.-Y. Yan, M. K. Simon and W. L. Martin, "Acquisition Performance Comparison of the Generalized Maximum A Posteriori Symbol Synchronizer Versus the Data-Transition Tracking Loop", JPL TMO Progress Report 42-132, February 15, 1998. [3] S. Kato and K. Feher, "Correlated Signal Processor", U.S. Patent 4,567,602, January 1986. [4] M. K. Simon and T.-Y. Yan, "Performance Evaluation and Interpretation of Unfiltered Feher-patented Quadrature Phase Shift Keying (FQPSK)", JPL TMO Progress Report 42-137, May, 1999.