

# A 128 x 128 CMOS Active Pixel Image Sensor for Highly Integrated Imaging Systems

Sunetra K. Mendis\*, Sabrina E. Kemeny and Eric R. Fossum

Center for Space Microelectronics Technology  
Jet Propulsion Laboratory, California Institute of Technology  
4800 Oak Grove Drive, Pasadena, CA 91109

## Abstract

A new CMOS-based image sensor that is intrinsically compatible with on-chip CMOS circuitry is reported. The new CMOS active pixel image sensor achieves low noise, high sensitivity, X-Y addressability, and has simple timing requirements. The image sensor was fabricated using a 2  $\mu\text{m}$  p-well CMOS process, and consists of a 128 x 128 array of 40  $\mu\text{m}$  x 40  $\mu\text{m}$  pixels. The CMOS image sensor technology enables highly integrated smart image sensors, and makes the design, incorporation and fabrication of such sensors widely accessible to the integrated circuit community.

## 1. Introduction

In most smart image sensors, it is highly desirable to integrate on-chip circuitry to both control the image sensor and perform signal and image processing on the output image. Charge-coupled devices (CCDs) which are typically employed for image acquisition are not easily integrable with CMOS circuitry due to additional fabrication complexity leading to high cost, and the high capacitances seen by on-chip driving circuitry. Limited on-chip signal and image processing has been performed with CCDs using charge domain circuits [1-6]. Although CCD imagers achieve high fill-factors, high quantum efficiency, low noise and large formats, it is difficult to implement random access and fast readout rates. A CCD is read out by sequentially transferring the signal charge through the semiconductor, and the readout rate is limited by the need for nearly perfect charge transfer to maintain signal fidelity. Photodiode arrays are amenable to integration with CMOS technology and offer X-Y addressability, but suffer from large noise levels, poor response uniformity and image lag [7]. Other sensor technologies that are CMOS-compatible include the charge modulation device (CMD) [8] and the bulk charge modulation device (BCMD) [9]. Both these technologies require specialized fabrication processes that are not available to most circuit designers.

An active-pixel-sensor (APS) is defined as a detector array technology with one or more active transistors within the pixel unit cell [10]. The signal is read out through a metal wire which eliminates the signal degradation due to charge-transfer inefficiency suffered by CCD imagers. This allows fast, selective readout of windows of interest.

The new CMOS-based image sensor that is reported in this paper is intrinsically compatible with on-chip CMOS circuitry. The CMOS image sensor technology enables highly integrated smart image sensors for machine vision, robotics, guidance and navigation, automotive applications, and some consumer products such as computer input devices, video phones, and home surveillance. Since the process is CMOS, the design, incorporation and fabrication of such sensors becomes widely accessible to the integrated circuit community.

## 2. Design and Operation

The CMOS active pixel sensor is shown schematically in Fig. 1. The devices within the dotted outline are contained in the pixel unit cell. The pixel unit cell consists of a photo-gate

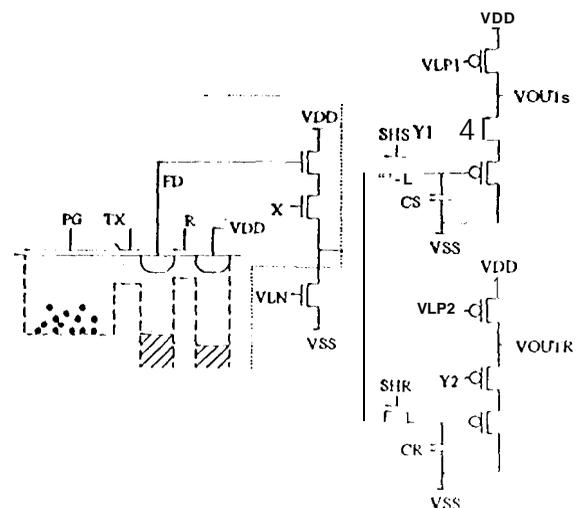


Fig. 1. Schematic of active-pixel-sensor unit cell and readout circuit.

\* S. Mendis is a Ph.D. student in the Department of Electrical Engineering, Columbia University, New York, performing her dissertation research at JPL.

PG, a d.c. biased transfer gate TX and an output diffusion FD. It also contains a reset transistor R, a source-follower input transistor and a row-selection transistor X. In essence, a small surface-channel CCD has been fabricated in each pixel. At the bottom of each column of pixels, there is a load transistor VLN and two output branches to store the reset and signal levels. Each branch consists of a sample and hold capacitor (CS or CR) with a sampling switch (SHS or SHR) and a second source-follower with a column-selection switch (Y1 or Y2). The readout circuits are common to an entire column of pixels, except the load transistors of the second set of source followers VLP1 and VLP2, which are common to the entire array,

The operation of the CMOS active-pixel sensor is illustrated in Fig. 2. It is assumed that the rail voltages are 5V and 0V, although higher and lower voltage operation is possible and has been demonstrated. The transfer gate TX and the source follower load transistors VLN, VLP1 and VLP2 are biased at 2.5V. During the signal integration period (Fig. 2a), photo-generated electrons are collected under the photo-gate biased high at 5V. The reset transistor R is biased at 2.5V to act as a lateral anti-blooming drain, and the row-selection transistor X is biased off (0V). Following signal integration, an entire row of pixels are read out simultaneously. First, the row of pixels to be read out are addressed by enabling row selection switch X. The pixel output node FD is reset by briefly pulsing the reset gate R to 5V, to reset the floating diffusion output node FD to approximately 3.5V (Fig. 2b). The output of the first source follower is sampled onto capacitor CR at the bottom of the column by enabling sample

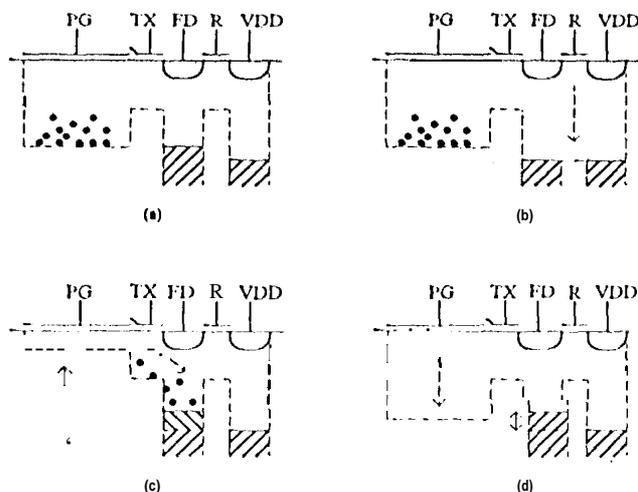


Fig. 2. Operation of the active-pixel-sensor: (a) signal integration; (b) reset; (c) signal charge transfer; (d) signal readout

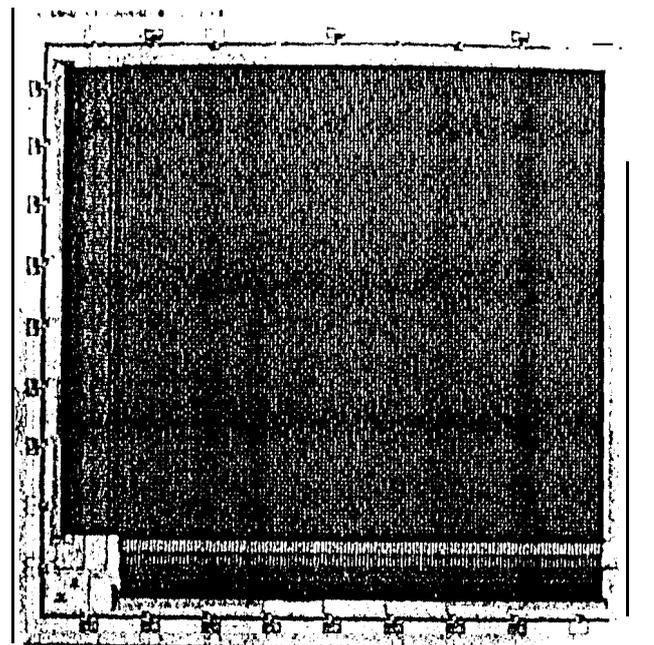


Fig. 3. Photograph of completed integrated circuit.

and hold switch SHR. Then, PG is pulsed low to 0V, transferring the signal charge to FD (Fig. 2c). The new output voltage is sampled onto capacitor CS by enabling sample and hold switch SHS (Fig. 2d). The stored reset and signal levels are sequentially scanned out through the second set of source followers by enabling column address switches Y1 and Y2. Storing the reset and signal levels on separate capacitors permits correlated double sampling (CDS) which suppresses kTC noise from the pixel and 1/f noise and threshold variations from the output transistor [11]. The main source of noise in this system is the kTC noise introduced by the sample and hold capacitors. The calculated r.m.s. noise on each 1 pF capacitor is 64  $\mu$ V, resulting in 91  $\mu$ V for differential mode.

The pixel unit cell and read out circuits were designed to achieve 30 Hz operation of a 128 x 128 array. The fabricated image sensor consists of a 128 x 128 array of active pixels, row and column address decoders, clock generator circuits and a bank of sample and hold capacitors and read out circuits. A double-poly, double-metal p-well CMOS process with 2  $\mu$ m design rules was used through MOSIS, resulting in a 40  $\mu$ m x 40  $\mu$ m pixel size. The fill-factor calculated as the ratio of the active area in the design to the total pixel area is 26%. The 7-bit row and column address decoders were formed using standard CMOS logic permitting direct

X-Y addressing of the image sensor. The address decoders and the clock generator circuits were laid out to fit within the 40  $\mu\text{m}$  pixel pitch. The completed IC fits a standard MOSIS 6.8mm x 6.8mm die and was packaged in a 40 pin DIP. A photograph of the completed IC is shown in Fig. 3.

### 3. Experimental Results

The active pixel image sensor was operated with the timing and voltages described above. Both dark and illuminated testing of the sensor was performed. By performing electrical tests on a test structure on a separate IC, the pixel sensitivity was determined to be  $4.0 \mu\text{V}/\text{e}^-$ . The sensor was nominally clocked at  $2 \mu\text{s}/\text{pixel}$ , corresponding to a frame rate of approximately 30 Hz. Although the well capacity was calculated to be approximately  $6 \times 10^6 \text{e}^-$ , saturation was determined by the output amplifier, and was observed to be 600 mV or 150,000  $\text{e}^-$ . Global fixed pattern noise (FPN) observed in the differential output signal was approximately 20 mV p-p (3.3% sat.), with a local variation of approximately 8 mV p-p. The global variation is attributed to poor control of the p-well potential towards the center of the array since slower clocking rates reduced the effect, and an earlier 28 x 28 array showed a similar but much smaller effect. Dark current was measured to be approximately  $62 \text{e}^-/\text{nm}^2/\text{pixel}$ , or under  $1 \text{nA}/\text{cm}^2$ . Noise in the fabricated array is fundamentally limited to 22  $\text{e}^-$  r.m.s. due to the kTC noise on the 1 pF sample and hold capacitors. However, the measured noise level at a 30 Hz frame rate at room temperature is presently limited by dark current shot noise (approximately 42  $\text{e}^-$  r.m.s., for a dynamic range of 71 dB. No

lag or smear was observed and blooming was suppressed through the biasing of the reset transistor R. A laser spot scan of a single pixel was performed with a 632 nm He-Ne laser with a beam diameter of approximately  $1.5 \mu\text{m}$ . The responsivity map of the pixel scanned with a step size of  $2 \mu\text{m}$  is presented in Fig. 4. The layout of the pixel is shown in Fig. 5 for comparison. The response is uniform across the poly1 photo-sate area with no overlap of poly2 or metal, and drops off rapidly at the edges. A lower response is noticeable in areas overlapped by poly2. Performance of the sensor is summarized in table 1. Images acquired by the CMOS active pixel sensor were displayed on a video monitor. A photograph of a US one dollar bill taken from the video monitor is shown in Fig. 6.

### 4. Conclusions

A new CMOS-based image sensor that is well suited for highly integrated imaging systems has been presented. Significant improvement in CMOS active-pixel-sensor is anticipated in the near future. Reducing fixed-pattern noise through the use of an n-well process and improvements in the column CDS circuitry are currently being investigated. A pixel design with a floating gate output structure enabling multiple read operations is also being considered. Reduction in pixel size through the use of  $0.8 \mu\text{m}$  CMOS technology should reduce dark current. The use of microlenses will improve the effective fill-factor to over 100%. This initial work paves the way for the development of more complex pixel structures and the integration of on-chip electronics in the future.

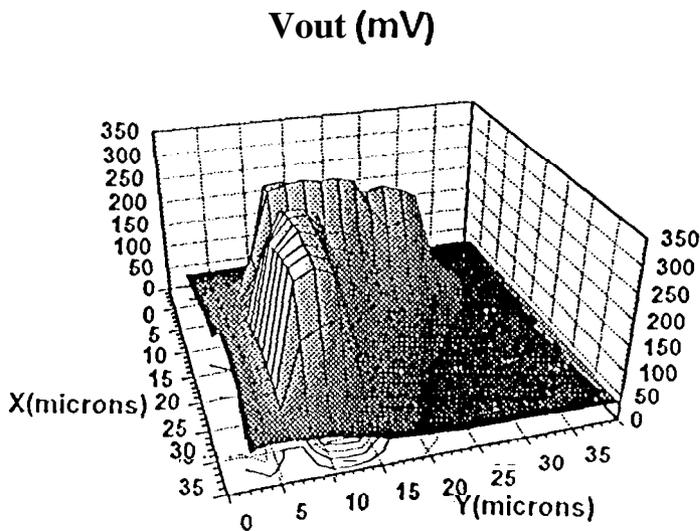


Fig. 4. Responsivity map of pixel

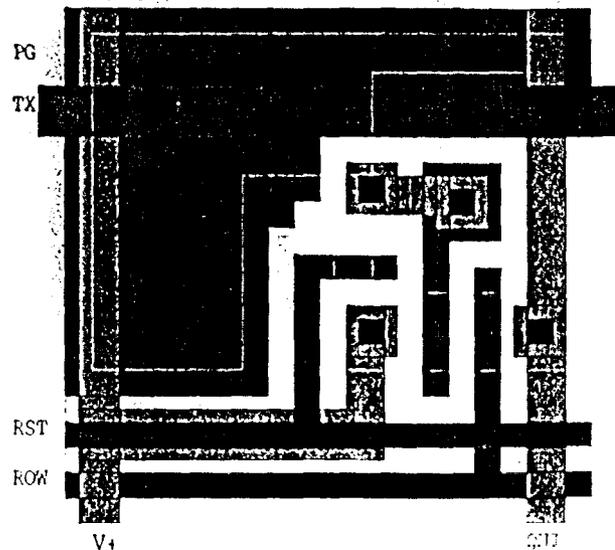


Fig. 5 Layout of pixel

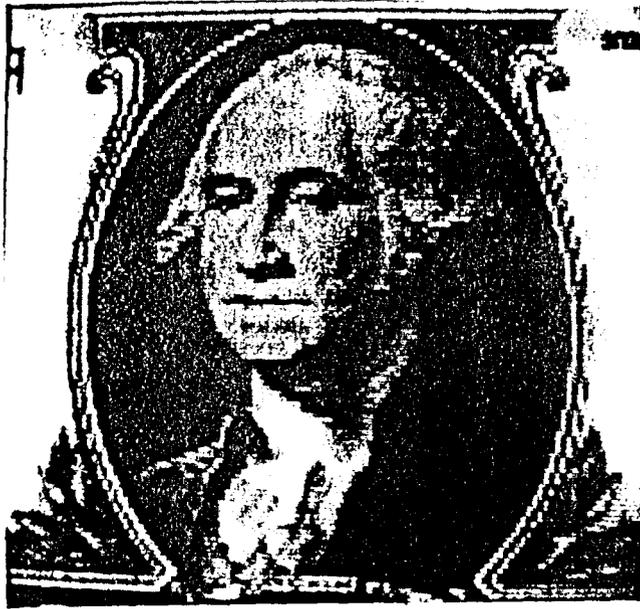


Fig. 6: Photograph of US \$1 bill taken from video monitor.

### S. Acknowledgments

The authors appreciate useful conversations and encouragement from our colleagues at JPL, especially B. Pain, R. Gee, C. Stevens, B. Wilcox and R. Bartman. The authors would like to acknowledge the assistance of Q. Kim of JPL who performed the laser spot scan experiment. The support of V. Sarohia of JPL and G. Johnston of NASA Headquarters is gratefully acknowledged.

The research described in this paper was carried out at the Jet Propulsion Laboratory, California Institute of Technology, and was sponsored by the Defense Advanced Research Projects Agency and the National Aeronautics and Space Administration.

Reference herein to any specific commercial product, process or service by trade name, trademark, manufacturer or otherwise, does not constitute or imply endorsement by the United States Government or the Jet Propulsion Laboratory, California Institute of Technology.

Table 1. CMOS Active Pixel Image Sensor

PARAMETER	UNIT	VALUE
Technology	—	2 $\mu\text{m}$ p-well CMOS
Pixel Size	—	40 $\mu\text{m}$ x 40 $\mu\text{m}$
Array Size	—	128 x 128
Aperture	—	26%
Required Voltages	—	Clocks: 0, 5V; V <sub>dd</sub> : c. 5.2V; V <sub>ss</sub> : 0V
Dark Current	—	62 e <sup>-</sup> /ms/pixel
Nominal Pixel Readout	—	500,000 pixels/s
Output Sensitivity	—	4.0 $\mu\text{V}/\text{e}^-$
Noise	—	42 e <sup>-</sup> r.m.s.
Saturation	—	150,000 e <sup>-</sup>
Dynamic Range	—	71 dB
Fixed Pattern Noise	—	3.3% p-p/sat

### 6. References

- [1] E. R. Fossum, "Architectures for focal-plane image processing," *Optical Engineering*, vol. 28(8) pp. 865-871 (1989).
- [2] E. R. Fossum, "Charge-coupled computing for focal-plane image processing," *Optical Engineering*, vol. 26(9) pp. 916-922 (1987).
- [3] W. Yang and A. Chiang, "A full-fill color CCD imager with integrated signal processors," *Proc. 1990 IEEE International Solid-State Circuits Conference*, pp. 218-219 (1990).
- [4] F.-S. Eid and E. R. Fossum, "Real time focal-plane array image processor," in *Automated Inspection and High Speed Vision Architectures III*, *Proc. SPIE* vol. 1197, paper 1 (1989).
- [5] S. E. Kemeny, F.-S. Eid, S. Mendis and E. R. Fossum, "Update on focal-plane image processing research" in *Charge-Coupled Devices and Solid-State Optical Sensors II*, *Proc. SPIE* vol. 1447, pp. 243-250 (1991).
- [6] S. E. Kemeny, H. Torbey, H. Meadows, R. Bredthauer, M. I. Shell and E. R. Fossum, "CCD focal-plane image reorganization processors for lossless image compression," *IEEE J. Solid-stat. Circuits*, vol. 27(3) pp. 398-405 (1992).
- [7] O. Yadid-Pecht, R. Ginosar and Y. Shacham-Diamand, "A Random access photodiode array for intelligent image capture," *IEEE Trans. Electron Devices*, vol. 38(8), pp. 1772-1780 (1991).
- [8] M. Ogata, T. Nakamura, K. Matsumoto, R. Ohta and R. Hyuga, "A Small pixel CMD image sensor," *IEEE Trans. Electron Devices*, vol. 37(4) pp. 964-971 (1990).
- [9] J. Hynacek, "An improved photosite structure for high density image sensors" *IEEE Trans. Electron Devices*, vol. 38(5), pp. 1011-1020 (1991).
- [10] E. R. Fossum, "Active pixel sensors - are CCDs dinosaurs?," *Proc. SPIE*, vol. 1900, pp. 2-14, 1993.
- [11] M. White, D. Lampe, I. Blaha and I. Mack, "Characterization of surface channel CCD image arrays at low light levels," *IEEE J. Solid-State Circuits*, vol. 9, pp. 1-13 (1974).