Applied Vertical Bloch Line (VBL) Storage Technology

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Presentation Overview

Technology description review:
Functional goals.
Performance ranges.
  ∨ ∃ L operability review.
VBL Technology
Functional Performance

Increase reliability:
Overcome mechanical and environmental limitations.
Combine nonvolatility and solid-state recorder advantages.

Increase storage capacity and performance:
Buffer greater quantities of science and engineering data.
Support onboard computation and processing.
Simplify data management.
Provide component with high modularity and storage granularity.
Increase data transfer rates.
Provide block access to data.
Reduce data access times.

Minimize consumption of precious resources:
Mass, Volume, and Power.
VBL Technology Advantages

VBL technology is the only known storage technology that could fill all of the following requirements simultaneously:

Advantages addressed in proposed development plan:
- Potential near term availability.
- High areal storage density.
- High chip storage capacities.
- High data rate capability.
- Data rate flexibility.
- Low mass, volume, and power consumption.
- Solid-state storage.
- Nonvolatile storage.

Advantages currently considered inherent to VBL technology:
- Radiation hard (SEU and total dose).
- High system capacities.
- High modularity for flexible system design.
- 3D packaging capability for high volumetric storage density.
VBL Applications

Provide compact, high-performance, nonvolatile, solid-state storage for:

Space applications:
- Microspacecraft.
- Microrovers.
- Planetary spacecraft.
- Earth-orbiting spacecraft.
- Mass storage.
- Embedded subsystem and instrument local storage.
- Distributed multiprocessing and onboard parallel processing.

High-volume commercial applications:
- Solid-state disks.
- Laptop and palmtop computer storage.
- Node storage for multiprocessors and supercomputers.
A VBL Memory Architecture

Garnet Grooving for Stripe Stabilization
Z-Bit Periodic Storage Cc//
Sample VBL bit Positions
Hard Magnetic Films for Bit Stabilization

Left Data In
Major Line (I/O)

R/W

Minor Loops

Stripes

Right Major Line (1/0)

Data In

R/W

Output detector

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VBL Storage Device Cross-Section

Wire bonding/mount on chip carrier

Passivation
500 nm Metal-4
100 nm Permalloy (Ni80Fe20)
500 nm Metal-3
500 nm Metal-2
500 nm Metal-1
500 nm Metal-1
500 nm Metal-1
500 nm Metal-1

2µm Epitaxial magnetic garnet film
(YBiGdHoCa)3(FeGeSi)5O12

500 nm groove planarized
200 nm groove planarized
100 nm ion implantation (unetched)

Substrate: GGG (Gadolinium Gallium Garnet)
Gd3Ga5O12

Grooves are formed through ion implantation and wet etching.
Ion implantation conditions, 1st groove: Ne+, 300 keV, 10^15 ions/cm².
Ion implantation conditions, 2nd groove: Ne+, 150 keV, 10^15 ions/cm².
Ion implantation conditions, hard-bubble suppression layer: 80 keV, 10^15 ions/cm².

Grooves and deposited layers should be planarized.

Layer period is approximately 1µm.

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VBL Storage Chips: Areal Storage Density Performance

<table>
<thead>
<tr>
<th>Lf = 1 μm</th>
<th>Lf = 0.5 μm</th>
<th>Lf = 0.1 μm</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sw = 5 μm</td>
<td>10 Mbits/cm²</td>
<td>20 Mbits/cm²</td>
</tr>
<tr>
<td>Sw = 2 μm</td>
<td>25 Mbits/cm²</td>
<td>50 Mbits/cm²</td>
</tr>
<tr>
<td>Sw = 1 μm</td>
<td>50 Mbits/cm²</td>
<td>100 Mbits/cm²</td>
</tr>
<tr>
<td>Sw = 0.5 μm</td>
<td>100 Mbits/cm²</td>
<td>200 Mbits/cm²</td>
</tr>
<tr>
<td>Sw = 0.25 μm</td>
<td>200 Mbits/cm²</td>
<td>400 Mbits/cm²</td>
</tr>
</tbody>
</table>

VBL Memory storage density is proportional to:
\[
\frac{0.5}{(Sw) \times (Lf)}
\]

Stripe:

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## VBL Storage Chips: Volumetric Storage Performance

<table>
<thead>
<tr>
<th>Areal Storage Density</th>
<th>16 die/cm</th>
<th>40 die/cm</th>
<th>200 die/cm</th>
<th>400 die/cm</th>
</tr>
</thead>
<tbody>
<tr>
<td>25 Mbits/cm²</td>
<td>(25 roils/die)</td>
<td>(10 roils/die)</td>
<td>(2 roils/die)</td>
<td>(1 roil/die)</td>
</tr>
<tr>
<td>100 Mbits/cm²</td>
<td>(625 µm/die)</td>
<td>(250 urn/die)</td>
<td>(50 µm/die)</td>
<td>(25 urn/die)</td>
</tr>
<tr>
<td>200 Mbits/cm²</td>
<td>0.4 Gbits/cc</td>
<td>1 Gbit/cc</td>
<td>5 Gbits/cc</td>
<td>10 Gbits/cc</td>
</tr>
<tr>
<td>1,000 Mbits/cm²</td>
<td>1.6 Gbits/cc</td>
<td>4 Gbits/cc</td>
<td>20 Gbits/cc</td>
<td>40 Gbits/cc</td>
</tr>
<tr>
<td>10,000 Mbits/cm²</td>
<td>3.2 Gbits/cc</td>
<td>8 Gbits/cc</td>
<td>40 Gbits/cc</td>
<td>80 Gbits/cc</td>
</tr>
<tr>
<td>10,000 Mbits/cm²</td>
<td>16 Gbits/cc</td>
<td>40 Gbits/cc</td>
<td>200 Gbits/cc</td>
<td>400 Gbits/cc</td>
</tr>
<tr>
<td>10,000 Mbits/cm²</td>
<td>160 Gbits/cc</td>
<td>400 Gbits/cc</td>
<td>2,000 Gbits/cc</td>
<td>4,000 Gbits/cc</td>
</tr>
</tbody>
</table>

### 3D VBL Chip Stack

### Chip Die Period
VBL Technology
Near Term Development Goals

Solid-state, nonvolatile chips:
- 16 Mbits, 64 Mbits, and/or 256 Mbit chips.
- 2 Gbits per cubic centimeter in 3D packaging.
- 300 Gbits per kg in 3D packaging.

Data rates:
- 0 to >40 Mbit/sec per chip.
- >1 Gbit/sec per system.

Power consumption:
- 10 mW per Mbit/sec during input/output operations.
- 90 mW per active chip during bit propagation operations.

Space qualifiability.
VBL Technology
Longer Term Potential Goals

Solid-state, nonvolatile chips with capacities of:
1 Gbit, 4 Gbits, and greater, are possible.
2 Tbits per cubic centimeter in 3D packaging.
300 Tbits per kg in 3D packaging.

Data rates:
0 to >100 Mbit/sec per chip.
>1 Gbit/sec per system.

Power consumption:
<1 mW per Mbit/sec during input/output operations.
<10 mW per active chip during bit propagation operations.
Summary VBL Technology Goals

VBL goals: Improved storage chip performance over DRAMs at disk drive efficiency.

<table>
<thead>
<tr>
<th>256 Mbit (32 Mbyte) devices</th>
<th>VBL</th>
<th>DRAM</th>
<th>Disk</th>
</tr>
</thead>
<tbody>
<tr>
<td>Solid-state form factor</td>
<td>Yes</td>
<td>Yes</td>
<td>No</td>
</tr>
<tr>
<td>Nonmechanical</td>
<td>Yes</td>
<td>Yes</td>
<td>No</td>
</tr>
<tr>
<td>Nonvolatile</td>
<td>Yes</td>
<td>No</td>
<td>Yes</td>
</tr>
<tr>
<td>Radiation hard medium</td>
<td>Yes</td>
<td>No</td>
<td>Yes</td>
</tr>
<tr>
<td>Reduced cost per bit</td>
<td>Yes</td>
<td>No</td>
<td>Yes</td>
</tr>
</tbody>
</table>
Test Device Processing

Phase 2: Test Devices including:
- Two ion implantation steps (with planarization).
- Three metallization steps.
- Two magnetic metal steps.

Test structures provide information on:
- Multimask fabrication in advance of full prototype fabrication.
- Design of full prototype chip (including bias field matching).
- Writing process.
- Read process.
- Bit Propagation.

Test structures will be selected initially from existing design sets.
Phase 3: Full prototype devices including:
Three ion implantation steps (with planarization).
Four metalization steps.
Two magnetic metal steps.

Verify full chip operation on prototype chips.
Include test chips and process verification chips.
Attempt fabrication of a 16 Mbit chip, to assess technical issues.

Prototype devices will be selected primarily from existing design sets.
VBL Testing and Experimentation

Improved electro-magneto-optic sampling microscope has been established to perform key VBL measurements:

- Hardware has been obtained through procurements and loan pool.
- Enhanced computer control with convenient interface.
- Improved image processing to perform quantitative VBL measurements.
- Improved laser operation, fiber-optics, mountings, and couplings.
- High output, fast rise-time electronics have been developed for test flexibility.
- Software programs for creating test chip and full chip test sequences are under development for margin testing.

Continuous illumination microscope is in place for complementary magnetic measurements.

Laboratory space is likely to support experimentation and simulation activities.
- VBL domain simulations will move from SUN SPARC 2GX platform to IBM-compatible 80486-based PC with doubling of throughput.
VBL Dynamics Research

Dr. Anne Bagneres, JPL visiting scientist, is continuing her interaction with JPL using the 512-node Caltech Intel Touchstone Delta:

- Demonstrated demagnetizing field calculation.
- Demonstrated improved demagnetizing field calculation.
- Working towards implementing entire micromagnetic VBL simulation on the Delta.

Contract to Boston University (BU) has been extended through May, 1993. Research at BU continues on the subjects of:

- Experimental VBL dynamics.
- Supercomputer simulations on the CM-5.
Dr. Anne Bagneres, JPL visiting scientist, is continuing her interaction with JPL using the 512-node Caltech Intel Touchstone Delta:


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CM-5 accessibility:

- Assessing access to JPL SAR project’s CM-5 in Bldg. 300.
- Assessing access to CM-5 at NASA Ames.
Conclusions

VBL storage technology offers many excellent data storage technology attributes.

VBL technology is multidisciplinary in nature and is best served through the involvement of many organizations.

VBL fabrication is proceeding under a phased plan to fabricate full prototype VBL chips by 2Q, FY'94.

VBL laboratory is being improved to perform precise measurements of VBL performance, to evaluate forthcoming VBL chips.
Supplemental Slides
VBL Chip Cost Competitiveness

Assume $5 K/wafer (processing + wafers+ material) (Overestimate)
Assume 50 chips are yielded per wafer (Underestimate)
Therefore chip cost is $1 00/chip.
For a 256 Mbit chip (32 Mbyte), cost is $3/Mbyte.

VBL bit costs are thus less costly than DRAM bit costs by an order of magnitude.

VBL bit costs are therefore comparable to magnetic disk drive bit costs.

VBL capitalization is estimated at $10M, which is less than $1 OOM for a DRAM line.

It is noted that VBL devices have implants, deposition, and lithography, but, unlike DRAMs (and SRAMs) have no diffusions and very few contacts.

VBL devices are therefore much simpler to process than DRAMs.

VBL technology offers very desirable price/performance ratios.
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