

## A Parallel Viterbi Decoder for Shared Memory Multiprocessor Architectures

The efficient implementation of the Viterbi Algorithm for a shared memory multiprocessing environment is examined. In particular, a simple method of partitioning the state metrics across  $N$  processors is suggested for architectures in which all processors are penalized equally for communication with any other processor. The suggested partitioning is shown to result in a concise, efficient update procedure for the state metrics requiring little communication between processors other than periodic barrier synchronization and exchange of pointers to starting regions on which to operate. If the state metrics are integer valued, the implementation does not require periodic renormalization of the metrics. For the particular application of the Viterbi algorithm to telemetry decoding with a large number of states ( $2^{13}$ ) and a small number of processors, the suggested state partitioning and update procedure is analyzed for performance and scalability. Specific timing results for one, two, and four processors are offered.

Richard H. Chauvin

Jet Propulsion Laboratory, Pasadena, CA

Kar-Ming Cheung

JPL Propulsion Laboratory, Pasadena, CA