CMOS ACTIVE PIXEL IMAGE SENSOR

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ABSTRACT

A new CMOS active pixel image sensor is reported. The sensor uses a 2.0 μm double-poly, double-metal foundry CMOS process and is realized as a 28 x 28 array of 40 μm x 40 μm pixels. The sensor features TTL compatible voltages, low noise and large dynamic range, and will be useful in machine vision and smart sensor applications.

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1. INTRODUCTION

Charge-coupled devices (CCDs) are typically employed for image acquisition. While offering high performance, CCDs are difficult to integrate with CMOS, complicating the integration of on-chip drive and signal processing electronics. Some achievement in on-chip signal processing with CCDs has been reported but a fully CMOS-compatible sensor technology enabling a higher level of integration would greatly benefit many applications. Simple p-n junction photodiode arrays have been fabricated using CMOS processes but typically have high read noise and suffer from image lag. Both bipolar and charge modulation device image sensors are compatible with CMOS integration, but require specialized fabrication processes. In this paper, a new, 100% CMOS-compatible image sensor with good performance is reported.

II. ACTIVE PIXEL SENSOR DESIGN AND OPERATION

The CMOS active pixel sensor is shown schematically in Fig. 1. For discussing the operation of the image sensor, it is assumed that the sensor is operated with voltage rails of 0 and +5 volts, though higher and lower voltage operation is possible and has been demonstrated. Operation of the sensor is as follows. During signal integration, the pixel photogate (PG) is biased at +5 volts, the transfer gate TX is biased at ±2.5 volts, and the reset transistor R and selection transistor S are both biased off (0 volts). Following integration, all pixels in the row to be read are read out simultaneously onto column lines by the following process. First, the pixels are addressed by the row selection transistor S biased at ±5 volts. This activates the source-follower output transistor in each pixel (the load transistor is located at the bottom of the pixel column and is biased at ±2.5 volts). The reset gate R is then briefly pulsed to ±5 volts to reset the floating diffusion output node to approximately ±3.5 volts. The output of the source-follower is then sampled onto a holding capacitor at the bottom of the column. The photogate PG is then pulsed low to 0 volts (with TX held at ±2.5 volts) to transfer the integrated signal charge under the photogate to the floating diffusion output node. The new source-follower output voltage is sampled onto a second holding capacitor at the bottom of the column. Storing the reset level and the signal level on separate capacitors permits correlated double sampling of the pixel, eliminating kT/C noise from the pixel, and suppressing 1/f noise and fixed pattern noise from the output transistor. In this circuit, the major source of readout noise is the kT/C noise introduced by the sample/hold capacitors, since kT/C noise from the pixel is suppressed by the differential output technique. The r.m.s. noise on these source follower capacitors is estimated to be 64 μV per capacitor, or 91 μV in differential mode.

All transistor were sized in anticipation of a 128x128 array size readout at the rate of 30 Hz, corresponding to a row readout time of 260 μsec/row. The total time to capture the row signal, in parallel, to the bank of capacitors at the bottom of each column was designed to be 0.7 μsec. The capacitors are sequentially scanned for serial readout.

The APS was designed using highly conservative 2 μm CMOS design rules and practices. The array was sized at 28 x 28 to fit within a standard 2 mm MOS/Si chip.
factor of the 40 \mu m \times 40 \mu m pixel, as measured by the ratio of active area (by design) to the total pixel area, is 26\%/0. Use of less conservative 2 \mu m design rules and practices could likely increase the fill-factor of the pixel to 350%. 

The row and column selection 5-to-32 decoders were implemented using a standard 5-input NAND gate designed to fit in the 40 \mu m pixel pitch. The PG and R pulses were gated with the row selection. The reset and signal channels for each column were laid out to be as symmetric as possible to ensure good common-mode rejection and differential output. The digital decoder was designed to be highly isolated from the column-wise analog circuitry. A light shield surrounding the imaging area was made using second level metal. A photograph of the completed sensor is shown in Fig. 2.

111. Experimental Results

The image sensors were driven in accordance to the timing and voltage levels described above. A sample image is shown in Fig. 3. Using an electrical test circuit on a separate IC, output conversion was determined to be 4.0 pV/electron. Saturation was measured to be 600 mV, or 150,000 electrons. The saturation level was determined by the output amplifier rather than well capacity since the 2.5 volt well capacity was estimated to be approximately 6x1 0^6 electrons for this surface-channel device. No lag was observed. The design of the CMOS APS reset transistor results in a lateral anti-blooming drain so that blooming is suppressed, Using the measured conversion gain, r.m.s. noise was estimated to be 23 electrons yielding a dynamic range of 76 dB. The fixed pattern noise (FPN) was approximately 1.5\%/0 p-p of the saturation level. It is believed that this can be reduced in future designs. Dark current was found to be well-behaved and measured to be approximately 2-3 nA/cm^2 at ambient temperature, though several non-saturating dark current spikes were observed.

IV. Conclusion

The first 100% CMOS active pixel image sensor has been demonstrated. The high performance obtained using standard foundry CMOS has encouraged us to pursue the fabrication of a 128 x 128 CMOS APS in the near future. A reduction in noise of more than a factor of 2, an increase in fill-factor to 35\%, and reduction in FPN to below 0.5\% p-p is believed to be readily feasible in later generations. The use of 0.8 \mu m design rules could yield a 15 \mu m \times 15 \mu m pixel size. Coupled with a microlens technology, the effective aperture could reach 65\%/0 or more. This initial work paves the way for more complex pixel structures and on-chip electronics for robot vision, guidance and navigation, and other smart sensor applications.

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VI. REFERENCES


VII. FIGURE CAPTIONS

Fig. 1. Schematic illustration of image sensor circuit. Dotted line shows boundary of in-pixel circuits. Remainder of circuit is at bottom of column.

Fig. 2. Photograph of fabricated CMOS APS array.

Fig. 3. Photograph taken from display of 28x28 image of George Washington taken from US $1 bill.
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