Power Optimization in Logic Isomers

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Abstract

Logic isomers are different realizations of a logic function which have the same number of transistors but have non-isomorphic graphs when the graphs are labeled with respect to the inputs. Logic isomers may have significantly different power requirements depending on the activity of the input signals even though they have the same number of transistors. A heuristic measure of signal activity can lead to significant optimizations in power-driven logic design as shown by several examples presented in the paper.

Summary

The thrust towards lower power in VLSI is motivated by the dual considerations of cooling 3D silicon and providing an extended operating life on battery power. While most of the research on low power has focused on low voltage technology, there has not been much research done in power-driven logic design. This paper presents some new techniques for power optimization in logic design. We first develop the concept of logic isomers which are different realizations of a logic function which have the same number of transistors but have non-isomorphic graphs when the graphs are labeled with respect to the inputs. Thus, for example, a two input NAND gate has two isomers depending on how the signals are assigned to the series transistors in the n-logic block. We show that even though the two inputs to the NAND gate are functionally equivalent, the inputs are not equivalent from a consideration of the power requirements for input switching. We show that even simple functions like a 1-bit full-adder can have very large isomeric cardinality (the total number of logic isomers) with significant differences in the power requirements of various isomers. The power requirements of the isomers depend on the behavior of the input signals which is formalized in the concept of signal activity. The signal activity is a measure of the transition frequency of the signal. We develop the notion of signal level which allows the logic designer (or logic synthesis tool) to obtain a heuristic measure of signal activity. We then show how this knowledge can be used to optimize the logic design for power by the use of two rules of thumb. We present several examples to show the relationship between signal level and signal activity and the different power requirements of the logic isomers for each example. The examples include a 16 bit carry lookahead adder, a 16-bit ripple-carry adder, and several randomly synthesized logic designs.