

**EXPERIMENTAL EVALUATION AND THEORETICAL ANALYSIS OF
BACK-TO-BACK BARRIER-N-N⁺ (bbBNN) VARACTOR FREQUENCY
MULTIPLIERS FOR MILLIMETER AND SUBMILLIMETER WAVE
APPLICATIONS**

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ABSTRACT

This paper describes the performance of planar back-to-back Barrier-N-N⁺ (bbBNN) devices for millimeter and submillimeter wave multiplier applications. A technique has been developed for characterizing planar bbBNN devices using a network analyzer, which gives both the series resistance and voltage dependent capacitance of the device. A large signal analysis approach has been used to calculate the multiplication efficiency of bbBNN devices. The embedding impedance requirements for these devices has also been analyzed. Results indicate that a small device and high C_{\max}/C_{\min} value is essential for high efficiency. So far, a tripling efficiency of 3.3% has been achieved using these devices in a 200 GHz crossed waveguide

mount. This is the first experimental result with a bbBNN waveguide frequency multiplier.

INTRODUCTION

The submillimeter-wave range of the spectrum holds enormous promise for spectral line studies of the interstellar medium, distant galaxies, solar system and earth remote sensing. To achieve high sensitivity and spectral resolution requirements of the submillimeter wave space missions, the baseline focal plane instrument includes heterodyne radiometers. In a heterodyne radiometer, a remote signal is downconverted to a much lower frequency by mixing with a local oscillator (LO) signal in a nonlinear device. Emphasis is placed on using technologies which are space qualifiable. The current approach is to use a solid state mm- wave Gunn oscillator driving a chain of frequency multipliers to generate the desired frequency.

One of the primary causes of failure in mm- and submm- wave mixers and multipliers is the whisker contact of the device. Thus, planar varactor devices are being developed to replace whisker contacted devices in order to improve the performance and ruggedness of spaceborne submillimeter wave heterodyne receivers [1]. One candidate is the planar back-to-back Barrier-N-N⁺ (bbBNN) varactor device. It exhibits a very sharp change in its capacitance versus voltage characteristic, resulting in very efficient harmonic generation at small input power levels. The bbBNN device has symmetric C-V and anti-symmetric I-V characteristics. Impedance nonlinearities symmetric to zero bias will generate only odd harmonics, thereby greatly simplifying the mount design. For instance, a tripler mount for a symmetric device will be similar in complexity to a doubler mount for a device without symmetry. Likewise, a quintupler mount will be similar to a traditional tripler mount, both requiring only one idler. It is expected that,

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bbBNN devices can be made to operate efficiently at frequencies over 1 THz [2-6]. Lower leakage current in these devices provides an advantage over the conventional Schottky devices.

DEVICE DESCRIPTION

A conceptual diagram of the device is shown in Fig.1. The semiconductor consists of several layers; the barrier, a sheet doping layer, a moderately doped layer and a highly doped region [5,6]. The layer thicknesses and compositions can be adjusted for optimum performance. When a forward bias is applied, charge supplied by the sheet doping layer accumulates under the barrier, resulting in the maximum capacitance of the device, determined by the barrier thickness. When reverse bias is applied, the charge is depleted to the heavily doped n^+ region and the capacitance is minimum, determined by the barrier and the moderately doped region thickness. The structure from the top surface down is, (i) an AlGaAs layer that is sufficiently thick to preclude tunneling but sufficiently thin to allow large capacitance per unit area, (ii) a highly doped (delta doped) region which introduces a built-in potential to ensure that the high capacitance mentioned above is achieved at zero voltage, (iii) a moderately doped GaAs drift/varactor region in which all of the doping can be depleted with little parasitic conduction to the metal contact pads, and (iv) a highly doped region that provides a low resistance path between the two metal contact pads.

bbBNN VARACTOR CHARACTERIZATION

The GaAs based bbBNN devices presented in this paper use the following layer

thicknesses and doping levels from top surface down: (i) 15 nm thick $\text{Al}_{0.45}\text{Ga}_{0.55}\text{As}$ barrier, (ii) 3 nm thick nominally undoped layer on top of $4 \times 10^{12} \text{ cm}^{-2}$ silicon planar doping, (iii) 125 nm thick GaAs layer with $1 \times 10^{17} \text{ cm}^{-3}$ doping level, (iv) 900 nm thick highly doped GaAs layer (doping level = $5 \times 10^{18} \text{ cm}^{-3}$), (v) 600 nm thick $\text{Al}_{0.45}\text{Ga}_{0.55}\text{As}$ etch stop layer, and (vi) a 508 μm thick GaAs substrate. The device fabrication technique is described in detail in [5].

Devices were first characterized by measuring the current/voltage (I-V) and capacitance/voltage (C-V) characteristics at 1 MHz. Fig.2(a) shows the capacitance of a $2 \mu\text{m} \times 4 \mu\text{m}$ device. Fig.2(b) shows the DC leakage current, which is many orders of magnitude lower than that for the conventional Schottky diodes. The series resistance of the device cannot be determined in the conventional way from the DC I-V curve. However, the remaining series resistance of some of the bbBNN devices were measured by shorting the device with an electric shock. With this technique, a DC resistance for several bbBNN devices was found to be between 7-14 Ω . This technique damages the device permanently and does not necessarily give the correct series resistance of an operating diode.

In order to more accurately determine the series resistance, a special mount was designed for mounting the planar bbBNN devices to perform S-parameter measurements with a HP 8510C network analyzer. Measurements were done from 1-20 GHz with 10 dBm source level and 20 dB port attenuation. The bias voltage was varied from -3.0 V to +3.0 V. S11 of the device was measured at different bias voltages. The results were fitted with a linear equivalent circuit model using HP Microwave Design System (MDS) software. This technique gives both the series resistance and the voltage dependent capacitance of the device. Fig.3(a) shows a schematic diagram of the device mounted in a test mount (see also [7]). Fig.3(b) illustrates the equivalent circuit of the bbBNN varactor in the test mount. Series resistance values of 11-14 Ω were

measured using this technique for various devices having maximum capacitance of 25-60 fF.

PHYSICAL DEVICE MODELING

The physical device simulations were performed using a number of simplifying assumptions. First, the depletion approximation was used. More importantly, the two-dimensionality inherent to the back-to-back varactor design was included only by using a resistance to represent the n^+ region. These assumptions result in a larger ratio of maximum capacitance (C_{max}) to minimum capacitance (C_{min}) than would be observed in real varactors.

Cut-off frequencies and breakdown voltages were also approximated. The cut-off frequency associated with the RC time constant of the device was determined by the formula

$$f_{c-RC} = \frac{1}{2\pi R_s} \left(\frac{1}{C_{min}} - \frac{1}{C_{max}} \right), \quad (1)$$

where R_s is the resistance modeled at zero bias, i.e., the resistance associated with twice the drift region thickness, the metal connection and the n^+ region. The cut-off frequency associated with the maximum velocity of the electrons (f_{c-vsat}) was determined by assuming that the input power is exactly sufficient to completely deplete the drift region and calculating when the electrons first start to lag that drive. The saturation velocity was assumed to be 3×10^5 m/s - this number is significantly higher than that commonly assumed for larger devices because of velocity overshoot effects. The breakdown voltage V_{bd} , modeled here is due to Fowler-Nordheim tunneling [6]. Avalanching is probably also important. Devices made in the laboratory have always shown lower breakdown voltages than the numbers here indicate, but results have been quite variable and are thought to be very sensitive to factors such as the presence of states near the surface.

Table-I shows characteristics for devices with 2 μm wide contacts across a 4 μm mesa and with a 2 μm separation between contacts. These devices (device area = 8 μm^2) are typical of those used in the 67 GHz to 200 GHz tripler. In Table-I(a) C_{max} was set constant by adjusting the barrier thickness x_b , and setting the planar doping n_s to a large enough value, so that the maximum capacitance could be reached at zero volt. From that starting point, C_{min} was varied, while holding the C-V width constant by varying the drift region thickness, x_d , and the doping density, N_d . In Table-I(b), x_b and x_d were calculated by setting C_{min} to be constant and varying $C_{\text{max}}/C_{\text{min}}$. n_s and N_d were set by keeping the voltages necessary to deplete the planar doping and the drift region, respectively, constant.

Table-II and Table-III are similar to Table-I, except that, the device areas are 4 μm^2 and 2 μm^2 respectively.

LARGE SIGNAL ANALYSIS

To achieve optimum performance of the device, it must be provided with the appropriate circuit embedding impedances. The impedances at the input and output frequencies must be set to maximize power coupling into and out of the device. The general circuit requirements are matched terminations at input and output frequencies, open circuited terminations at the higher harmonics and optimum reactive terminations at the idler frequencies.

A modified version of the nonlinear program by Siegel et. al [8], was used to calculate the multiplication efficiency of the bbBNN devices. This analysis also optimized embedding impedance values. Since the series resistance is important in evaluating the device performance, simulations of a 67 GHz to 200 GHz tripler were carried out for a range of series

resistances. Measured C-V and I-V characteristics of a device with anode area of $8 \mu\text{m}^2$ (Fig.2) were used. Fig.4 presents efficiency versus input power plot for the tripler to 200 GHz with the series resistance of the device as a parameter. Theoretical efficiency is found to be high at low input power levels. Due to a very low leakage current, efficiency of the device does not degrade significantly when the measured I-V characteristic is included.

In order to isolate the device parameters important to optimizing efficiency, parameters representing a number of different devices were chosen in order to illustrate different trends and design strategies. The resulting device characteristics obtained from the physical model (Tables-I,II and III) were then used in the large signal analysis in order to determine the RF performance.

The effect of $C_{\text{max}}/C_{\text{min}}$ ratio on the device tripling and quintupling efficiency was analyzed. Fig.5(a) shows tripling efficiency versus input power plot for a tripler to 200 GHz, parameterized by the $C_{\text{max}}/C_{\text{min}}$ ratio. Here, C_{max} was assumed to be 30 fF (device area= $8 \mu\text{m}^2$), while C_{min} was changed. Fig.5(b) also shows efficiency versus input power with various $C_{\text{max}}/C_{\text{min}}$ ratios, but here C_{min} was assumed to be constant, equal to 7.5 fF. The highest $C_{\text{max}}/C_{\text{min}}$ ratio clearly yields the best efficiency. However, if the input power is limited to a few milliwatts in this case of a large device, a smaller $C_{\text{max}}/C_{\text{min}}$ gives optimum performance. Fig.6 presents similar results for a $4 \mu\text{m}^2$ area device, when C_{max} was kept constant. It shows that a smaller area diode gives better efficiency, which in the case of $C_{\text{max}}/C_{\text{min}} = 5$ is 70%, while for a $8 \mu\text{m}^2$ device with $C_{\text{max}}/C_{\text{min}}=5$, the maximum efficiency is only 53%. Figs. 7 and 8 illustrate simulation results for a tripler to 600 GHz and a quintupler to 1000 GHz, respectively, using a $2 \mu\text{m}^2$ device (C_{max} constant). Theoretical tripling efficiency of about 57% and quintupling efficiency of about 33% are calculated for the tripler to 600 GHz and the quintupler to 1 THz, respectively, at 10 mW

input power. Note that, $f_{c\text{-vsat}}$ is less than 1 THz for $C_{\text{max}}/C_{\text{min}}=5$ (Tables I-III) and therefore a capacitance ratio of 4 gives the maximum efficiency at 1 THz. Furthermore, similar simulations were carried out with a $4 \mu\text{m}^2$ device for a tripler to 200 GHz, keeping C_{min} constant and for a tripler to 600 GHz, keeping either C_{max} or C_{min} constant. Simulations were also carried out with a $2 \mu\text{m}^2$ device for a quintupler to 1 THz, keeping C_{min} constant.

From the above simulations, following conclusions can be drawn: If the input power is restricted to a very low level (say, below 5 mW), the optimum $C_{\text{max}}/C_{\text{min}}$ ratio is between 2 to 4, which is in good agreement with results in reference [9]. This is especially true if the diode area is too large (i.e. not optimum) for the given frequency. But if a higher input power (about 10 mW or more, which is readily available at frequencies below 100 GHz and which at least $8 \mu\text{m}^2$ and $4 \mu\text{m}^2$ devices can easily handle) is available, and the proper device size for the given frequency is used, the highest possible $C_{\text{max}}/C_{\text{min}}$ ratio gives maximum efficiency. This is in agreement with the "rule of thumb" stating that the highest cut-off frequency, $f_{c\text{-RC}}$, gives the highest multiplication efficiency. However, in the case of a quintupler to 1 THz, the maximum velocity of electrons sets a limit to the highest usable $C_{\text{max}}/C_{\text{min}}$ ratio. Highest efficiency would then be obtained with $C_{\text{max}}/C_{\text{min}}=4$.

EXPERIMENTAL TRIPLER PERFORMANCE

The embedding impedances were provided to the planar bbBNN device by a crossed waveguide mount. A schematic of the crossed waveguide block of the 200 GHz tripler mount is shown in Fig.9. The output waveguide in the mount is actually oriented perpendicular to the plane of the paper. The planar bbBNN device is mounted spanning the output waveguide

as shown in the diagram. The input waveguide is 0.148" X 0.074" and the output waveguide is 0.039" X 0.010". The input power is coupled to the varactor in the output waveguide through a suspended substrate low-pass filter on a 76 μm thick quartz substrate. The filter prevents the higher harmonic powers from propagating back to the input waveguide, and is a critical element in providing the proper embedding impedances to the varactor at the various harmonics. The output waveguide is cutoff at the fundamental and second harmonic frequencies. Sliding tuners in the input waveguide, in its E-plane arm and in the output waveguide as well as the proper design of the low pass filter, provide the possibility of partial optimization of the embedding impedances at the fundamental and third harmonic frequencies.

The performance of the assembled tripler was measured using the set-up described in reference [10]. Backshorts and E-plane tuners were adjusted for the best performance at each measurement frequency and pump power level. Fig.10 shows the measured flange-to-flange efficiency versus input power for the tripler at 188 GHz, using the bbBNN device whose C-V and I-V characteristics are shown in Fig.2. The flange-to-flange efficiency of the tripler reaches its maximum value of $3.3\% \pm 1.0\%$ at 6 mW input power, and then begins to decrease as the pump power level is increased.

In order to find out the embedding impedances available at the varactor terminals, a 20 times scale model of the crossed waveguide mount was constructed. The embedding impedances at the fundamental and higher harmonics were measured for various mount parameters with the HP 8510C vector network analyzer at 3-20 GHz. The end of a miniature coaxial cable (UT 34) was used as a probe to measure the impedances seen by the gap for the varactor diode. This technique is described in reference [11]. According to the measurements, this multiplier mount can provide a perfect impedance match at the fundamental frequency band of

60-70 GHz to any of our bbBNN devices. But, the behaviour of the third harmonic impedance at 180-210 GHz is less optimum. The output embedding impedance as a function of output backshort position circles around the desired impedance region (for the measured device) as shown in Fig.11. At frequencies above 200 GHz, there is a small leakage of the third harmonic signal back to the input waveguide. This is due to the suspended stripline quartz substrate of 635 μm width, which can support a parasitic waveguide mode in the filter channel.

The large signal analysis of the bbBNN device was also carried out for a tripler to 188 GHz using the available embedding impedances of the mount. The effect of the third harmonic embedding impedances on the tripler efficiency was studied for different available embedding impedance values obtained from scale model measurements (compare Fig.11). Fig.12 shows efficiency versus input power plots for the bbBNN tripler, with the third harmonic embedding impedance of the mount as parameter. The embedding impedance at the fifth harmonic was found to have insignificant effect on the tripler efficiency.

Based on the previous measurements of the mount (see reference [10]), losses in the input and output waveguides and the filter are about 45%. Hence, the measured efficiency at the diode is estimated to be about 6%. This is in excellent agreement with the calculations, taking into account the mismatch loss shown in Fig.12.

CONCLUSIONS

A flange-to-flange tripling efficiency of $3.3\% \pm 1.0\%$ has been obtained for planar bbBNN devices in a 200 GHz crossed waveguide mount, with the efficiency at the diode about 6% (output impedance mismatch loss is included). This is the first reported experimental result

with a bbBNN waveguide frequency multiplier. A new technique has been developed to characterize the C-V curve and series resistance of these planar devices using network analyzer. Measured device characteristics compare very well with those obtained using other techniques. bbBNN devices are found to have lower series resistance compared to BIN devices [12]. Highest possible C_{\max}/C_{\min} value is also desirable for these devices. However, the highest usable capacitance ratio at frequencies beyond 1 THz is limited by the maximum electron velocity. High efficiency at low input power levels makes these devices very attractive for submillimeter wave frequency multiplier applications.

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REFERENCES

- 1] W.L.Bishop, E.R.Meiburg, R.J.Mattauch and T.W.Crowe, 'A micron thickness planar Schottky chip for terahertz applications with theoretical minimum capacitance', 1990 IEEE MTT-

S International Microwave Symposium Digest, vol.III, pp.1305-1308.

2] T.J.Tolmunen and M.A.Frerking, 'Theoretical performance of novel multipliers at millimeter and submillimeter wavelengths', International Journal of Infrared and Millimeter Waves, vol.12, no.10, pp.1111-1133, 1991.

3] M.A.Frerking and J.R.East, 'Novel heterojunction varactors', Proceedings of IEEE, vol.80, no.11, pp.1853-1860, Nov.1992.

4] A.V.Räisänen, 'Frequency multipliers for millimeter and submillimeter wavelengths', Proceedings of IEEE, vol.80, no.11, pp.1842-1852, Nov.1992.

5] R.P.Smith, D.Choudhury, S.Martin, M.A.Frerking, J.K.Liu and F.A.Grunthaner, 'A new fabrication technique for back-to-back varactor diodes', Proceeding of Third International Symposium on Space Terahertz Technology, pp.158-163, March 24-26, 1992.

6] U.Lieneweg, T.J.Tolmunen.M.Frerking and J.Maserjian, 'Design of planar varactor frequency multiplier devices with blocking barriers', IEEE Trans. on Microwave Theory and Techniques, Special issue on Space Terahertz Technology, vol.40,no.5,pp.839-845, May 1992.

7] O.Boric,T.J.Tolmunen,E.Kollberg and M.A.Frerking, 'Anomalous capacitance of quantum well double-barrier diodes', International Journal of Infrared and Millimeter waves, vol.13, no.6, pp.799-814, 1992.

- 8] P.H.Siegel, A.R.Kerr and W.Huang, 'Topics in the optimization of millimeter wave mixers', NASA Tech. paper 2287, 1984.
- 9] H.Grönqvist, S.M.Nilsen, A.Rydberg and E.Kollberg, 'Character-izing highly efficient millimeter wave single barrier varactor multiplier diodes', Proceedings of the 22nd European Microwave Conference (Espoo, Finland), pp.479-484, August 1992.
- 10] D.Choudhury, M.A.Frerking and P.D.Batelaan, 'A 200 GHz single barrier varactor tripler', IEEE Trans. on Microwave Theory and Tech., Mini-Special issue on Space Terahertz Technology, 1993 (to be published).
- 11] A.V.Räisänen, W.R.McGrath, D.G.Crete and P.L Richards, 'Scaled model measurements of embedding impedances for SIS waveguide mixers', International Journal of Infrared and Millimeter Waves, vol.6, no.12, pp.1169-1189, 1985.
- 12] R.J. Hwu and L.P. Sadwick, 'Limitations of the back-to-back barrier-intrinsic-n⁺ (BIN) diode frequency tripler', IEEE Trans. on Electron Devices, vol.39, no.8, pp.1805-1810, August 1992.

FIGURE CAPTIONS

1. Schematic diagram of a back-to-back BNN varactor.
2. Measured (a) C-V and (b) I-V characteristics of a $8 \mu\text{m}^2$ bbBNN varactor diode.
3. (a) Schematic diagram of the planar bbBNN device in a test mount without the top cover.
(b) Equivalent circuit of the device in the test mount.
4. Calculated tripling efficiency at 200 GHz for bbBNN varactor with series resistance of the device as a parameter.
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8. Quintupling efficiency versus input power plot for 200 GHz to 1000 GHz quintupler parameterized by $C_{\text{max}}/C_{\text{min}}$ (device area= $2 \mu\text{m}^2$, Table-III), $C_{\text{max}}=7.5$ fF, variation of C_{min} .
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Table II Physical bbBNN device modeling,
device area= $4\mu\text{m}^2$.

Table III Physical bbBNN device modeling,
device area= $2\mu\text{m}^2$.

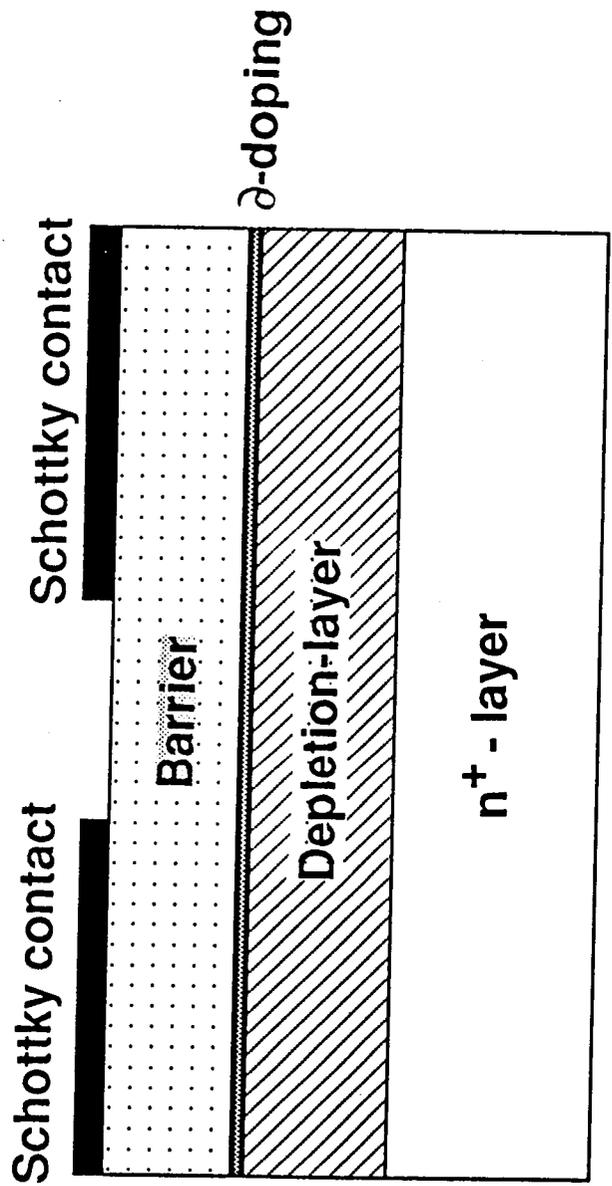
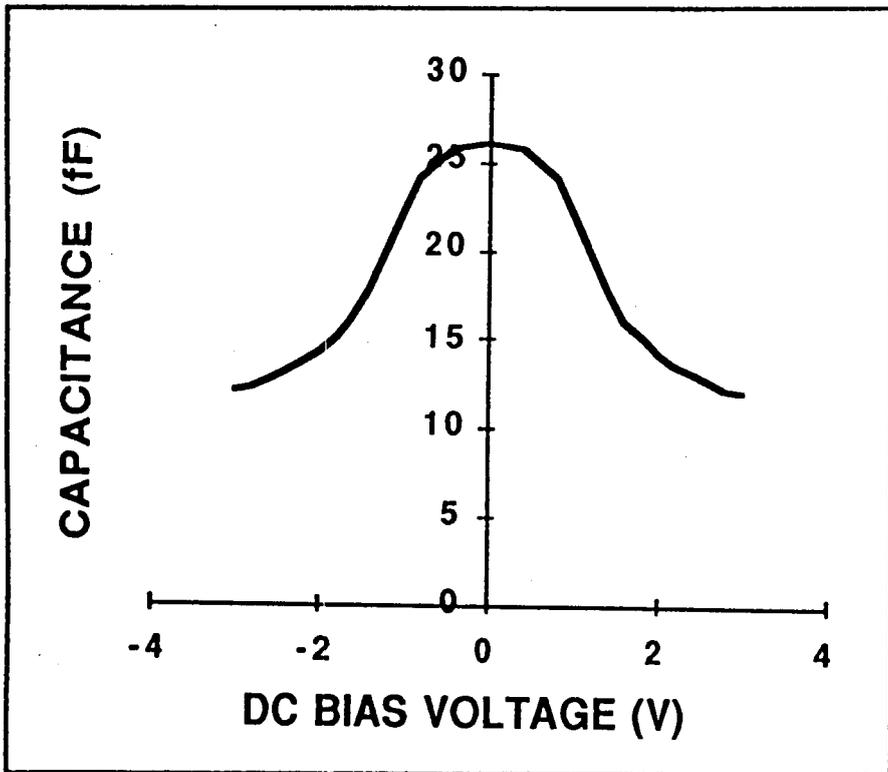
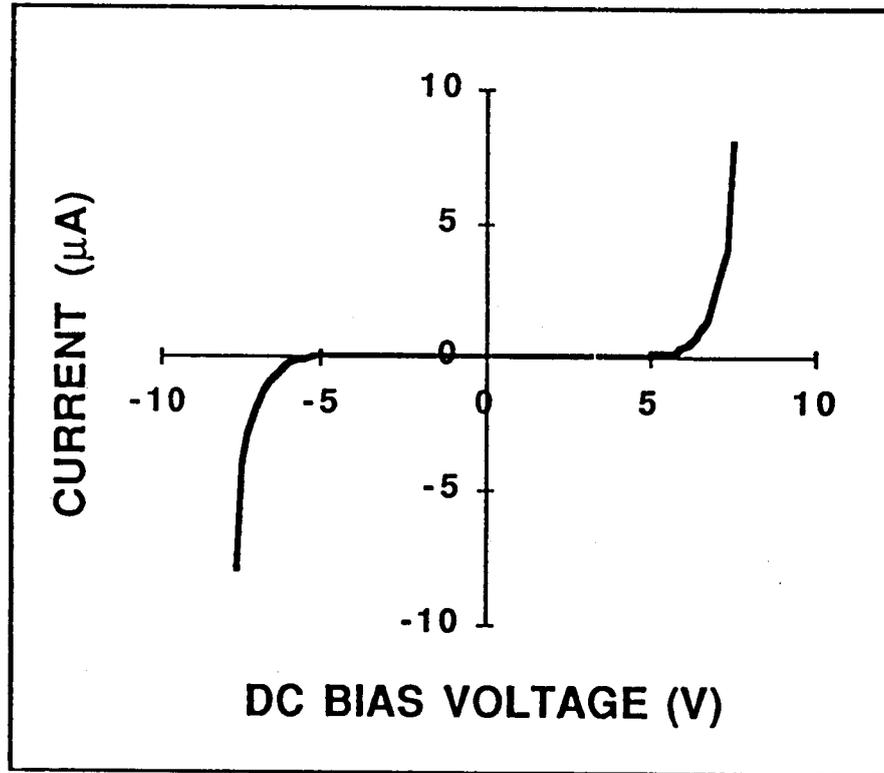


Fig. 1

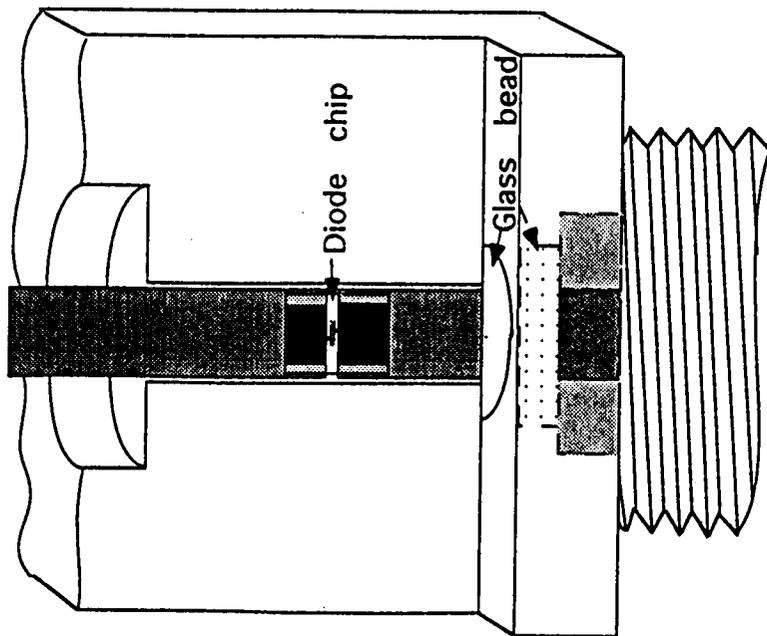


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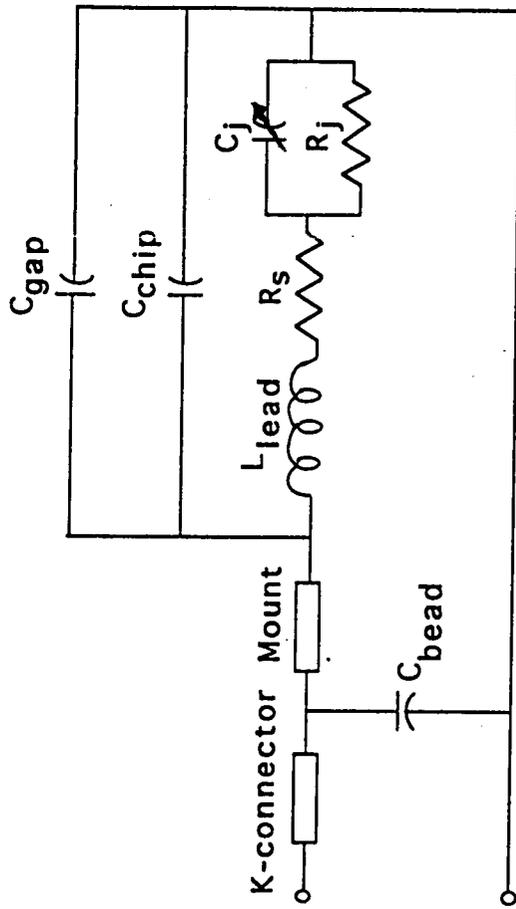


(b)

Fig. 2



(a)



(b)

Fig. 3

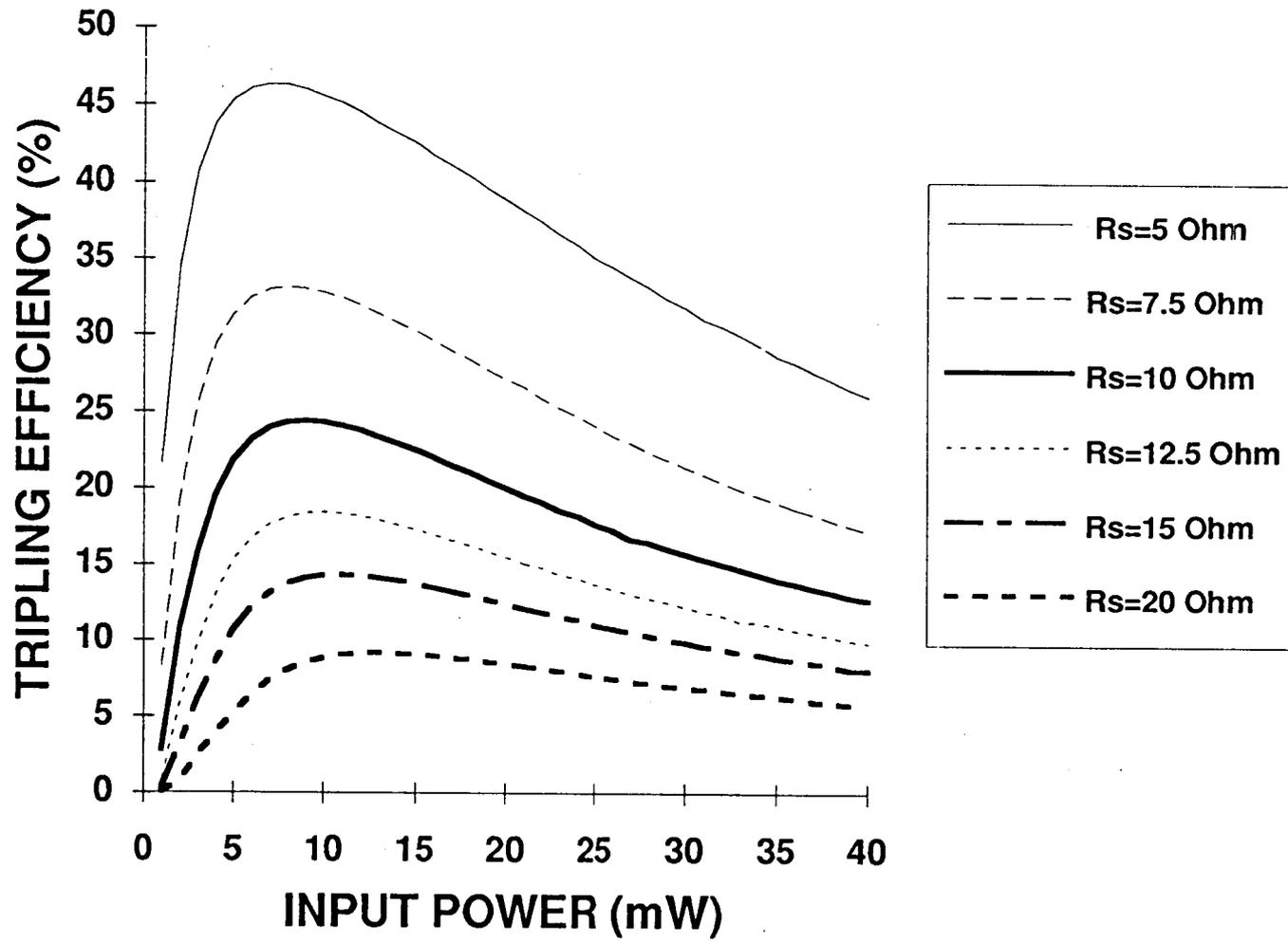


Fig. 4

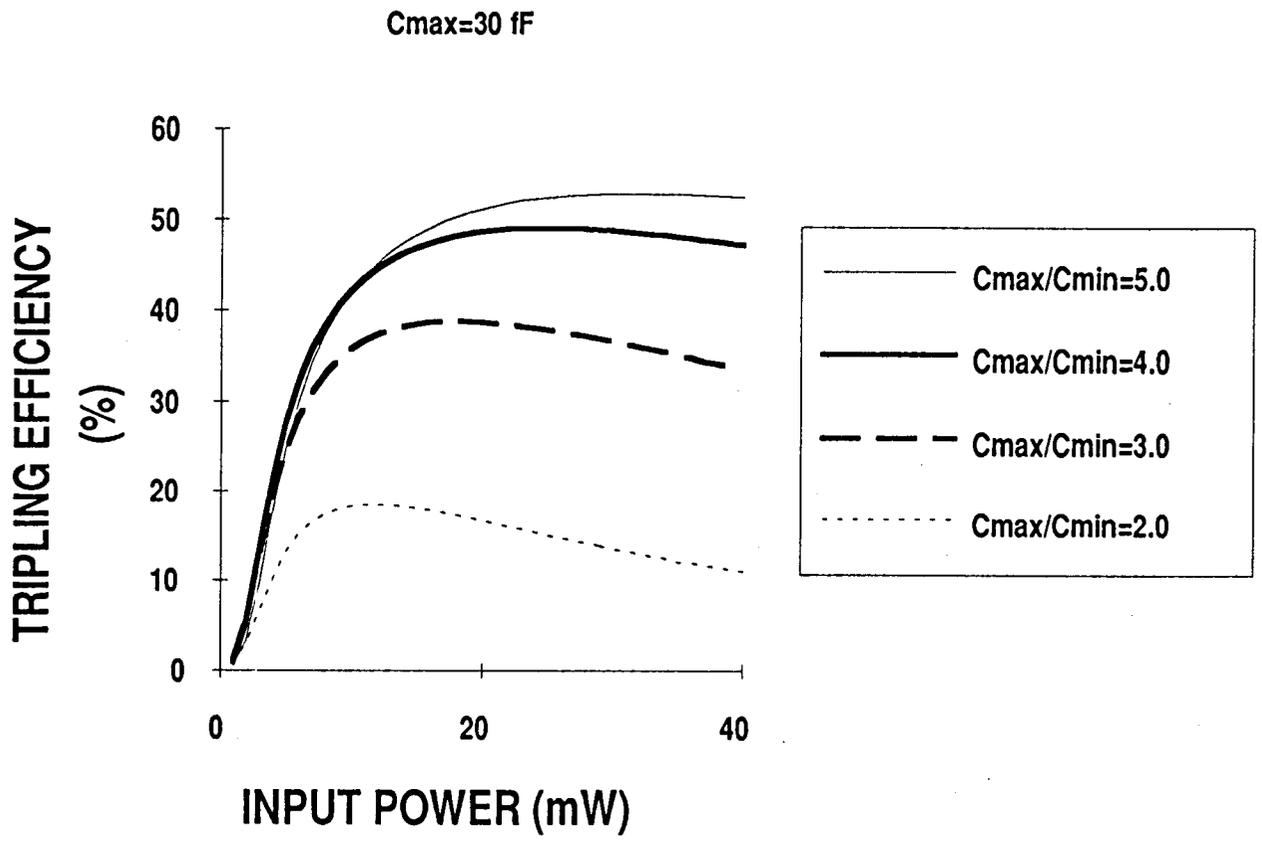


Fig 5(a)

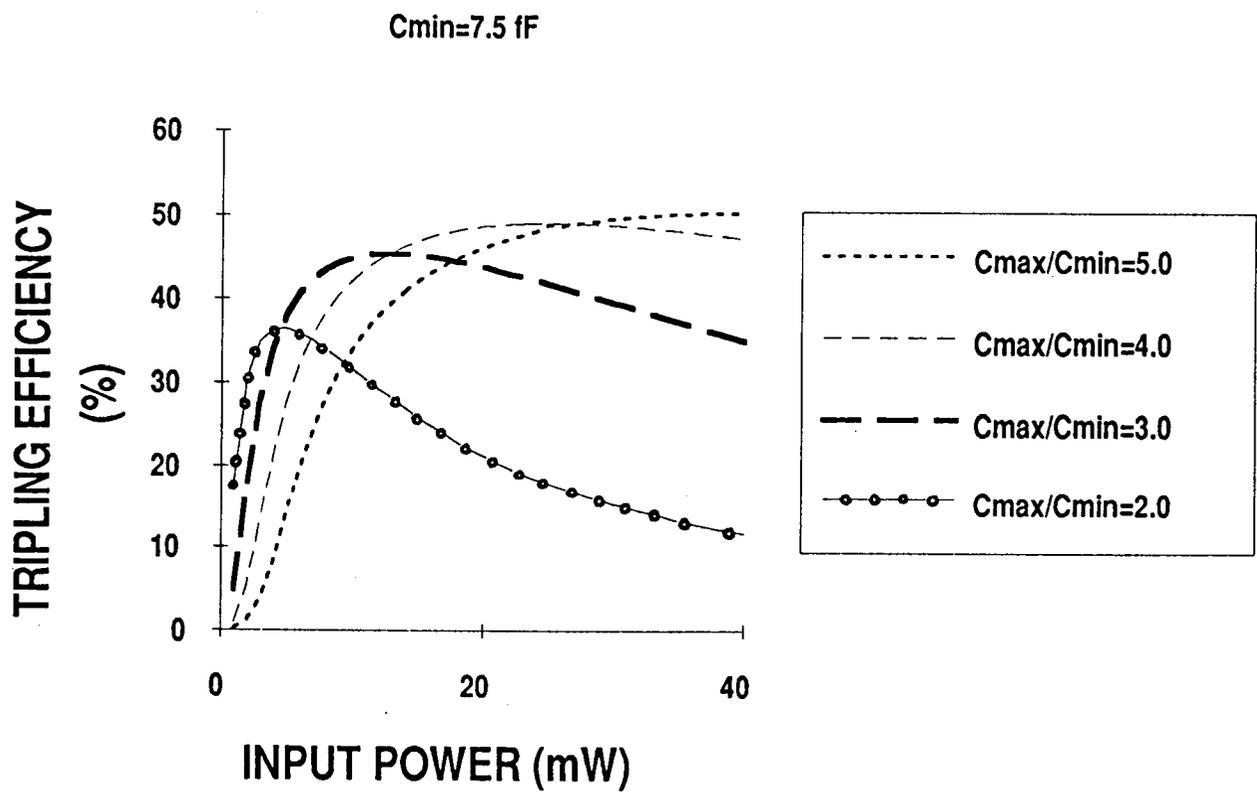


Fig. 5(b)

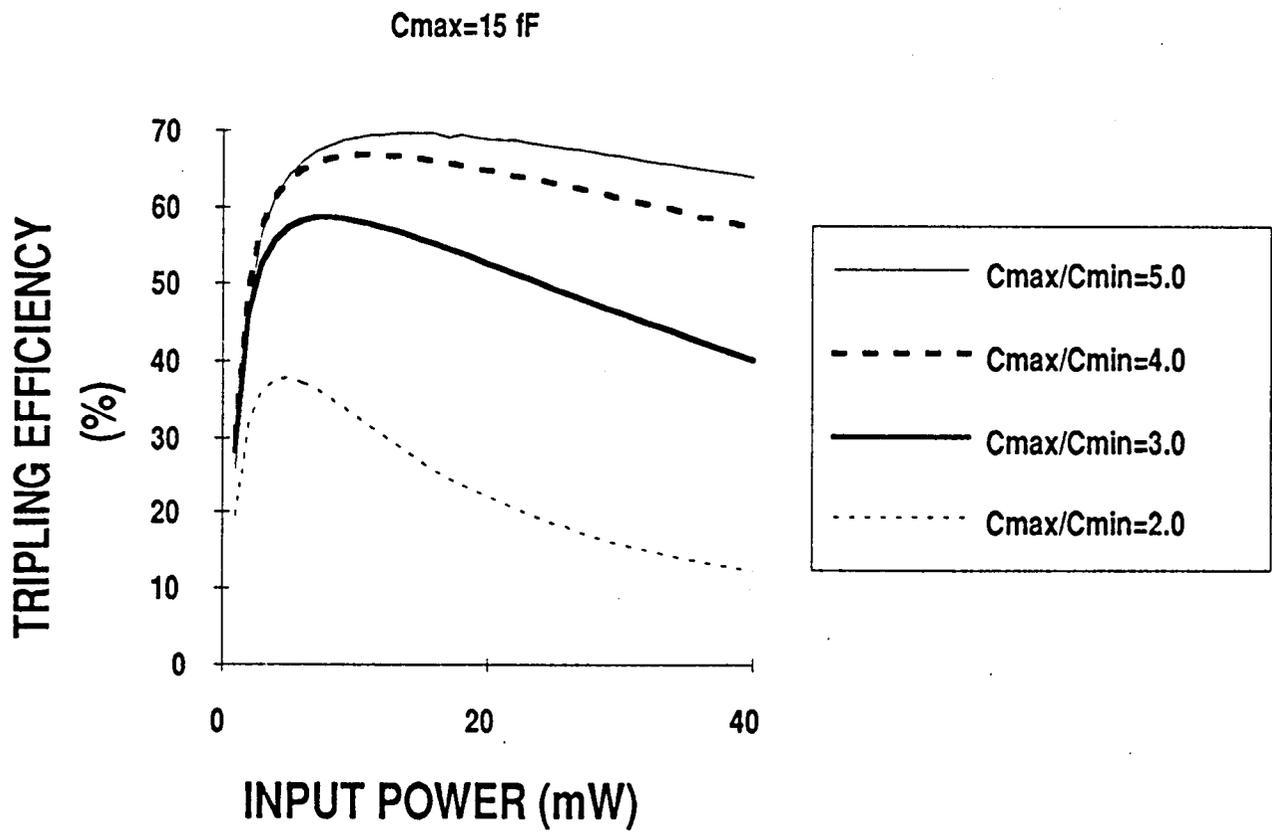


Fig. 6

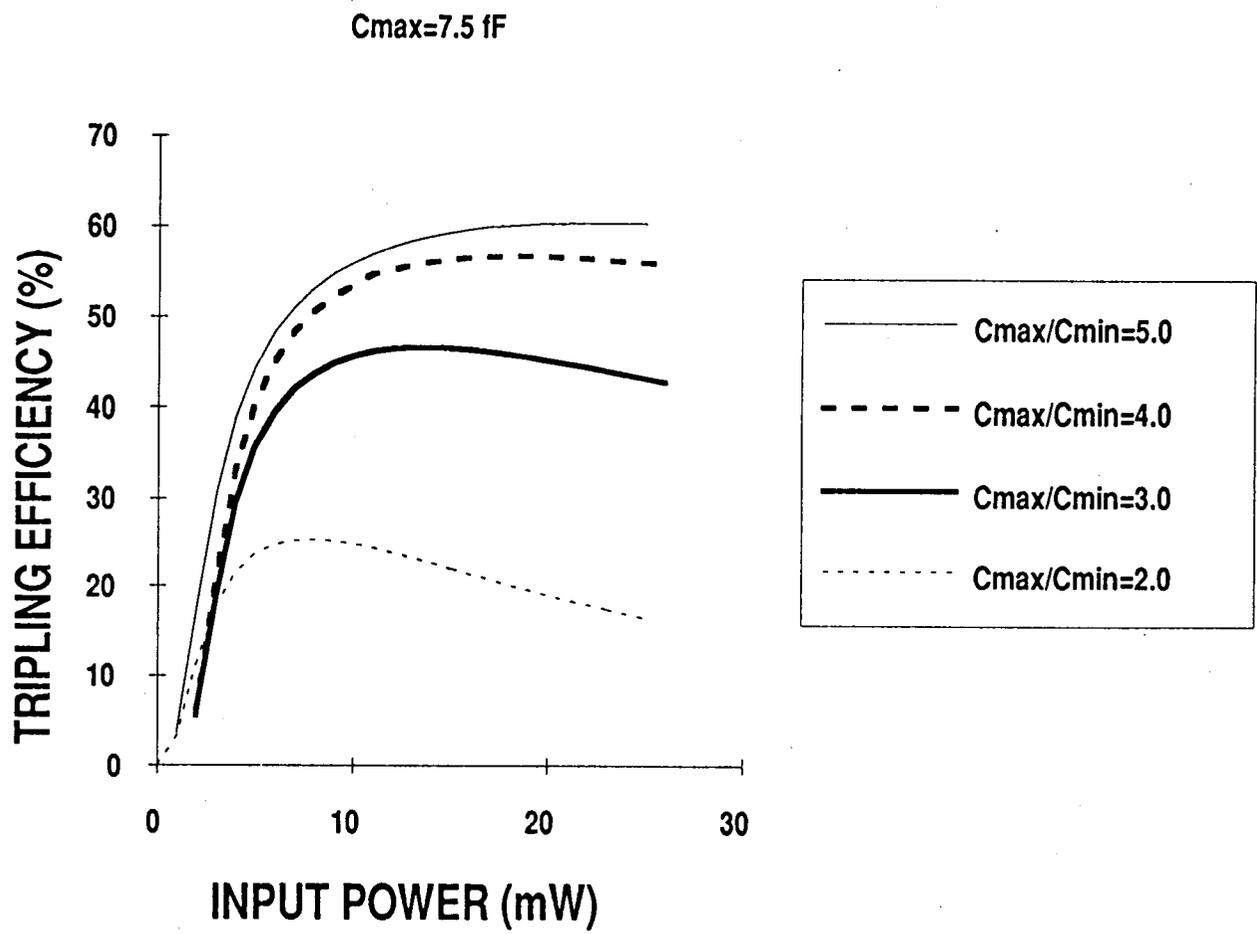


Fig-7

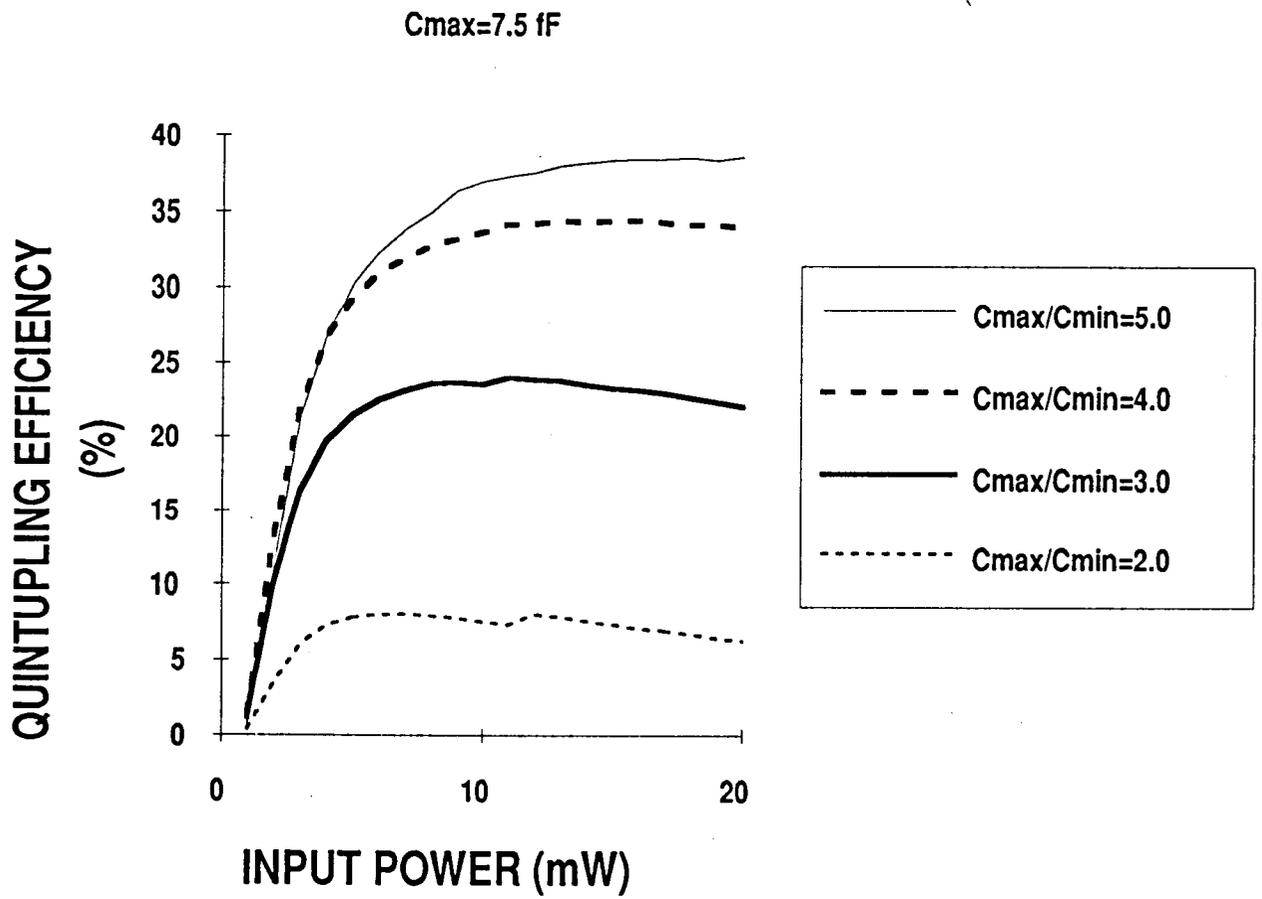


Fig. 8

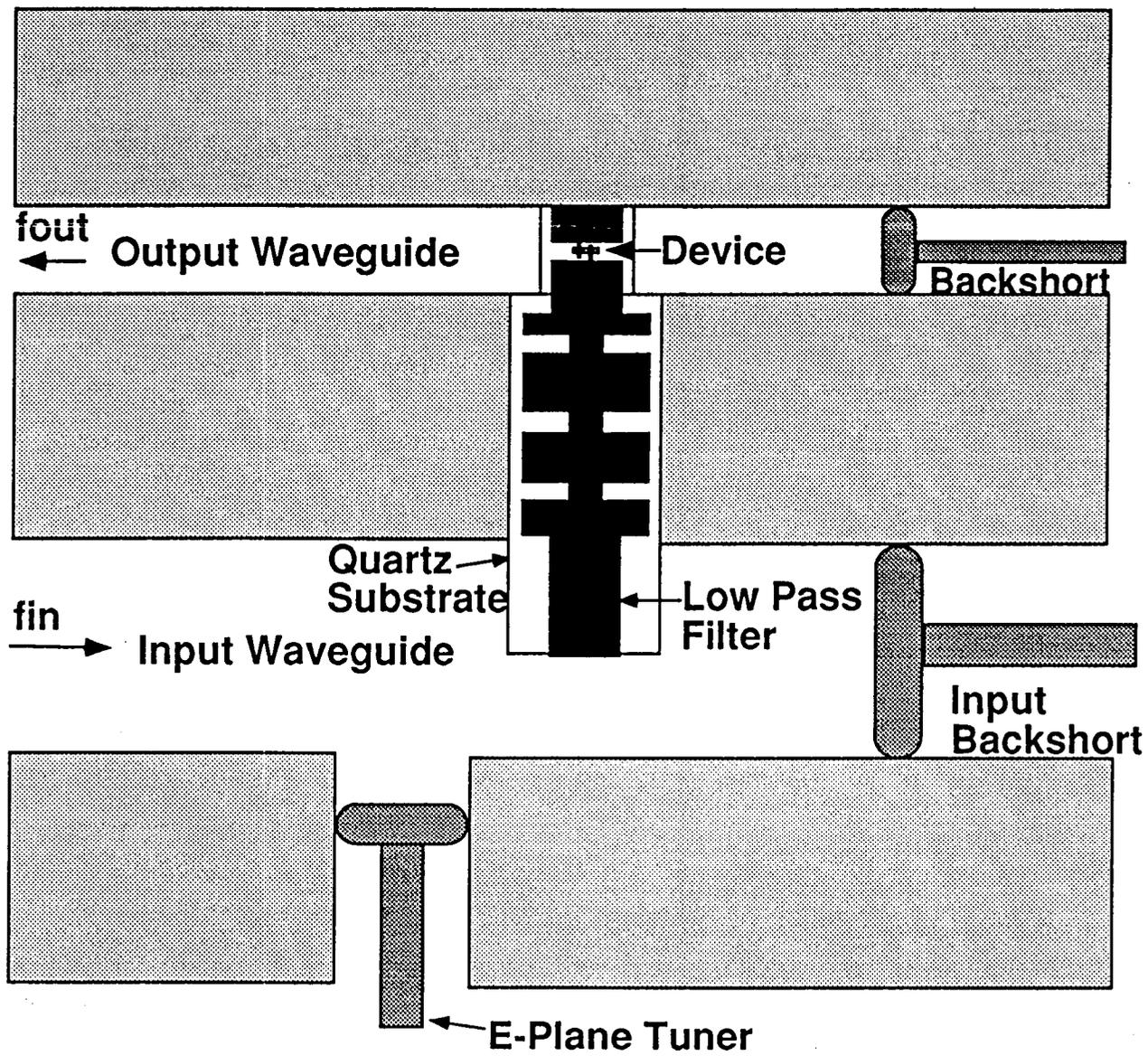


Fig. 9

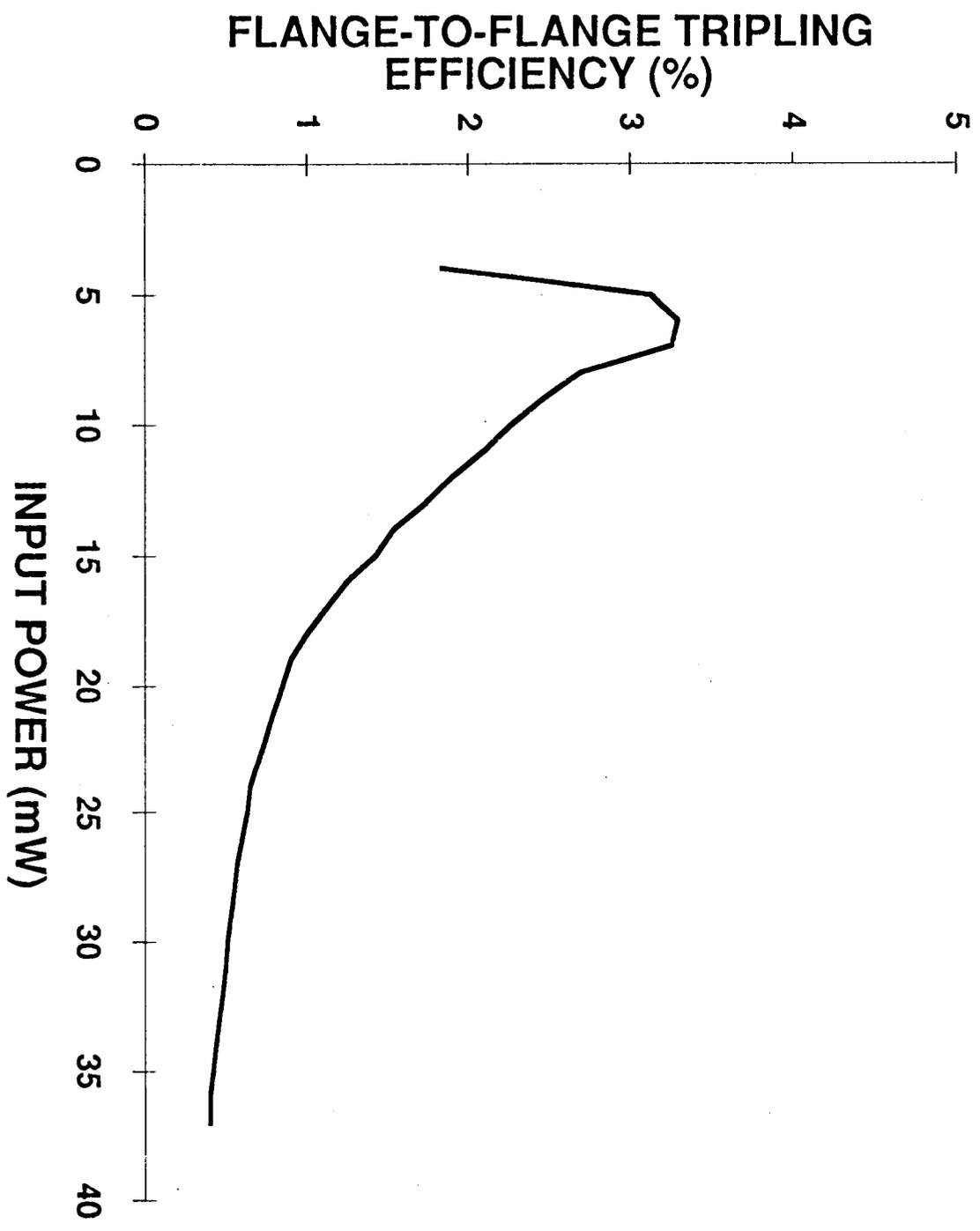


Fig. 10

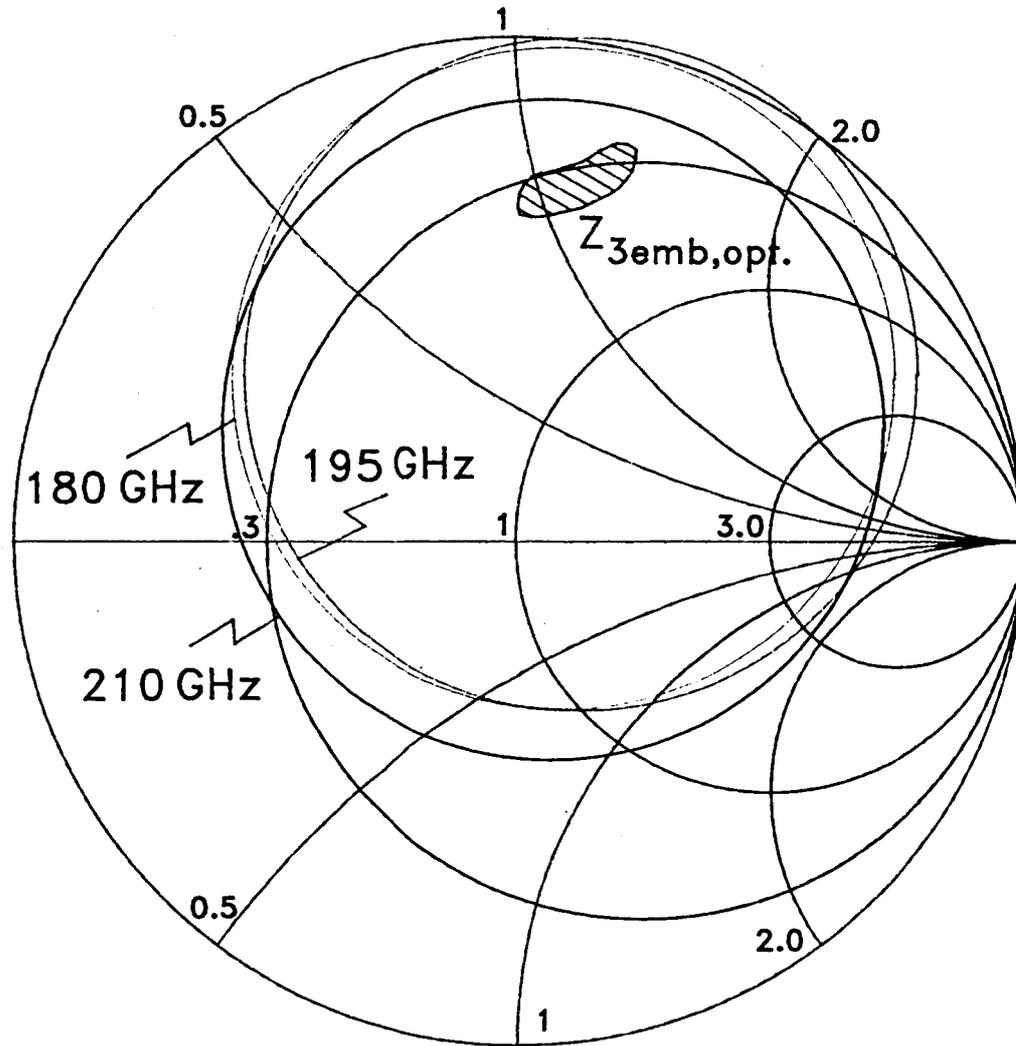


Fig. 11

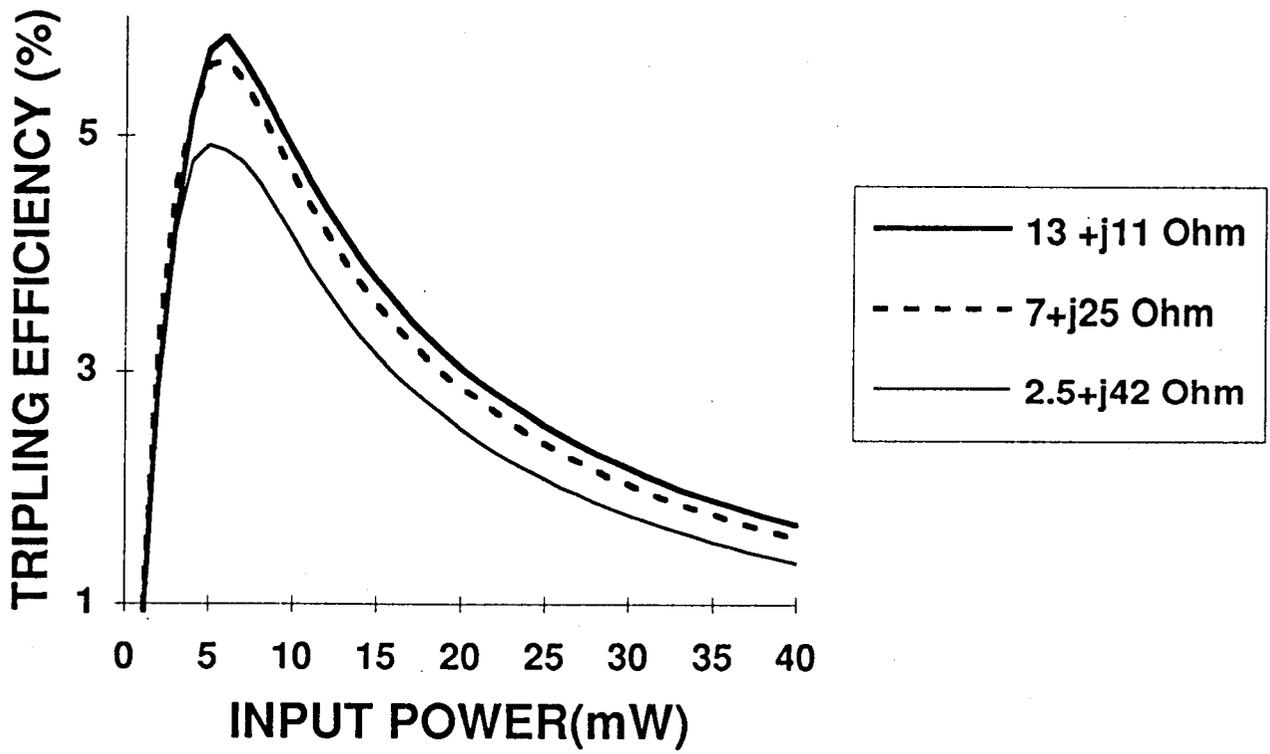


Fig. 12

Table - I

(a) $C_{max}=30$ IF and voltage needed to deplete the drift region is 2.32 V								
$\frac{C_{max}}{C_{min}}$	x_b (nm)	x_d (nm)	n_s (cm^{-2})	N_d (cm^{-3})	R_s (Ω)	$f_c RC$ (GHz)	$f_c - v_{sat}$ (GHz)	V_{bd} (volts)
5	150	1200	$5.00E+12$	$1.00E+17$	12.5	1660	796	19.6
4	150	900	$5.00E+12$	$1.66E+17$	10.6	1470	1061	15.5
3	150	600	$5.00E+12$	$3.33E+17$	9.5	1090	1592	11.3
2	150	300	$5.00E+12$	$1.00E+18$	9.1	571	3183	7.2

(b) $C_{min}=7.5$ IF and voltage needed to deplete the drift region is 2.32 V								
$\frac{C_{max}}{C_{min}}$	x_b (nm)	x_d (nm)	n_s (cm^{-2})	N_d (cm^{-3})	R_s (Ω)	$f_c RC$ (GHz)	$f_c - v_{sat}$ (GHz)	V_{bd} (volts)
5	123	980	$7.00E+12$	$1.45E+17$	10.98	1540	974	13.3
4	150	900	$5.00E+12$	$1.66E+17$	10.59	1470	1061	15.5
3	204	819	$3.70E+12$	$1.80E+17$	10.3	1370	1166	17
2	306	615	$2.47E+12$	$2.37E+17$	9.76	1090	1553	16.9

Table - II

(a) $C_{max}=15$ IF and voltage needed to deplete the drift region is 2.32 V								
$\frac{C_{max}}{C_{min}}$	x_b (nm)	x_d (nm)	n_s (cm^{-2})	N_d (cm^{-3})	R_s (Ω)	$f_c RC$ (GHz)	$f_c - v_{sat}$ (GHz)	V_{bd} (volts)
5	153	1225	$5.00E+12$	$2.00E+17$	12.6	3370	780	20
4	153	920	$5.00E+12$	$3.00E+17$	10.8	2950	1038	15.8
3	153	614	$5.00E+12$	$4.00E+17$	9.9	2150	1555	11.6
2	153	307	$5.00E+12$	$5.00E+17$	9.4	1130	3111	7.4

(b) $C_{min}=3.75$ IF and voltage needed to deplete the drift region is 2.32 V								
$\frac{C_{max}}{C_{min}}$	x_b (nm)	x_d (nm)	n_s (cm^{-2})	N_d (cm^{-3})	R_s (Ω)	$f_c RC$ (GHz)	$f_c - v_{sat}$ (GHz)	V_{bd} (volts)
5	122.75	980	$6.00E+12$	$1.40E+17$	11.9	2860	974	14.6
4	153	920	$5.00E+12$	$2.00E+17$	11.7	2720	1038	15.8
3	204	819	$3.70E+12$	$1.80E+17$	11.2	2530	1166	16.9
2	306.5	615	$2.47E+12$	$2.37E+17$	10.5	2020	1553	16.9

Table -III

(a) $C_{max}=7.5$ IF and voltage needed to deplete the drift region is 2.32 V

$\frac{C_{max}}{C_{min}}$	x_b (nm)	x_d (nm)	n_s (cm^{-2})	N_d (cm^{-3})	R_s (Ω)	f_{cRC} (GHz)	f_{c-vsat} (GHz)	V_{bd} (volts)
5	153.4	1220	5.00E+12	4.00E+17	12.6	6710	783	19.9
4	153.4	920	5.00E+12	5.50E+17	11	5810	1038	15.8
3	153.4	615	5.00E+12	6.00E+17	10.2	4170	1553	11.6
2	153.4	306	5.00E+12	7.00E+17	9.5	2230	3111	7.4

(b) $C_{min}=1.87$ IF and voltage needed to deplete the drift region is 2.32 V

$\frac{C_{max}}{C_{min}}$	x_b (nm)	x_d (nm)	n_s (cm^{-2})	N_d (cm^{-3})	R_s (Ω)	f_{cRC} (GHz)	f_{c-vsat} (GHz)	V_{bd} (volts)
5	122.6	985	5.00E+12	5.00E+17	11.3	6030	969	14.7
4	153.4	920	5.00E+12	5.50E+17	11	5810	1038	15.8
3	204	820	3.00E+12	6.00E+17	10.6	5350	1165	13.2
2	307	615	2.47E+12	7.00E+17	10	4240	1553	17